

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

**TC7MH175FK**

## Quad D-Type Flip-Flop with Clear

The TC7MH175FK is an advanced high speed CMOS quad D-type flip-flop fabricated with silicon gate C<sup>2</sup>MOS technology.

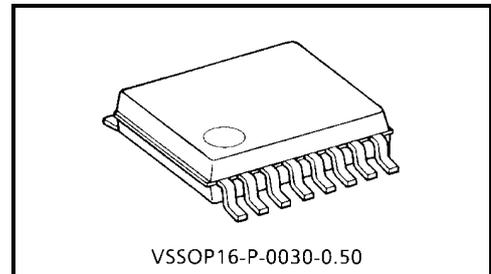
It achieves the high speed operation similar to equivalent bipolar schottky TTL while maintaining the CMOS low power dissipation.

These four flip-flops are controlled by a clock input (CK) and a clear input ( $\overline{\text{CLR}}$ ).

The information data applied to the D inputs (D1 thru D4) are transferred to the outputs (Q1 thru Q4 and  $\overline{\text{Q}}$ 1 thru  $\overline{\text{Q}}$ 4) on the positive-going edge of the clock pulse.

When the  $\overline{\text{CLR}}$  input is held low, the Q outputs are at the low logic level and the  $\overline{\text{Q}}$  outputs are at the high logic level, regardless of other input conditions.

An input protection circuit ensures that 0 to 7 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.



Weight: 0.02 g (typ.)

**Features**

- High speed:  $f_{\text{max}} = 210 \text{ MHz (typ.) (VCC = 5 V)}$
- Low power dissipation:  $I_{\text{CC}} = 4 \mu\text{A (max) (Ta = 25^\circ\text{C})}$
- High noise immunity:  $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC (min)}}$
- Power down protection is provided on all inputs.
- Balanced propagation delays:  $t_{\text{pLH}} \approx t_{\text{pHL}}$
- Wide operating voltage range:  $V_{\text{CC (opr)}} = 2\sim 5.5 \text{ V}$
- Low noise:  $V_{\text{OLP}} = 0.8 \text{ V (max)}$
- Pin and function compatible with 74ALS175

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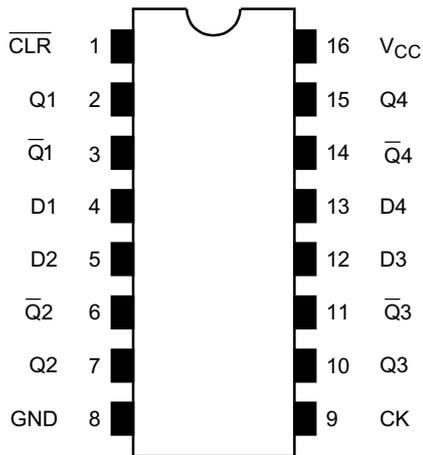
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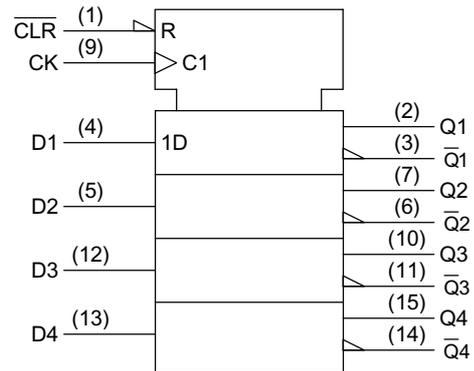
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## Pin Assignment (top view)



## IEC Logic Symbol

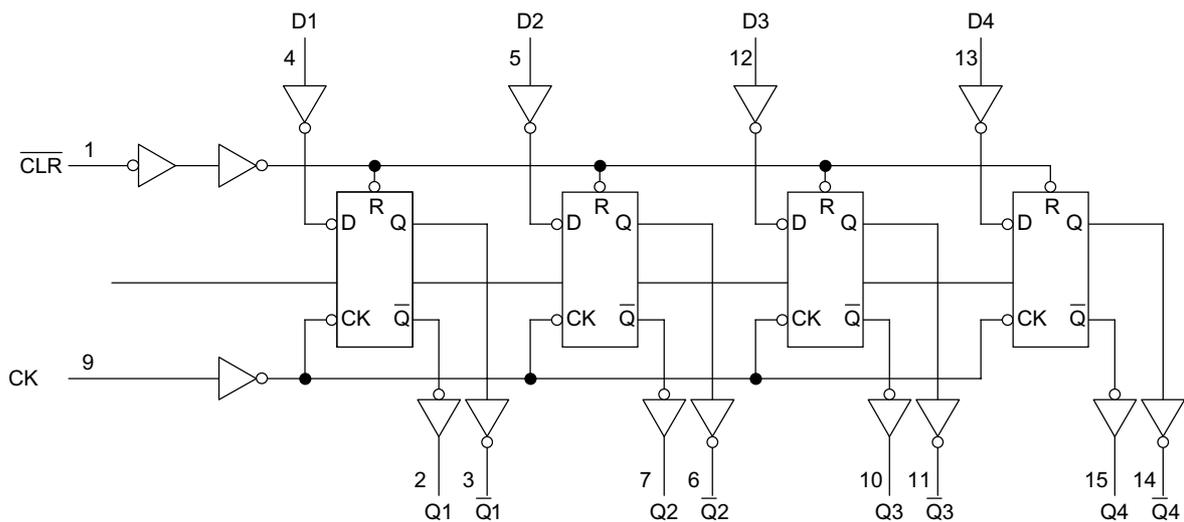


## Truth Table

Inputs			Outputs		Function
$\overline{\text{CLR}}$	D	CK	Q	$\overline{\text{Q}}$	
L	X	X	L	H	Clear
H	L	$\uparrow$	L	H	—
H	H	$\uparrow$	H	L	—
H	X	$\downarrow$	$Q_n$	$\overline{\text{Q}}_n$	No change

X: Don't care

## System Diagram



## Maximum Ratings

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5~7.0	V
DC input voltage	$V_{IN}$	-0.5~7.0	V
DC output voltage	$V_{OUT}$	-0.5~ $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	-20	mA
Output diode current	$I_{OK}$	±20	mA
DC output current	$I_{OUT}$	±25	mA
DC $V_{CC}$ /ground current	$I_{CC}$	±50	mA
Power dissipation	$P_D$	180	mW
Storage temperature	$T_{stg}$	-65~150	°C

## Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2.0~5.5	V
Input voltage	$V_{IN}$	0~5.5	V
Output voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating temperature	$T_{opr}$	-40~85	°C
Input rise and fall time	dt/dv	0~100 ( $V_{CC} = 3.3 \pm 0.3$ V) 0~20 ( $V_{CC} = 5 \pm 0.5$ V)	ns/V

## Electrical Characteristics

### DC Characteristics

Characteristics		Symbol	Test Condition	$T_a = 25^\circ\text{C}$			$T_a = -40\sim 85^\circ\text{C}$		Unit					
				$V_{CC}$ (V)	Min	Typ.	Max	Min		Max				
Input voltage	High level	$V_{IH}$	—	2.0 3.0~5.5	1.50 $V_{CC} \times 0.7$	— —	— —	1.50 $V_{CC} \times 0.7$	— —	V				
	Low level	$V_{IL}$	—	2.0 3.0~5.5	— —	— —	0.50 $V_{CC} \times 0.3$	— —	0.50 $V_{CC} \times 0.3$					
Output voltage	High level	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu\text{A}$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V			
				$I_{OH} = -4 \text{ mA}$	3.0 4.5	2.58 3.94	— —	— —	2.48 3.80	— —				
				Low level	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu\text{A}$	2.0 3.0 4.5	— — —	0 0 0		0.1 0.1 0.1	— — —	0.1 0.1 0.1
							$I_{OL} = 4 \text{ mA}$	3.0 4.5	— —	— —		0.36 0.36	— —	0.44 0.44
	Input leakage current	$I_{IN}$	$V_{IN} = 5.5 \text{ V or GND}$				0~5.5	—	—	±0.1		—	±1.0	μA

**Timing Requirements (Input:  $t_r = t_f = 3 \text{ ns}$ )**

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40~85°C		Unit
			V <sub>CC</sub> (V)	Typ.	Limit	Limit	
Minimum pulse width (CK)	$t_w(L)$ $t_w(H)$	—	3.3 ± 0.3	—	5.0	5.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum pulse width ( $\overline{\text{CLR}}$ )	$t_w(L)$	—	3.3 ± 0.3 5.0 ± 0.5	—	5.0 5.0	5.0 5.0	ns
Minimum set-up time	$t_s$	—	3.3 ± 0.3 5.0 ± 0.5	—	5.0 4.0	5.0 4.0	ns
Minimum hold time	$t_h$	—	3.3 ± 0.3 5.0 ± 0.5	—	1.0 1.0	1.0 1.0	ns
Minimum removal time ( $\overline{\text{CLR}}$ )	$t_{rem}$	—	3.3 ± 0.3 5.0 ± 0.5	—	5.0 5.0	5.0 5.0	ns

**AC Characteristics (Input:  $t_r = t_f = 3 \text{ ns}$ )**

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40~85°C		Unit			
			V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Typ.		Max	Min	Max
Propagation delay time (CK-Q)	$t_{pLH}$ $t_{pHL}$	—	3.3 ± 0.3	15	—	7.5	11.5	1.0	13.5	ns
				50	—	10.0	15.0	1.0	17.0	
			5.0 ± 0.5	15	—	4.8	7.3	1.0	8.5	
				50	—	6.3	9.3	1.0	10.5	
Propagation delay time ( $\overline{\text{CLR}}$ -Q)	$t_{pHL}$	—	3.3 ± 0.3	15	—	6.3	10.1	1.0	12.0	ns
				50	—	8.8	13.6	1.0	15.5	
			5.0 ± 0.5	15	—	4.3	6.4	1.0	7.5	
				50	—	5.8	8.4	1.0	9.5	
Maximum clock frequency	$f_{max}$	—	3.3 ± 0.3	15	90	140	—	75	—	MHz
				50	50	75	—	45	—	
			5.0 ± 0.5	15	150	210	—	125	—	
				50	85	115	—	75	—	
Output to output skew	$t_{osLH}$ $t_{osHL}$	(Note1)	3.3 ± 0.3	50	—	—	1.5	—	1.5	ns
			5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input capacitance	C <sub>IN</sub>	—	—	—	4	10	—	10	pF	
Power dissipation capacitance	C <sub>PD</sub>	(Note2)	—	—	44	—	—	—	pF	

Note1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note2: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per bit)}$$

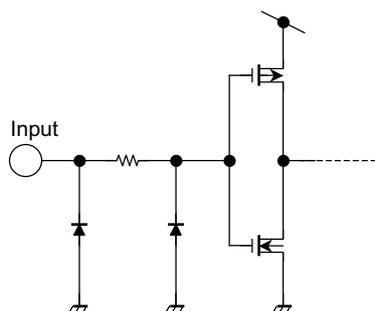
And the total C<sub>PD</sub> when n pcs of flip-flop operate can be gained by the following equation:

$$C_{PD} \text{ (total)} = 30 + 14 \cdot n$$

## Noise Characteristics (Input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			V <sub>CC</sub> (V)	Typ.	Limit	
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	C <sub>L</sub> = 50 pF	5.0	0.4	0.8	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	C <sub>L</sub> = 50 pF	5.0	-0.4	-0.8	V
Minimum high level dynamic input voltage V <sub>IH</sub>	V <sub>IHD</sub>	C <sub>L</sub> = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage V <sub>IL</sub>	V <sub>ILD</sub>	C <sub>L</sub> = 50 pF	5.0	—	1.5	V

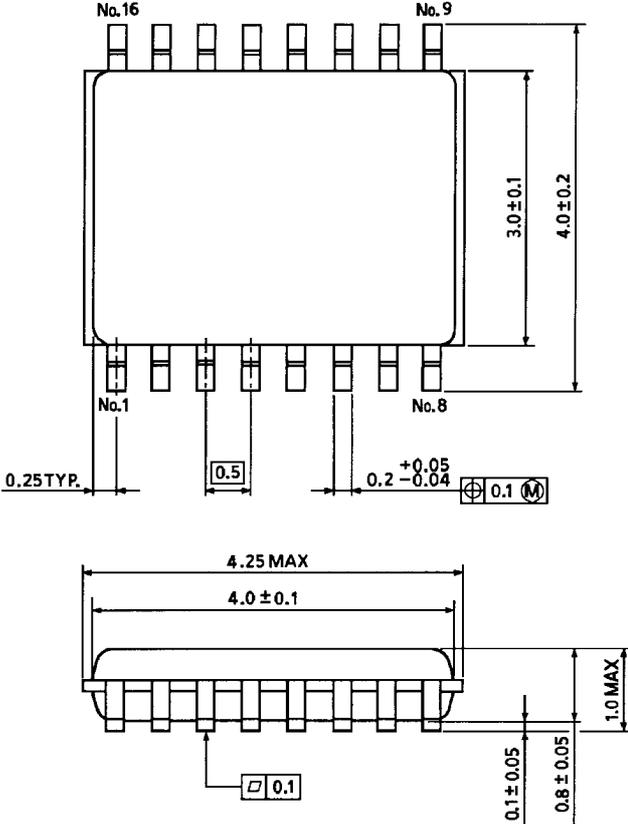
## Input Equivalent Circuit



Package Dimensions

VSSOP16-P-0030-0.50

Unit : mm



Weight: 0.02 g (typ.)