TOSHIBA CMOS Integrated Circuit Silicon Monolithic

J T 6 N 3 8 S

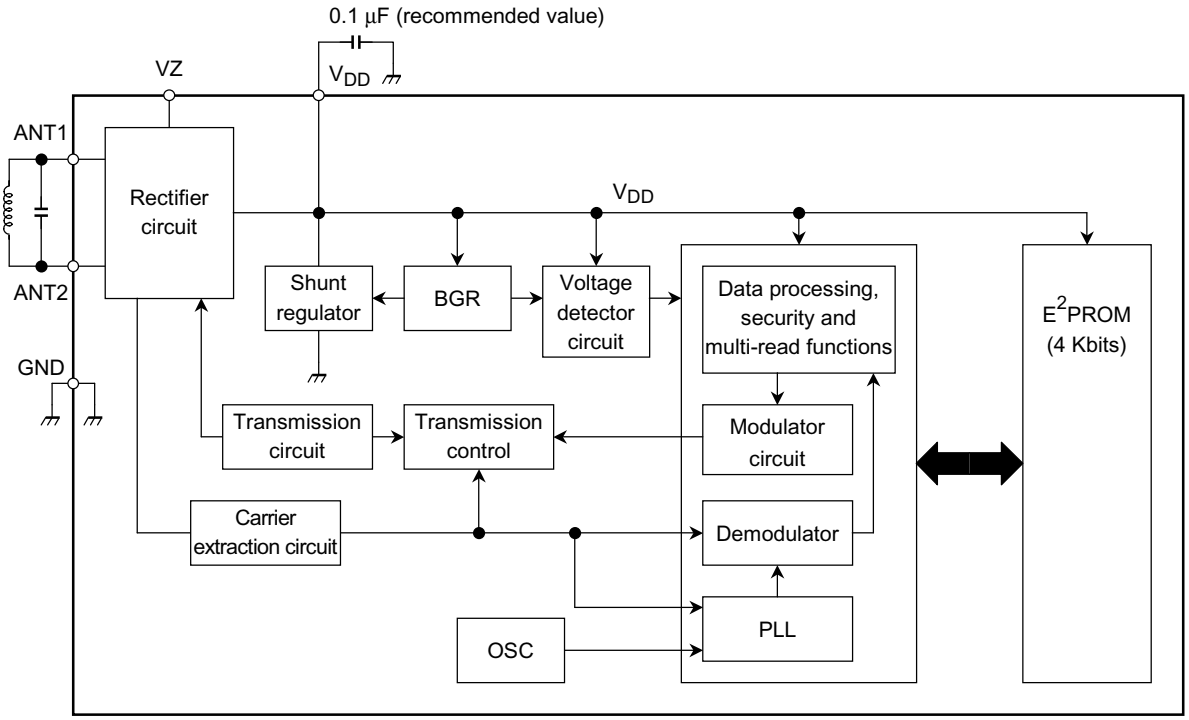
Single-Chip System LSI for RFID Card

The JT6N38S is a system LSI for radio frequency identification (RFID) wireless cards. The JT6N38S incorporates an analog circuit, a data processing circuit and data memory in a single chip.

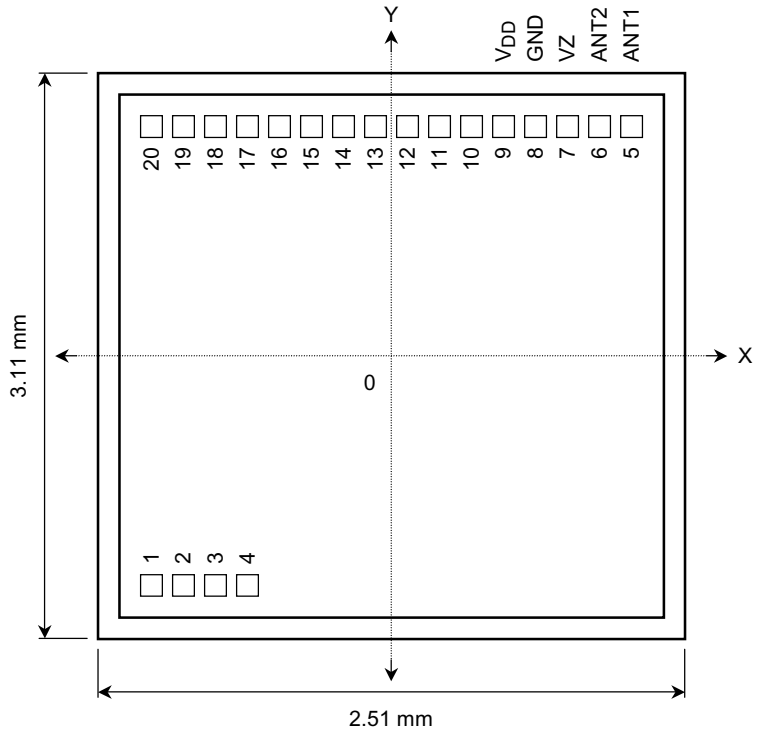
Features

- High-noise-resistant PSK modulation:
  binary phase-shift keying (BPSK) for both reader-to-RFID and RFID-to-reader transmission.
- Start-stop synchronization and half-duplex transmission: with parity, 1 stop bit
- High-efficiency power generation circuit using electromagnetic induction:
  battery less operation, full-wave rectifier circuit, shunt regulator
- Data processing logic circuit: digital PLL, security circuit
- High-reliablity E^2PROM: 4 Kbits
  Maximum write time: 7 ms (16-byte batch write)
  Overwrite: 100,000 times
  Data retention: 10 years
- Selectable receive carrier frequency: 120 kHz to 500 kHz (when external antenna circuit is used)
- Serial transmitter circuit (for active PSK): long-distance communication supported
- Programmable security circuit: security level can be set
- High-speed transfer rate of 25 kbps: 1/16 of receive carrier frequency = 400 kHz
- High-speed multi-read of 32 IDs per second: when receive carrier frequency = 400 kHz (ID only read)
- Supplied as chips or on wafer
  Chip thickness: 175 μm (typ.)

System Block Diagram



Pad Allocation



Pad Coordinates

Pad No.	Pad Name	X-Coordinate (μm)	Y-Coordinate (μm)
1	Test pin	−989	−1419
2	Test pin	−849	−1419
3	Test pin	−709	−1419
4	Test pin	−569	−1419
5	ANT1	1108	1419
6	ANT2	968	1419
7	Test pin	828	1419
8	GND	688	1419
9	V_{DD}	548	1419
10	Test pin	408	1419
11	Test pin	268	1419
12	Test pin	128	1419
13	Test pin	−12	1419
14	Test pin	−152	1419
15	Test pin	−292	1419
16	Test pin	−432	1419
17	Test pin	−572	1419
18	Test pin	−712	1419
19	Test pin	−852	1419
20	Test pin	−1000	1419

Note: Values for X-and Y-coordinates are pad center values.

Pin Functions

Pin No.	Symbol	Function
5	ANT1	Rectifier diode input, antenna connection pin 1
6	ANT2	Rectifier diode input (carrier extraction input side), antenna connection pin 2
7	VZ	Bridge diode output for rectification
8	GND	GND-internal circuit voltage reference
9	V_{DD}	Power supply for regulator voltage and internal circuits
1~4, 10~20	—	LSI test pins

LSI External Specifications

Parameter	Specifications
Power supply	Battery less-externally supplied by electromagnetic induction
Coupling type	Electromagnetic induction
Power feed frequency	120 kHz~500 kHz Note: External devices such as antenna and capacitors must be selected.
Communications method	Receive: PSK, Transmission: PSK (carrier frequency is half the power feeding frequency)
Transfer speed	1/16 of power feeding frequency
Transfer method	Half-duplex start-stop synchronization transmission (with parity, 1 stop bit)
Memory size	4-Kbit E^2PROM (512 bits are used as security area.)
Write time	7 ms max (for batch write of 16 bytes)
Control circuit	Key checking and access level control by hardware • Incorporates six access keys (6-byte key and 2-byte status). • Using access keys, read-only or write/read privilege can be set independently for each 64-byte area (programmable security). • Block write or read in units of 16 bytes using an access key and physical address. • Controls multi-read using Multi-Read command.
Multi-read	32 reads/s (typical value with power feed frequency of 400 kHz)
Operating temperature	−20°C~+85°C

Functions and Specifications of the Core Block

The JT6N38S is comprised of the following: an RF analog block for power generation, carrier extraction and regulation, and a digital block for data modulation, demodulation and data processing an E^2PROM for data storage.

1. Analog Block

(1) Rectifier circuit
Receives radio wave via the (external) antenna circuit and generates DC power for operating internal circuits with full-wave rectification.

(2) Shunt regulator
Maintains the voltage generated by the rectifier circuit at a fixed voltage, 3.1 V (typ.).
The digital circuits and E^2PROM operate using the voltage supplied by the shunt regulator.
The shunt regulator also protects internal circuits from the effects of strong electric fields.

(3) Carrier extraction circuit
Shapes the PSK-processed received carrier in to a square wave which is then input to the logic circuits for demodulation.

(4) Oscillation circuit (OSC)
Generates a clock for the digital PLL in the logic block.
(Oscillation frequency range: 8 MHz~12 MHz)

(5) Transmitter circuit (serial transmitter circuit for active PSK)
Powerfully modulates transmission by switching the line between the rectifier circuit and the shunt regulator. The switching is performed at half the received carrier frequency. That is, the transmission carrier frequency is half the received carrier frequency.
Note that when the rectifier circuit and the shunt regulator are left open, protection is performed for the bridge rectifier circuit so that the voltage at the bridge rectifier circuit is up to three times the remaining voltage of the shunt regulator.

(6) Voltage detector
Supports three types of voltage detector circuit for initializing the system and enabling/disabling E^2PROM writing. As a result, operation is always stable.

2. Digital Block

(1) Demodulator
Converts the PSK signal shaped by the carrier extraction circuit of the analog block into binary data.

(2) Digital PLL
Compares the frequency of the oscillator circuit in the analog block with the signal shaped by the carrier extraction circuit and generates a clock with a fixed frequency for operation of the entire digital block. Using the clock the internal LSI operates in synchronize with the carrier.

(3) Data processing
Processes data according to the commands received. Processes include parity check, E^2PROM write and read, and reset of the entire LSI.

(4) Security logic
Six keys can be set simultaneously using the security area allocated to the E^2PROM. Using the keys, write/read, read or no access can be set in units of 64-byte blocks (obtained by dividing E^2PROM memory area by four). (For example, with key A, read/write for a particular block can be set, while with key B, read/write for all block can be set.)

(5) Status reply
Replies to a command from the R/W consist of the status followed by data. The status represents, the internal status of the LSI to the R/W. If the LSI status is normal, status data 00H is inserted at the beginning (without any parity, start or end bits) followed by the data. If the LSI status is abnormal, no data follows and only the status indicating the abnormality is sent. The bit corresponding to each abnormality condition which has occurred is set to 1 in the status field.

(6) Multi-read
Multi-read is a function used for reading multiple RFIDs in the communications area using the same reader/writer (R/W). An RFID (LSI) generates a random number internally using the Multi-Read command transmitted by the R/W. The RFID replies using the response timing determined by the corresponding time slot. Thus, replies from the different RFIDs will not conflict, enabling data to be received properly by the R/W.
Note: Depending on the reading environment, the ability to read all the data may fluctuate . In some cases, some data may be left unread (since it cannot be undetected). Toshiba recommend the use of an additional chip with a detection function other than the multi-read function.

Electrical Characteristics

1. Ratings

Parameter	Symbol	Operating Rating	Unit
Input current (between ANT1 → GND → ANT2)	I_{ANT}	DC30	mA
Operating temperature range	T_{opr}	−20~+85	°C
Storage temperature range	T_{stg}	−50~+150	°C

*: Unless otherwise specified, the specifications are within the above operating temperature range.

2. DC Characteristics (Ta = −20~+85°C)

Parameter	Symbol	Test Circuit	Description	Min	Typ.	Max	Unit
Minimum operating voltage 1	V_{DD} (min)	—	Minimum operating voltage excluding memory write (Voltage check pin is V_{DD}.)	—	2.0	2.2	V
Minimum operating voltage 2	V_{DD} (eew)	—	Minimum operating voltage including memory write (Voltage check pin is V_{DD}.)	—	2.7	2.9	V
Operating current dissipation 1	I_{DDopr1}	—	Current dissipation for operations excluding memory write (V_{DD} = 2.5 V)	—	400	600	μA
Operating current dissipation 2	I_{DDopr2}	—	Current dissipation for all operations including memory write (V_{DD} = 2.9 V)	—	600	900	μA
Reply Peak Voltage	V_{psk}	—	Peak voltage of VZ pin at reply (V_{DD} as reference) times	—	2.5	—	

3. Operation Characteristics (Ta = −20~+85°C)

Parameter	Symbol	Test Circuit	Description	Min	Typ.	Max	Unit
Receive carrier frequency	f_{crr}	—	Carrier frequency at which operation is possible	120	—	500	kHz
Reply carrier frequency	f_{psk}	—	Carrier frequency at reply	fcrr × 1/2			kHz
Transfer rate	—	—	Transfer speed	fcrr × 1/16			bps
Receive 1-bit frequency	—	—	Receiving carrier frequency per bit	16			Cycles
Reply 1-bit frequency	—	—	Reply carrier frequency per bit	8			Cycles
E^2PROM write time	t_{pw}	—	—	—	—	7	ms
E^2PROM overwrite time	—	—	—	10^5	—	—	No. of times
E^2PROM data hold time	—	—	—	10	—	—	Years

Memory Map

Page No	16-Byte Block		Page No	16-Byte Block	
00H	ATR data		01H	Key 0010	Key 0011
02H	Key 0100	Key 0101	03H	Key 0110	Key 0111
04H	Any data		05H	Any data	
06H	Any data		07H	Any data	
08H	Any data		09H	Any data	
0AH	Any data		0BH	Any data	
0CH	Any data		0DH	Any data	
0EH	Any data		0FH	Any data	
10H	Any data		11H	Any data	
12H	Any data		13H	Any data	
14H	Any data		15H	Any data	
16H	Any data		17H	Any data	
18H	Any data		19H	Any data	
1AH	Any data		1BH	Any data	
1CH	Any data		1DH	Any data	
1EH	Any data		1FH	Any data	

Note 1: ATR: Answer to Reset. The LSI sends back the ATR data after receiving a reset command or self reset.

Note 2: Using the keys at 01H to 03H, access privileges can be set for the 64-byte blocks (enclosed by bold lines) from 04H to 1FH. A key area consists of 8 bytes.

Note 3: Write to E^2PROM is performed in units of 16 bytes to addresses matching the page numbers above.

The advantage of using this LSI is that it can be supplied as a single LSI for RFID allowing the user to configure peripherals (e.g. antennae, and reader/writers) so as to develop the desired system. However, because the peripheral environment may be highly user-specific, incompatibilities between the LSI and the user-configured environment (communications failures) may occur. Please carry out sufficient research before using this LSI.