

Preliminary

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC90A67F

Single Chip Picture-in-Picture IC (PAL/NTSC)

TC90A67F is a Picture-in-Picture (PIP) IC including a PIP controller and a PAL/NTSC decoder function on a chip. TC90A67F has an ADC, a video decoder, a vertical filter, a field memory, DACs and so on, so that it is easy to design a PIP application with the least external components.

Features

Video Decoder for the Sub-Picture

- NTSC, PAL (Europe), M-PAL and N-PAL systems
- Automatic color system identification
- 8-bit ADC for a composite video input
- Y/C separation by built-in digital filters
- ACC, Color killer circuits
- Contrast, Brightness, Tint and Color level controls
- Accessible V-chip signal data via. IIC bus

Main-Picture System Clock

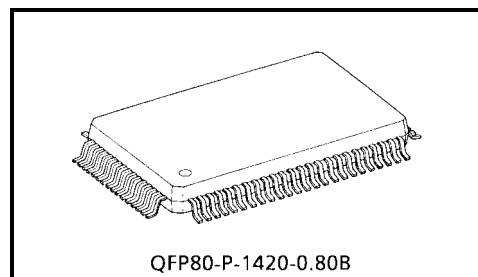
- External PLL circuit for main-picture system clock (A recommended IC TI: TLC2933)

PIP Controller

- 525-60 Hz, 626-50 Hz and mixed are available
- Vertical filter
- Field memory (181 kbit)
- PIP mode: Single PIP with 1/9 or 1/16 size, 6 PIPs with 1/36 size
- Flexible PIP position
- 3ch 8-bit DACs for YUV or RGB outputs
- YUV to RGB converter

Others

- 42 MHz crystal oscillator
- I²C bus control
- Package: QFP80
- Power supply: 3.3 V

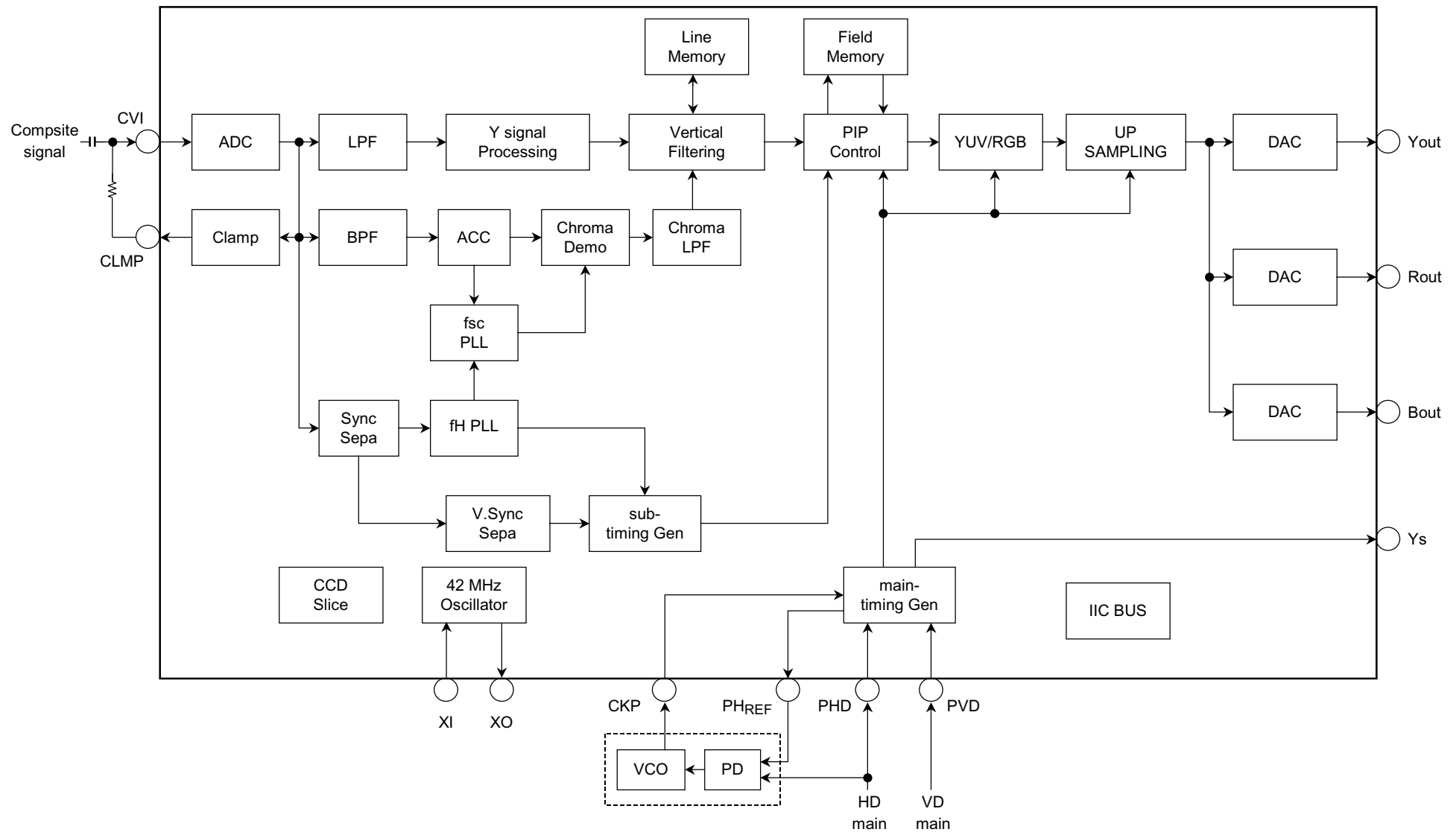


Weight: 1.6 g (typ.)

980910EBA1

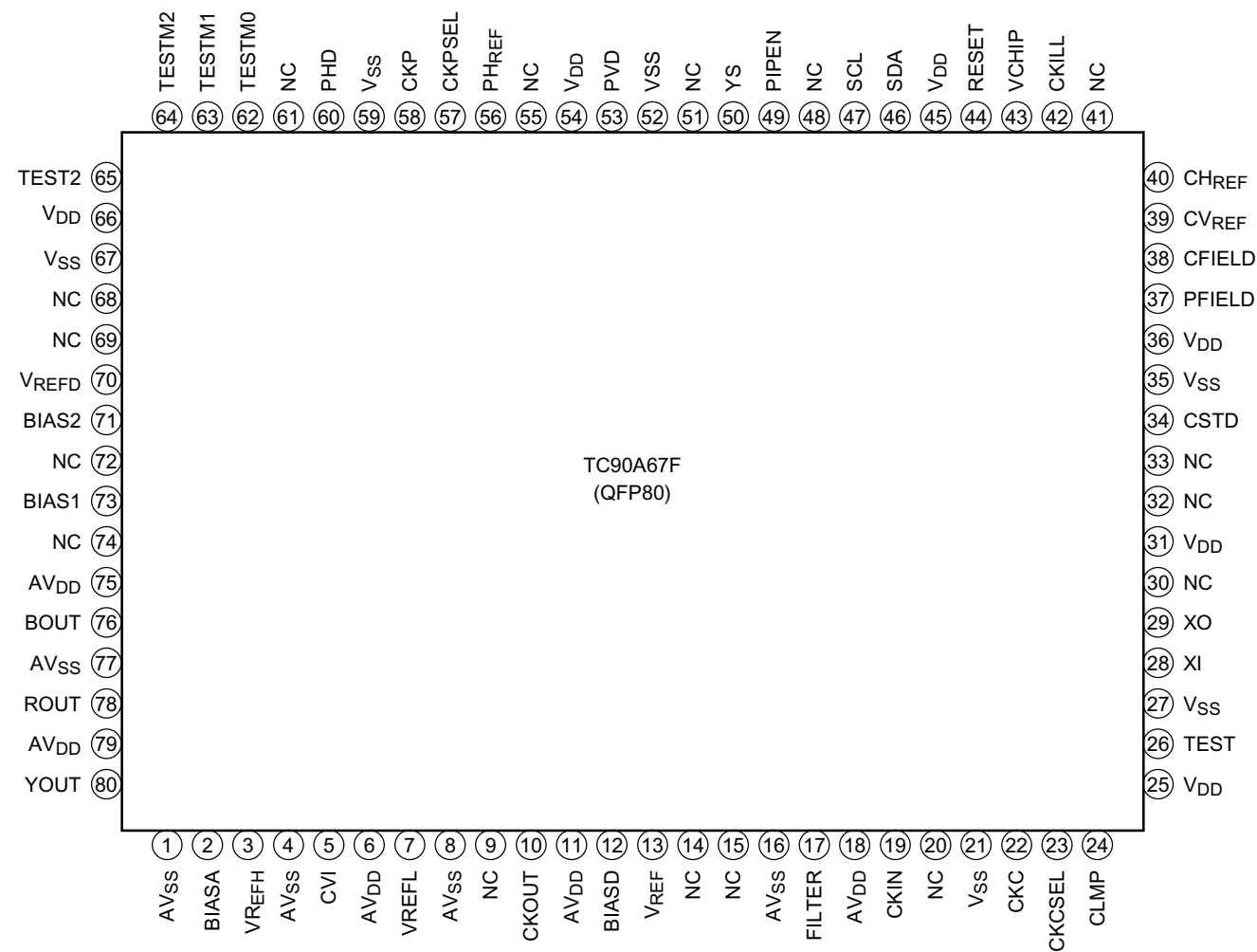
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Block Diagram



Terminal Connection Diagram

QFP80-P-1420-0.80B



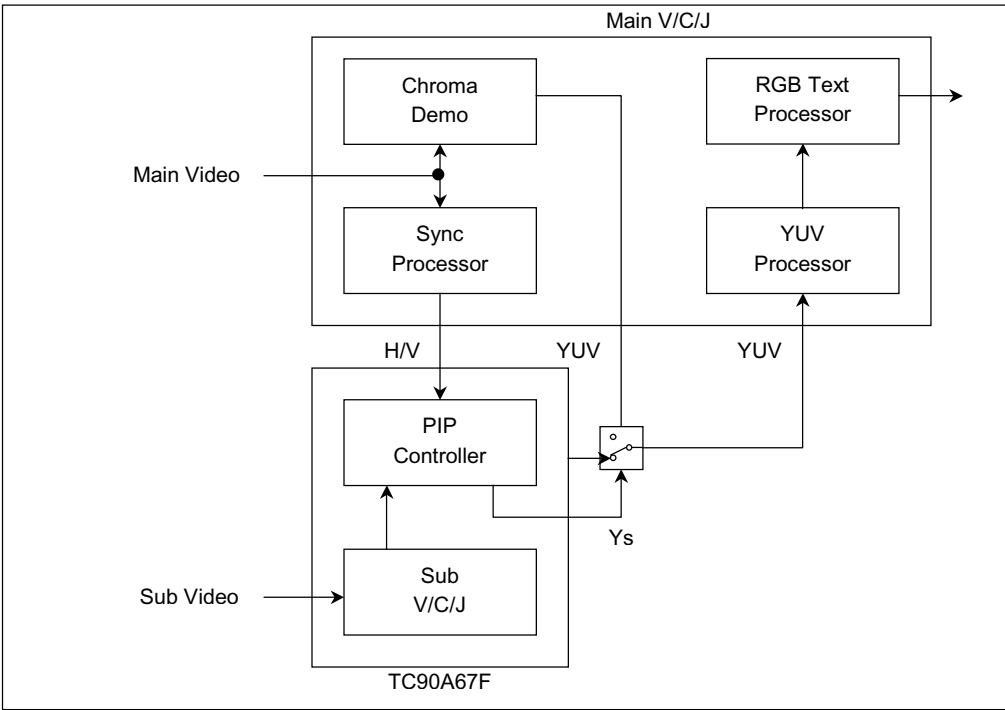
Terminal Function

QFP80-P-1420-0.80B

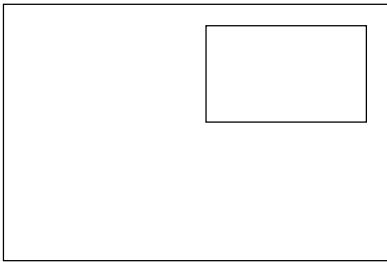
| PIN | Name | I/O | Function | Condition |
|-----|-------------------|-----|---------------------------------------|--------------------------|
| 1 | AV _{SS} | — | Ground for DAC | |
| 2 | BIASA | — | ADC bias voltage | |
| 3 | V _{REFH} | — | Upper limit reference voltage of ADC | normal: 2.3 V |
| 4 | AV _{SS} | — | Ground for ADC | |
| 5 | CVI | I | Composite video signal input | |
| 6 | AV _{DD} | — | Power supply for ADC | |
| 7 | V _{REFL} | — | Lower limit reference voltage of ADC | normal: 1.0 V |
| 8 | AV _{SS} | — | Ground for ADC | |
| 9 | NC | — | | |
| 10 | CKOUT | O | 384fH-clock output | |
| 11 | AV _{DD} | O | Power supply for VCO | |
| 12 | BIASD | — | DAC bias voltage | |
| 13 | V _{REF} | — | Lower limit reference voltage of DAC | normal: 1.8 V |
| 14 | NC | — | | |
| 15 | NC | — | | |
| 16 | AV _{SS} | — | Ground for VCO | |
| 17 | FILTER | O | VCO filter terminal | |
| 18 | AV _{DD} | — | Power supply for DAC | |
| 19 | CKIN | I | 384fH-clock input | |
| 20 | NC | — | | |
| 21 | V _{SS} | — | Ground for digital circuit | |
| 22 | CKC | I | Clock input (sub-picture) | |
| 23 | CKCSEL | I | Internal/external 384fH VCO select | L: internal, H: external |
| 24 | CLMP | O | Clamp level output | |
| 25 | V _{DD} | — | Power supply for digital circuit | |
| 26 | TEST | I | Test pin | normal: H |
| 27 | V _{SS} | — | Ground for crystal oscillator | |
| 28 | XI | I | 42 MHz crystal oscillator input | |
| 29 | XO | O | 42 MHz crystal oscillator output | |
| 30 | NC | — | | |
| 31 | V _{DD} | — | Power supply for crystal oscillator | |
| 32 | NC | — | | |
| 33 | NC | — | | |
| 34 | CSTD | O | Internal signal output | |
| 35 | V _{SS} | — | Ground for DRAM | |
| 36 | V _{DD} | — | Power supply for DRAM | |
| 37 | PFIELD | O | Field odd/even output (main picture) | H: even, L: odd |
| 38 | CFIELD | O | Field odd/even output (sub picture) | H: even, L: odd |
| 39 | CV _{REF} | O | Vertical sync. output (sub picture) | |
| 40 | CH _{REF} | O | Horizontal sync. output (sub picture) | |
| 41 | NC | — | | |

| PIN | Name | I/O | Function | Condition |
|-----|-------------------|-----|--|-------------------------------|
| 42 | CKILL | O | Color killer detection output (sub picture) | H: color killer ON, L: OFF |
| 43 | VCHIP | I | 23rd-line detect signal output | 23rd-line: H |
| 44 | RESET | I | Reset input | L: reset |
| 45 | V _{DD} | — | Power supply for digital circuit | |
| 46 | SDA | I/O | I ² C BUS data input, data and acknowledge output | |
| 47 | SCL | I | I ² C BUS clock input | |
| 48 | NC | — | | |
| 49 | PIPEN | I | PIP enable | normal: H |
| 50 | YS | O | Main, sub-picture switching pulse | sub-picture: high |
| 51 | NC | — | | |
| 52 | V _{SS} | O | Ground for digital circuit | |
| 53 | PVD | I | Vertical sync. input (main picture) | normal: negative |
| 54 | V _{DD} | O | Power supply for digital component | |
| 55 | NC | — | | |
| 56 | PHREF | O | Horizontal sync. output (main picture) | |
| 57 | CKPSEL | I | CKP frequency selection | L: 24 MHz, H: 48 MHz |
| 58 | CKP | I | Clock input (main-picture) | |
| 59 | V _{SS} | — | Ground for digital circuit | |
| 60 | PHD | I | Horizontal sync. input (main picture) | normal: positive |
| 61 | NC | — | | |
| 62 | TESTM0 | I | Test pin | normal: H |
| 63 | TESTM1 | I | Test pin | normal: H |
| 64 | TESTM2 | I | Test pin | normal: H |
| 65 | TEST2 | I | Test pin | normal: H |
| 66 | V _{DD} | — | Power supply for digital circuit | |
| 67 | V _{SS} | — | Ground for digital circuit | |
| 68 | NC | — | | |
| 69 | NC | — | | |
| 70 | V _{REFD} | I | Lower limit reference voltage of DAC | normal: 1.8 V |
| 71 | BIAS2 | — | DAC bias reference voltage | |
| 72 | NC | — | | |
| 73 | BIAS1 | — | DAC bias reference voltage | |
| 74 | NC | — | | |
| 75 | AV _{DD} | — | Power supply for DAC | |
| 76 | BOUT | O | Analog signal output (B-Y or B) | |
| 77 | AV _{SS} | — | Ground for DAC | |
| 78 | ROUT | O | Analog signal output (R-Y or R) | |
| 79 | AV _{DD} | — | Power supply for DAC | |
| 80 | YOUT | O | Analog signal output (Y or G) | |

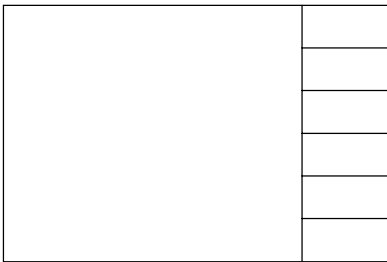
System Block Diagram



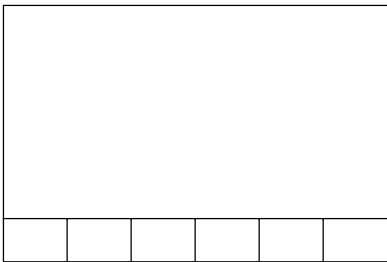
PIP Mode



1 PIP MODE
Size: 1/3, 1/4, 1/6



6 PIP MODE 1
Size: 1/6 × 6



6 PIP MODE 2
Size: 1/6 × 6

Function

TC90A67F has horizontal and vertical sync separation circuit for sub picture, color demodulation circuit for sub picture, horizontal and vertical timing generation circuit for main picture, PIP control circuit.

Color demodulation circuit consists of digital circuit, and corresponds to M-NTSC, PAL, M-PAL, N-PAL system. It is possible to process the sub picture easily, according to adopting system clock of 24 MHz by digital PLL circuit locked fH. Horizontal and vertical timing generation circuit uses system clock (24 MHz) generated by analog PLL circuit locked main picture's fH.

PIP control circuit consists of filter for horizontal and vertical reduction, line memory, field memory and according to changing horizontal and vertical reduction factors, it is possible to carry out various pip sizes.

1. ADC, Clamping Circuit

Dynamic range of ADC is $1.32 V_{p-p}$ whose voltage is fixed in IC. (top voltage is 2.31 V, bottom voltage is 0.99 V) ADC has pedestal clamp function, base voltage is output from CLMP terminal. The pedestal level becomes about 1.32 V. (64LSB)

2. Horizontal and Vertical Sync for Main Picture

It is necessary to input main picture's H-sync and V-sync at PHD and PVD terminal in order to make system clock for readout stored data into the internal field memory. PHD and PVD are fitted to 5 V. It can be inverted the polarity using IICBUS registers WHINV and WNINV at sub address 29hex.

At terminals of IC, polarity of H-sync is positive and V-sync is negative.

The clocks from external VCO are selectable in 24 MHz and 48 MHz, it can be switched by given voltage to CKPSEL (SDIP: 52 pin, QFP: 57 pin) terminal. (CKPSEL = L: 24 MHz, CKPSEL = H: 48 MHz)

3. The System Clock Locked to the Sub Picture's Horizontal Sync.

The signal converted into the digital environment passes through horizontal sync separation circuit, horizontal locked circuit, which construct PLL circuit, it makes the system clock locked to the sub picture's horizontal sync.

This clock is put in internal VCO and generated the system clock of 24 MHz.

4. Horizontal Reduction

It is necessary to limit to frequency bandwidth for Y signal and color difference signal concerning PIP mode. Horizontal reduction is selectable using HWS. (HWS: sub address 10hex)

| HWS [1:0] | Horizontal Reduction | Sampling Rate for Y | Sampling Rate for Color Difference |
|-----------|----------------------|---------------------|------------------------------------|
| 00 | 1/3 | 4 MHz | 1 MHz |
| 01 | 1/4 | 3 MHz | 0.75 MHz |
| 10 | 1/6 | 2 MHz | 0.5 MHz |
| 11 | 1/8 | 1.5 MHz | 0.375 MHz |

In order to horizontal reduction, LPFs are used for Y signal and color difference signal.

It is selectable in two kinds of LPF for Y signal and six kinds of LPF for color difference signal.

5. Vertical Reduction

It is necessary to reduce vertical direction concerning PIP mode, and vertical reduction is carried out from multiplication of coefficient as below. Vertical reduction is selectable using VWS.

(VWS: sub address 10hex)

| Vertical Reduction | 1H Coefficient | 2H Coefficient | 3H Coefficient | 4H Coefficient | 5H Coefficient | 6H Coefficient |
|----------------------|----------------|----------------|----------------|----------------|----------------|----------------|
| 1/3 (VWS [1:0] = 00) | 1/4 | 1/2 | 1/4 | — | — | — |
| 1/4 (VWS [1:0] = 01) | 1/8 | 3/8 | 3/8 | 1/8 | — | — |
| 1/5 (VWS [1:0] = 10) | 1/16 | 1/4 | 3/8 | 1/4 | 1/16 | — |
| 1/6 (VWS [1:0] = 11) | 1/16 | 3/16 | 1/4 | 1/4 | 3/16 | 1/16 |

6. The Sub Picture's Area of Writing in the Field Memory and Reading from the Field Memory

Writing start position is defined horizontal start point to write (sub address 16hex: CHS) and vertical start point to write. (sub address 16hex: CVSN or sub address 17hex: CVSP)

CVSN: Vertical frequency of sub picture is 60 Hz

CVSP: Vertical frequency of sub picture is 50 Hz

Horizontal width of the sub picture is defined by sampling number of horizontal direction. (sub address 1Ahex: HSPL) The number of writing vertical lines is determined internally according to vertical frequency of the main picture and VWS.

Reading start position is defined horizontal start point to read (sub address 14hex: PHS) and vertical start point to read. (sub address 14hex: PVSN or 15hex: PVSP)

PVSN: Vertical frequency of sub picture is 60 Hz

PVSP: Vertical frequency of sub picture is 50 Hz

Horizontal display size of the sub picture is defined by PHW (sub address 12hex) and the readout number of vertical lines is defined by PVWN (sub address 12hex) or PVWP (sub address 13hex).

PVWN: Vertical frequency of sub picture is 60 Hz

PVWP: Vertical frequency of sub picture is 50 Hz

7. DACs for Y Signal and Color Difference Signal

TC90A67F is built-in three 8 bit-DAC in motion on 24 MHz. Output dynamic range is determined by the difference between VDD and VREFD terminal voltage. Standard level is 1.5 V_{p-p}.

8. ACC Control

ACC control is carried out comparing demodulation result of color burst signal with set reference level by ACCPAL or ACCNTSC register. (ACCPAL, ACCNTSC: sub address 21hex)

When compared value is less than the reference level, controller puts on gain, and more than reference level, controller cuts down one.

9. Peaking Circuit for Y Signal

It is possible to carry out a clear picture according to putting up some frequency bandwidth when sub picture becomes indistinct picture for reducing high frequency bandwidth using LPF for Y signal. There are two kinds of characteristics for LPF, and it is selectable about gain of four stages respectively using YPKGS and YPKGG.

YPKGS: select for LPF characteristics (sub address 10hex)

YPKGG: select for gain (sub address 10hex)

10. PGB Matrix Circuit

For a built-in RGB matrix circuit, and when RGBON = 1, it can be changed R-Y, Y, B-Y into RGB signal. How to find the value of coefficient (a, b, c) is as below.

1Chex: MTXCR: a, MTXCG2: b, MTXCG1: c (on condition $0 \leq a < 1$, $0 \leq b < 1$, $0 \leq c < 1$)

$R = a(R - Y) + Y$

$G = b\{-(R - Y)\} + c\{-(B - Y)\} + Y$

$B = (B - Y) + Y$

11. Blue Back Function

It is possible to control blue back function using BBACK register.

(BBACK: sub address 13hex, BBACK = 1: blue back mode)

It is available for only sub picture set to live mode. BBACK is useful when detected V chip or no signal. it can be selected in four kinds of colors using BLEVEL.

(BLEVEL: sub address 13hex)

12. Addition of Frame

It is possible to add the frame to the sub picture. It is selectable frame width by FRAMEW and adjustable frame color for RGB or R-Y, Y, B-Y respectively by FRAMEYG, FRAMER, FRAMEB.

(FRAMEW, FRAMEYG, FRAMER, FRAMEB: sub address 1Ehex)

13. CCD Slice Circuit

This IC has a CCD slice circuit, picks up CCD data, the CCD data and CCD slice conditions can be checked on using IIC BUS read mode.

Bus Map (the value in parentheses indicate presetted data. the parts of mesh is fixed, input the indicated value.)

| Sub Address | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|------------------|--------------------|---------------------|-------------------|--------------------|------------------|--------------------|--------------------|-------------------|--------------------|------------------|---------------|----------------|---------------|---|
| 00 (READ) | CR13DET | CRIN [3:0] | | | | CFIELD | SBDDET | AEDGE | BEDGE | SLV [6:0] | | | | | | |
| 01 (READ) | CCDATA [15:0] | | | | | | | | | | | | | | | |
| 02 (READ) | NOSIG | CVMD525 | CNOVPN | CVDET60 | BCF [1:0] | | PVMD525 | PNOVPN | PVDET60 | CKIL | PD UNLOCK | PALDET | | | | |
| 10 | 0 | TRAPFIX (0) | TRAP358 (0) | YDLY1 [1:0] (1) | | YPKGS (0) | YLPFS (0) | YPKGG [1:0] | | CLPF [2:0] | | | VWS [1:0] (0) | | HWS [1:0] (0) | |
| 11 | 0 | 0 | MF (0) | STRO [3:0] (0) | | | TATEON (0) | PIPNUM [2:0] (0) | | | RON (0) | MSNUM [2:0] (0) | | | MSON (0) | |
| 12 | PHW [6:0] (31) | | | | | | PVWN [8:0] (04A) | | | | | | | | | |
| 13 | BBACK (0) | BLEVEL [1:0] (0) | | SELGAIN (0) | PHW 0 [2:0] (0) | | | PVWP [8:0] (05C) | | | | | | | | |
| 14 | PHS [7:0] (2B) | | | | | | PVSIN [7:0] (99) | | | | | | | | | |
| 15 | PHC [6:0] (00) | | | | | | PVSP [8:0] (83) | | | | | | | | | |
| 16 | CHS [7:0] (19) | | | | | | CVSN [7:0] (0A) | | | | | | | | | |
| 17 | BRTRGB [5:0] (00) | | | | | 1 | CVSP [8:0] (112) | | | | | | | | | |
| 18 | DRAMCLRN (0) | 1 | 0 | WADOS [12:0] (0000) | | | | | | | | | | | | |
| 19 | 0 | 0 | 0 | RADOS [12:0] (0000) | | | | | | | | | | | | |
| 1A | HSPL [5:0] (32) | | | | | CLVL [4:0] | | | | | CTRT [4:0] (00) | | | | | |
| 1B | 0 | 0 | HUEBIAS [5:0] (00) | | | | | HUE [7:0] (00) | | | | | | | | |
| 1C | MTXCB [5:0] (31) | | | | | MTXCG [24:20] (0C) | | | | | MTXCG [14:10] (0A) | | | | | |
| 1D | YGOS [5:0] (00) | | | | | ROS [4:0] (00) | | | | | BOS [4:0] (00) | | | | | |
| 1E | YSDLYS [1:0] (0) | | FRAMEW [1:0] (0) | | FRAMEYG [3:0] (0) | | | FRAMER [3:0] (0) | | | | FRAMEB [3:0] (0) | | | | |
| 1F | TYDLY [1:0] (0) | (0) | 0 | PMDFIX (0) | PMDS [1:0] (0) | OFF2527 (0) | SELREV (0) | 0 | 0 | 0 | 0 | 0 | PFLDREV (0) | CFLDREV (0) | RGBON (0) | |
| 20 | CHLOADN [7:0] (FE) | | | | | | | CHLOADP [7:0] (F9) | | | | | | | | |
| 21 | 0 | 0 | ACCPAL [6:0] (3A) | | | | | | ACCNTSC [6:0] (51) | | | | | | | |
| 22 | 0 | 0 | KILON [6:0] (0C) | | | | | | KILOFF [6:0] (14) | | | | | | | |
| 23 | 0 | 0 | NTSOFF [6:0] (14) | | | | | | NTSON [6:0] (0C) | | | | | | | |
| 24 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PIDREF [6:0] (76) | | | | | | |
| 25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | FSSTM [1:0] (1) | FSSEL [1:0] (0) | | FSMO [1:0] (1) | | |

| | | | | | | | | | | | | | | | | |
|-------------|-----------------|----|----|-----------|----------------|-----------|-------------------|---------|---------|---------|---|------------------|---|------------|--------------|------------|
| Sub Address | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 26 | SSLV [5:0] (20) | | | | | | CCDSBH [4:0] (0C) | | | | | CCDSBL [4:0] (4) | | | | |
| 27 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FLDSEL (1) | SELFLOOP (0) | SLVFIX (1) |
| 28 | 1 | 0 | 1 | 0 | CCDL [3:0] (8) | | | | F60 (0) | F50 (0) | 0 | 0 | 0 | 0 | 0 | WS262 (0) |
| 29 | 1 | 0 | 0 | WS262 (0) | WVINV (0) | WHINV (0) | F60 (0) | F50 (0) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Description of I²C Bus Registers

Write Command

| Sub Address | Bit | Name | Preset | Comment |
|-------------|----------|-------------|--------|--|
| 10H | D15 | — | 0 | Fix to '0' |
| | D14 | TRAPFIX | 0 | Change fsc-trap mode. 0: auto, 1: fix |
| | D13 | TRAP358 | 0 | Select fsc-trap characteristic. (active at TRAPFIX = 1 only) 0: 4.43 MHz, 1: 3.58 MHz |
| | D12, D11 | YDLY1 [1:0] | 01 | Y-output signal delay against U and V output signal (rough). |
| | D10 | YPKGS | 0 | Select Y-peaking filter characteristic. 0: hi-band, 1: low-band |
| | D9 | YLPFS | 0 | Select Y-horizontal decimation filter characteristic. 0: hi-band, 1: low-band |
| | D8, D7 | YPKGG [1:0] | 00 | Select Y-peaking gain level. 00: 0, 01: 1/4, 10: 1/2, 11: 1 |
| | D6 to D4 | CLPF [2:0] | 000 | Select R-Y/B-Y horizontal decimation filter characteristic. |
| | D3, D2 | VWS [1:0] | 00 | Select vertical decimation. 00: 1/3, 01: 1/4, 10: 1/5, 11: 1/6 |
| | D1, D0 | HWS [1:0] | 00 | Select horizontal decimation. 00: 1/3, 01: 1/4, 10: 1/6, 11: 1/8 |

| | | | | |
|-----|-----------|--------------|------|--|
| 11H | D15, D14 | — | 00 | Fix to '0' |
| | D13 | MF | 0 | Set single-field display mode. 0: normal, 1: Fixed to single-field display |
| | D12 to D9 | STRO [3:0] | 0000 | Select off-and-on cycle of field memory writing. (4 field step) 0000: normal 0001: strobe (once 6 fields) 1110: strobe (once 58 fields) 0010: strobe (once 10 fields) 1111: still |
| | D8 | TATEON | 0 | Sub-pictures' set at multi-pictures 0: horizontal, 1: vertical |
| | D7 to D5 | PIPNUM [2:0] | 000 | Set multi-picture numbers of the animation picture. |
| | D4 | RON | 0 | Sub-picture display ON/OFF. 0: OFF, 1: ON |
| | D3 to D1 | MSNUM [2:0] | 000 | Select multi-strobe pictures number. 000: 1-picture, 001: 2-pictures, 010: 3-pictures, 011: 4-pictures, 100: 5-pictures, 101: 6-pictures |
| | D0 | MSON | 0 | Select multi-strobe mode. (0: normal strobe mode, 1: multi-strobe mode) |

| | | | | |
|-----|-----------|------------|---------------|--|
| 12H | D15 to D9 | PHW [6:0] | 011000 1 | Sub-pictures range in the main-picture. (horizontal width, rough) |
| | D8 to D0 | PVWN [8:0] | 001001 010 | Sub-pictures range in the main-picture (vertical height) , when main-picture is 60 Hz system. |

| | | | | |
|-----|-----------|--------------|---------------|---|
| 13H | D15 | BBACK | 0 | Replace sub-picture by blue-back at write-memory. 0: normal, 1: blue-back |
| | D14, D13 | BLEVEL [1:0] | 00 | Select blue-back level. (DRAMCLR = 1 or BBACK = 1 only) 00: black, 01: blue1, 10: blue2, 11: blue3 |
| | D12 | SELGAIN | 00 | Control internal Y-level. 0: 1.5 times, 1: Twice |
| | D11 to D9 | PHE0 [2:0] | 000 | Sub-pictures range in the main-picture. (horizontal width, fine) |
| | D8 to D0 | PVWP [8:0] | 001011 100 | Sub-pictures range in the main-picture (vertical height) , when main-picture is 50 Hz system. |

| Sub Address | Bit | Name | Preset | Comment |
|-------------|-----------|------------|---------------|---|
| 14H | D15 to D8 | PHS [7:0] | 001010 11 | Horizontal starting point of the sub-pictures in the main-picture. |
| | D7 to D0 | PVSN [7:0] | 1001100 01 | Vertical starting point of the sub-pictures in the main-picture , when main-picture is 60 Hz system. |

| | | | | |
|-----|-----------|------------|---------------|---|
| 15H | D15 to D9 | PHC [6:0] | 000000 0 | Set clock frequency of main-picture processing. (set the dividing number of fH PLL.) |
| | D8 to D0 | PVSP [8:0] | 010000 011 | Vertical starting point of the sub-pictures in the main-picture , when main-picture is 50 Hz system. |

| | | | | |
|-----|-----------|------------|--------------|---|
| 16H | D15 to D8 | CHS [7:0] | 000110 01 | Horizontal starting point to write into the memory in the sub-picture. |
| | D7 to D0 | CVSN [7:0] | 000010 10 | Vertical starting point to write into the memory in the sub-picture at 60 Hz system. |

| | | | | |
|-----|------------|--------------|---------------|---|
| 17H | D15 to D10 | BRTRGB [5:0] | 000000 | Control bright at RGB mode. 100000: -32 LSB, 000000: 0 LSB, 011111: +31 LSB |
| | D9 | — | 1 | Fix to '1' |
| | D8 to D0 | CVSP [8:0] | 100010 010 | Vertical starting point to write into the memory in the sub-picture at 50 Hz system. |

| | | | | |
|-----|-----------|--------------|-----------------------|---|
| 18H | D15 | DRAMCLRN | 0 | Field-memory reset 0: normal, 1: reset |
| | D14 | — | 1 | Fix to '1' |
| | D13 | — | 0 | Fix to '0' |
| | D12 to D0 | WADOS [12:0] | 000000 000000 0 | Set start-address to write the memory. (for the memory partition to memorize several sub-pictures at the same time.) |

| | | | | |
|-----|------------|--------------|-----------------------|--|
| 19H | D15 to D13 | — | 000 | Fix to '0' |
| | D12 to D0 | RADOS [12:0] | 000000 000000 0 | Set start-address to read from the memory. (for the select of sub-pictures in the memory) |

| | | | | |
|-----|------------|------------|--------|---|
| 1AH | D15 to D10 | HSPL [5:0] | 110010 | Set number of horizontal sampling on the input sub-picture. |
| | D9 to D5 | CLVL [4:0] | 00000 | Set color-level. 10000: -6 dB, 00000: 0 dB, 01111: +6 dB |
| | D4 to D0 | CTRT [4:0] | 00000 | Set contrast level. 00000: +1 dB, 11111: +3.5 dB |

| | | | | |
|-----|-----------|---------------|--------------|--|
| 1BH | D15, D14 | — | 00 | Fix to '0' |
| | D13 to D8 | HUEBIAS [5:0] | 000000 | Adjustment the demodulation phases for R-Y signal. (NTSC only) 000000: 0°, 111111: +45° |
| | D7 to D0 | HUE [7:0] | 000000 00 | Adjustment the demodulation phase for R-Y and B-Y signals. (NTSC only) 10000000: -45°, 00000000: 0°, 01111111: +45° |

| Sub Address | Bit | Name | Preset | Comment |
|-------------|------------|---------------|--------|-------------------------------|
| 1CH | D15 to D10 | MTXCB [5:0] | 110001 | Set RGB matrix coefficient 1. |
| | D9 to D5 | MTXCG [24:20] | 01100 | Set RGB matrix coefficient 2. |
| | D4 to D0 | MTXCG [14:10] | 01010 | Set RGB matrix coefficient 3. |

| | | | | |
|-----|----------|------------|--------|--|
| 1DH | D15, D10 | YGOS [5:0] | 000000 | Set DC offset of sub-picture. (Y or G signal) 100000: -32 LSB, 000000: 0 LSB, 011111: +31 LSB |
| | D9 to D5 | ROS [4:0] | 00000 | Set DC offset of sub-picture. (R-Y or R signal) 10000: -16 LSB, 00000: 0 LSB, 01111: +15 LSB |
| | D4 to D0 | BOS [4:0] | 00000 | Set DC offset of sub-picture. (B-Y or B signal) 10000: -16 LSB, 00000: 0 LSB, 01111: +15 LSB |

| | | | | |
|-----|-----------|---------------|------|---|
| 1EH | D15, D14 | YSDLY [1:0] | 01 | Timing offset of Ys pulse. 00: -1 ck, 01: center, 10: +1 ck, 11: +2 ck (24 MHz) |
| | D13, D12 | FRAMEW [1:0] | 00 | Select the side frame width of sub-picture. 00: OFF (no-frame), 01: narrow, 10: center, 11: wide |
| | D11 to D8 | FRAMEYG [3:0] | 0000 | Select frame signal level of PIP. (Y or G signal) |
| | D7 to D4 | FRAMER [3:0] | 0000 | Select frame signal level of PIP. (R-Y or R signal) |
| | D3 to D0 | FRAMEB [3:0] | 0000 | Select frame signal level of PIP. (B-Y or B signal) |

| | | | | |
|-----|----------|-------------|-------|--|
| 1FH | D15, D14 | TYDLY [1:0] | 00 | Y-output signal delay for U and V output signal. (fine). |
| | D13 | — | 0 | Fix to '0' |
| | D12 | PMDFIX | 0 | Clock frequency to read from the memory. 0: auto, 1: fix |
| | D11, D10 | PMDS [1:0] | 00 | Select Clock frequency to read from the memory. (active at PMDFIX = 1 only) 00: 12 MHz, 01: 9 MHz, 10: 18 MHz, 11: 16 MHz |
| | D9 | OFF2527 | 0 | Set 50 Hz/ 60 Hz-conversion mode. (VWS = 1/3 mode only) 0: ON, 1: OFF |
| | D8 | SELREV | 0 | Set reverse mode. 0: normal, 1: reverse |
| | D7 to D3 | — | 00000 | Fix to '0' |
| | D2 | PFLDREV | 1 | Reverse PFIELD at internal circuit. 0: reverse, 1: normal |
| | D1 | CFLDREV | 0 | Reverse CFIELD at internal circuit. 0: normal, 1: reverse |
| | D0 | RGBON | 1 | Select output signal format. 0: YUV, 1: RGB |

| | | | | |
|-----|-----------|---------------|--------------|---|
| 20H | D15 to D8 | CHLOADN [7:0] | 111111 10 | Set clock frequency of sub-picture processing at 60 Hz system. (set the dividing number of H-PLL) |
| | D7 to D0 | CHLOADP [7:0] | 111110 01 | Set clock frequency of main-picture processing at 50 Hz system. (set the dividing number of H-PLL) |

| Sub Address | Bit | Name | Preset | Comment |
|-------------|-----------|---------------|-------------|--|
| 21H | D15, D14 | — | 00 | Fix to '0' |
| | D13 to D7 | ACCPAL [6:0] | 011101 0 | Set ACC reference level (for PAL). 0: Minimum level 127: Maximum level |
| | D6 to D0 | ACCNTSC [6:0] | 101000 1 | Set ACC reference level (for NTSC). 0: Minimum level 127: Maximum level |

| | | | | |
|-----|-----------|--------------|-------------|---|
| 22H | D15, D14 | — | 00 | Fix to '0' |
| | D13 to D7 | KILON [6:0] | 000110 0 | Set color killer ON level. 0: Minimum level 63: maximum level It must be set "KILON" < "KILOFF" |
| | D6 to D0 | KILOFF [6:0] | 001010 0 | Set color killer OFF level. 0: Minimum level 63: maximum level It must be set "KILON" < "KILOFF" |

| | | | | |
|-----|-----------|--------------|-------------|--|
| 23H | D15, D14 | — | 00 | Fix to '0' |
| | D13 to D7 | NTSOFF [6:0] | 001010 0 | Set level to turn over from NTSC to PAL in NTSC/PAL detector. 0: Minimum level 63: maximum level It must be set "NTSON" < "NTSOFF" |
| | D6 to D0 | NTSON [6:0] | 000110 0 | Set level to turn over from PAL to NTSC in NTSC/PAL detector. 0: Minimum level 63: maximum level It must be set "NTSON" < "NTSOFF" |

| | | | | |
|-----|-----------|--------------|---------------|---|
| 24H | D15 to D7 | — | 000000 000 | Fix to '0' |
| | D6 to D0 | PIDREF [6:0] | 111011 0 | Sensitivity of PAL-IDENT detection. 0: Minimum Sensitivity 63: Maximum Sensitivity |

| | | | | |
|-----|------------|-------------|------|--|
| 25H | D15 to D12 | — | 0000 | Fix to '0' |
| | D11 to D8 | — | 1111 | Fix to '1' |
| | D7, D6 | — | 00 | Fix to '0' |
| | D5, D4 | FSSTM [1:0] | 10 | Set cycle of color system detection in color sub-carrier frequency detector. (1field step) 0: 1 field 3: 4 fields |
| | D3, D2 | FSSEL [1:0] | 00 | Set color system of sub-picture processing. (at FSMO = 11 only) 00: N-PAL, 01: M-PAL, 10: M-NTSC, 11: BG-PAL/4.43NTSC |
| | D1, D0 | FSMO [1:0] | 01 | Mode for color sub-carrier frequency search 00: M-NTSC only, 01: BG-PAL/4.43NTSC→M-NTSC, 10: N-PAL→M-PAL→M-NTSC, 11: FSSEL [1:0] |

| | | | | |
|-----|------------|--------------|--------|---|
| 26H | D15 to D10 | SSLV [5:0] | 100000 | Set slice level for CCD. (this data is initial value of peak detector circuit at auto-slice mode.) |
| | D9 to D5 | CCDSBH [4:0] | 01100 | Set minimum-width of high-period in start-bit for CCD. |
| | D4 to D0 | CCDSBL [4:0] | 00100 | Set minimum-width of low-period in start-bit for CCD. |

| Sub Address | Bit | Name | Preset | Comment |
|-------------|-----------|----------|-----------------|--|
| 27H | D15, D14 | — | 11 | Fix to '1' |
| | D13 to D3 | — | 000000 00000 | Fix to '0' |
| | D2 | FLDSEL | 1 | Control CCD slice 1. |
| | D1 | SELPLOOP | 0 | Control CCD slice 2. |
| | D0 | SLVFIX | 0 | Fix CCD slice level. 0: fix, 1: auto-slice |

| | | | | |
|-----|-----------|------------|-------|--|
| 28H | D15 | — | 1 | Fix to '1' |
| | D14 | — | 0 | Fix to '0' |
| | D13 | — | 1 | Fix to '1' |
| | D12 | — | 0 | Fix to '0' |
| | D11 to D8 | CCDL [3:0] | 1000 | Set line No. of data slicing for CCD. 1000: 21 H (NTSC) |
| | D7 | F60 | 0 | Force 60 Hz mode (sub-picture). 0: normal, 1: force |
| | D6 | F50 | 0 | Force 50 Hz mode (sub-picture). 0: normal, 1: force |
| | D5 to D1 | — | 00000 | Fix to '0' |
| | D0 | WS262 | 0 | Reverse CFIELD polarity. 0: even high, 1: odd high |

| | | | | |
|-----|----------|-------|--------------|--|
| 29H | D15 | — | 0 | Fix to '0' |
| | D14, D13 | — | 11 | Fix to '1' |
| | D12 | WS262 | 0 | Reverse PFIELD polarity. 0: even high, 1: odd high |
| | D11 | WVINV | 0 | Set polarity of vertical sync pulse input at pin "PVD". (main-picture) 0: Negative, 1: Positive |
| | D10 | WHINV | 0 | Set polarity of horizontal sync pulse input at pin "PHD". (main-picture) 0: Positive, 1: Negative |
| | D9 | F60 | 0 | Force 60 Hz mode (main-picture) 0: OFF, 1: ON |
| | D8 | F50 | 0 | Force 50 Hz mode (main-picture) 0: OFF, 1: ON |
| | D7 to D0 | — | 000000 00 | Fix to '0' |

Read Command

| Sub Address | Bit | Name | Comment |
|-------------|------------|----------------|---|
| 00H | D15 | CRI3DET | CRI detection. |
| | D14 to D11 | CRIN [3:0] | CRI number detection. |
| | D10 | CFIELD | Field-detection. (sub-picture) 1: 1st field, 0: 2nd field |
| | D9 | SBDDET | Start-bit (001) detection. 0: not start-bit detected, 1: start-bit detected |
| | D8 | AEDGE | Caution of too near sampling point for back-edge of data. 0: OK, 1: too near |
| | D7 | BEDGE | Caution of too near sampling point for front-edge of data. 0: OK, 1: too near |
| | D6 to D0 | SLV [6:0] | Slice level data. |
| 01H | D15 to D0 | CCDDATA [15:0] | CCD data including parity bits. |
| 02H | D15 | NOSIG | Result of no-signal detection (sub-picture) 0: exist, 1: not-signal |
| | D14 | CVMD525 | Vertical sync frequency standard/non-standard detection. (sub-picture) 0: Non-standard, 1: Standard |
| | D13 | CNOVPN | Vertical sync detection. (sub-picture) 0: exist, 1: No vertical sync |
| | D12 | CVDET60 | Vertical frequency detection. (sub-picture) 0: 50 Hz, 1: 60 Hz |
| | D11, D10 | BCF [1:0] | System mode detection. (sub-picture) 00: N-PAL, 01: M-PAL, 10: M-NTSC, 11: BG-PAL/4.43NTSC |
| | D9 | PVMD525 | Vertical sync frequency standard/non-standard detection. (main-picture) 0: Non-standard, 1: Standard |
| | D8 | PNOVPN | Vertical sync detection. (main-picture) 0: exist, 1: No vertical sync |
| | D7 | PVDET60 | Vertical frequency detection. (main-picture) 0: 50 Hz, 1: 60 Hz |
| | D6 | CKIL | Color Killer detection. (sub-picture) 0: Killer-off, 1: Killer-on |
| | D5 | PDUNLOCK | H-PLL condition. (sub-picture) 0: Lock, 1: Un-lock |
| | D4 | PALDET | PAL signal detection. 0: NTSC or No-color, 1: PAL |

CCD Data Slicer Supplementary Explanation

| SLVFIX | SELFLOOP | FLDSEL | Slice Level Control Circuit | Detected Slice Level Feedback | Motion Field at Auto Slice |
|--------|----------|--------|--|-------------------------------|----------------------------|
| 1 | 0 | — | ON | ON | 1st and 2nd field |
| | | | Auto slice function works both field. (CCD details sliced at suitable level) | | |
| 1 | 1 | — | ON | OFF | 1st and 2nd field |
| | | | Slice level is detecting from value of SSLV resistor, and sliced the most suitable value. (Detected slice level is not feedback at the next field) | | |
| 0 | 1 | — | ON | OFF | — |
| | | | Slice level is fixed value of SSLV resistor. | | |
| 0 | 0 | 0 | ON | ON | 2nd field (CFIELD = 0) |
| | | | Renewed slice level reading value of SLV resistor only 2nd field. | | |
| | | 1 | ON | ON | 1st field (CFIELD = 1) |
| | | | Renewed slice level reading value of SLV resistor only 1st field. | | |

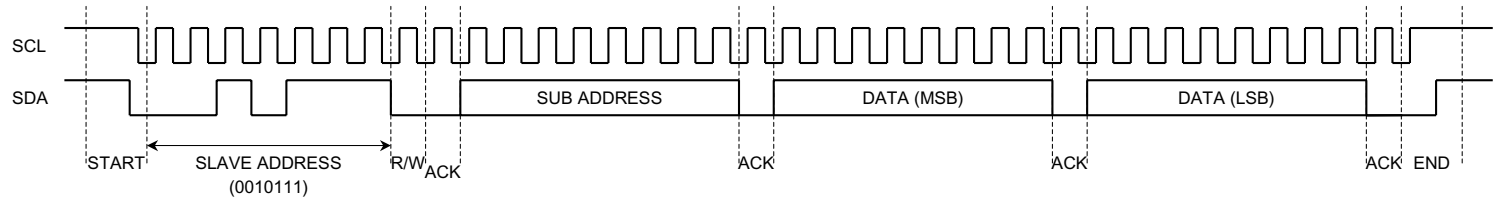
Outline of I²C BUS Control Format

Sub-pictures range in the main-picture. (horizontal width)

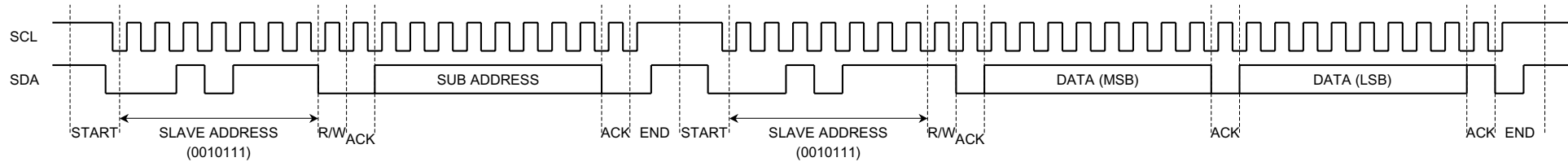
Slave Address

| | | | | | | | |
|----|----|----|----|----|----|----|-----|
| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1/0 |

Write Format



Read Format

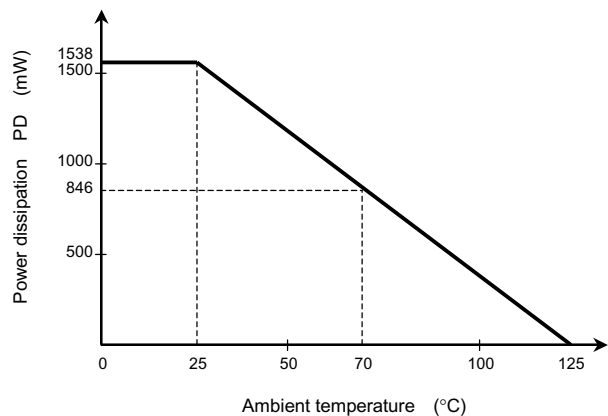


Purchase of TOSHIBA I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

Maximum Ratings (V_{SS} = 0 V, Ta = 25°C)

| Characteristics | Symbol | Rating | Unit |
|---------------------|------------------|--|------|
| Supply voltage | V _{DD} | V _{SS} to V _{SS} + 4.5 | V |
| Applied voltage | V _{IN} | −0.3 to V _{DD} + 0.3 | V |
| Applied current | I _{IN} | ±10 | mA |
| Power dissipation | PD | 1538 | mW |
| Storage temperature | T _{STG} | −55 to 125 | °C |

TD-PD (on board mounting)



Recommended Operating Conditions

| Characteristics | Symbol | Rating | Unit |
|---------------------|------------------|----------------------|------|
| Supply voltage | V _{DD} | 3.0 to 3.6 | V |
| Input voltage | V _{IN} | 0 to V _{DD} | V |
| Output voltage | V _{OUT} | 0 to V _{DD} | V |
| Ambient temperature | T _{OPR} | −10 to 70 | °C |

Electrical Characteristics

DC Characteristics

Digital Part Operating Condition: $V_{DD} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$

| Characteristics | | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit | Applicable Terminals |
|-------------------------|-----------------------|-----------|--------------|----------------|---------------------|------|----------|---------------|----------------------|
| Consumption current | | I_{DD} | — | — | — | 160 | 230 | mA | — |
| High input voltage | CMOS input | V_{IH1} | — | — | $V_{DD} \times 0.8$ | — | V_{DD} | V | (Note1) |
| | Schmitt trigger input | V_{IH2} | — | — | $V_{DD} \times 0.8$ | — | V_{DD} | V | (Note2) |
| Low level input voltage | CMOS input | V_{IL1} | — | — | — | — | 0.8 | V | (Note1) |
| | Schmitt trigger input | V_{IL2} | — | — | — | — | 0.8 | V | (Note2) |
| Input current | High level | I_{IH} | — | — | -10 | — | +10 | μA | (Note1) (Note2) |
| | Low level | I_{IL} | — | — | -10 | — | +10 | μA | (Note1) (Note2) |
| Output voltage | High level | V_{OH} | — | — | 2.4 | — | — | V | (Note3) |
| | Low level | V_{OL} | — | — | — | — | 0.4 | V | (Note3) |

Note1: CKC, CKCSEL, TEST, SDA, PIPEN, CKPSEL, CKP, TESTM0, TESTM1, TESTM2, TEST2

Note2: RESET, SCL, PVD, PHD

Note3: CLMP, CSTD, PFIELD, CFIELD, CVREF, CHREF, CKILL, VCHIP, Ys, PHREF

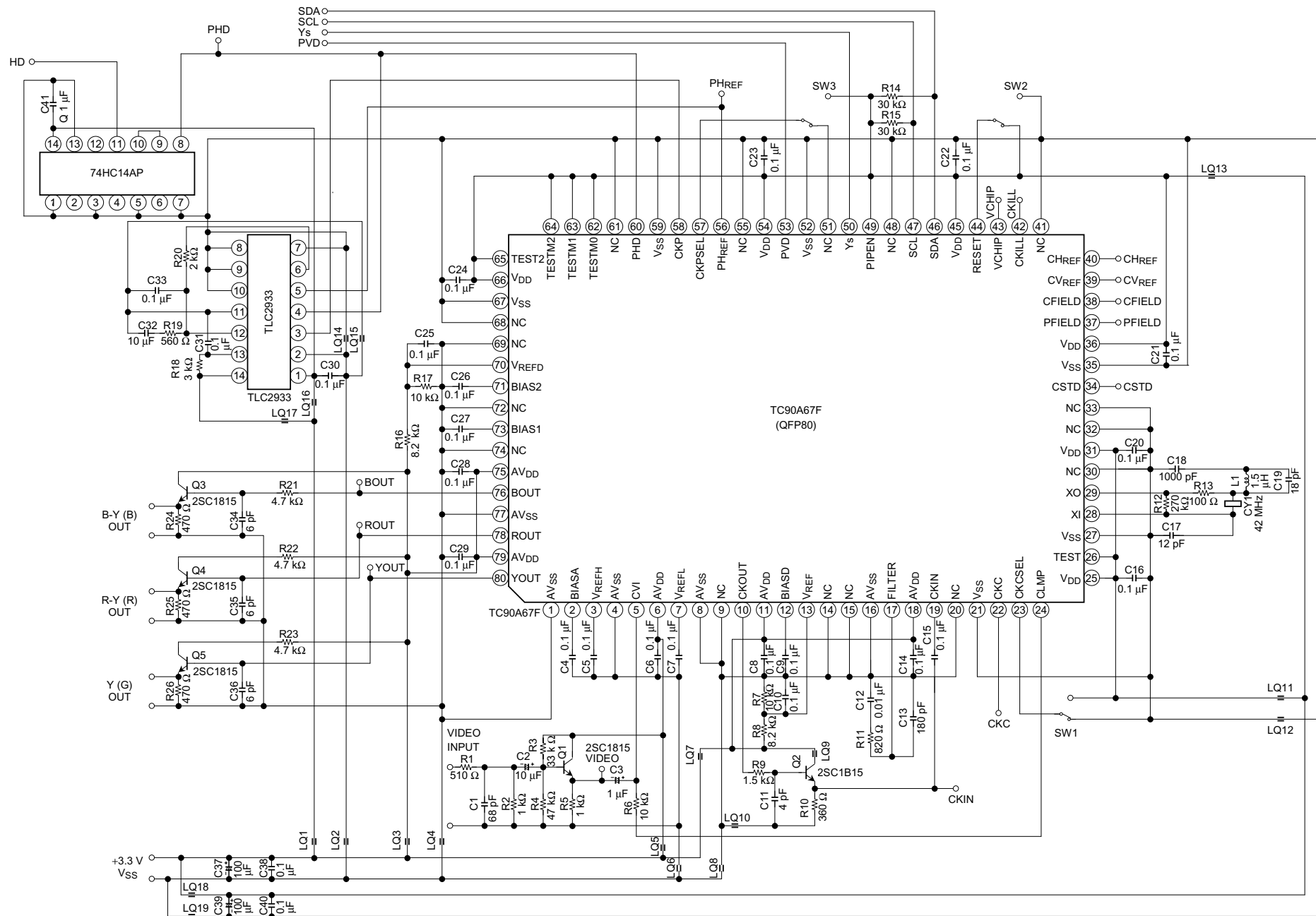
ADC Characteristics Operating Condition: $V_{DD} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$

| Characteristics | | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit | Applicable Terminals |
|-----------------|-------------------------------|------------|--------------|--------------------------|-----|------|---------|-----------|----------------------|
| A/D converter | Resolution | R_{S1} | — | — | — | — | 8 | bit | — |
| | Input level | ADIN | — | $AV_{DD} = 3.3\text{ V}$ | — | 1.32 | — | V_{p-p} | CVI |
| | Pin voltage | BIASA | — | — | — | 0.9 | — | V | BIASA |
| | | V_{REFH} | — | — | — | 2.3 | — | V | V_{REFH} |
| | | V_{REFL} | — | — | — | 1.0 | — | V | V_{REFL} |
| | Non-linear error | ILE1 | — | (8 bit precision) | — | — | ± 3 | LSB | — |
| | Differential non-linear error | DLE1 | — | (8 bit precision) | — | — | ± 2 | LSB | — |
| | DG | DG | — | — | 0 | — | 6.5 | % | — |
| | DP | DP | — | — | 0 | — | 4.0 | deg | — |

DAC, VCO Characteristics Operating Condition: $V_{DD} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$

| Characteristics | | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit | Applicable Terminals |
|-----------------------|-------------------------------|------------|--------------|-----------------------|------|------|---------|-----------|----------------------|
| D/A converter (VIDEO) | Resolution | R_{S2} | — | — | — | — | 8 | bit | — |
| | Output level | YOUT | — | $(V_{DD} - V_{REFD})$ | — | — | 1.5 | V_{p-p} | YOUT |
| | | ROUT | — | $(V_{DD} - V_{REFD})$ | — | — | 1.5 | V_{p-p} | ROUT |
| | | BOUT | — | $(V_{DD} - V_{REFD})$ | — | — | 1.5 | V_{p-p} | BOUT |
| | Non-linear error | ILE2 | — | (8 bit precision) | — | — | ± 1 | LSB | — |
| | Differential non-linear error | DLE2 | — | (8 bit precision) | — | — | ± 1 | LSB | — |
| | Pin voltage | BIAS1 | — | — | 0.8 | 1.0 | 1.4 | V | BIAS1 |
| | | BIAS2 | — | — | 1.8 | 2.0 | 2.2 | V | BIAS2 |
| | Reference voltage level | V_{REFD} | — | — | 1.8 | — | — | V | V_{REFD} |
| | Output impedance | ZOUT1 | — | — | — | 200 | — | Ω | YOUT, ROUT, BOUT |
| D/A converter (CLOCK) | Resolution | R_{SD2} | — | — | — | — | 6 | bit | — |
| | Output level | CKOUT | — | $(V_{DD} - V_{REF})$ | — | — | 2.0 | V_{p-p} | CKOUT |
| | Non-linear error | ILE3 | — | (6 bit precision) | — | — | ± 3 | LSB | — |
| | Differential non-linear error | DLE3 | — | (6 bit precision) | — | — | ± 2 | LSB | — |
| | Pin voltage | BIASD | — | — | 0.8 | 1.0 | 1.4 | V | BIASD |
| | Reference voltage level | V_{REF} | — | — | 1.3 | — | — | V | V_{REF} |
| | Output impedance | ZOUT2 | — | — | — | 200 | — | Ω | CKOUT |
| VCO | Pull-in frequency | FCK1 | — | — | 5.4 | 6.0 | 6.6 | MHz | — |
| | Input amplitude | VCK | — | — | 1.0 | 2.0 | — | V | CKIN |
| | Pull-in oscillation frequency | FCK2 | — | — | 21.6 | 24.0 | 26.4 | MHz | — |
| | FILTER terminal voltage | FILTER | — | — | 0.8 | — | 2.7 | V | FILTER |

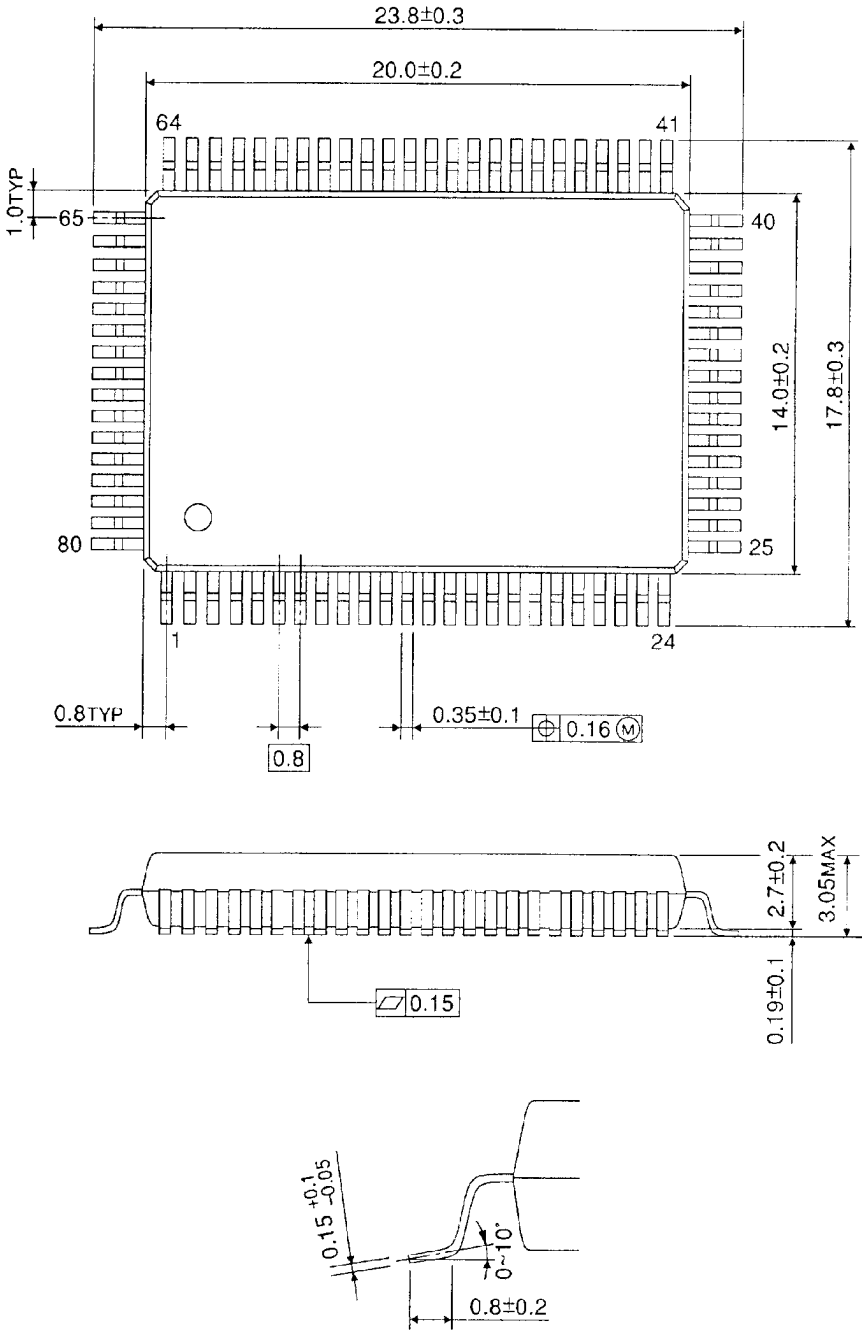
Application Circuit



Package Dimensions

QFP80-P-1420-0.80B

Unit : mm



Weight: 1.6 g (typ.)