

Radiation Hardened, SEGR Resistant N-Channel Power MOSFET



Intersil StarPower Rad Hard MOSFETs have been specifically developed for high performance applications in a commercial or military space environment.

StarPower MOSFETs offer the system designer both extremely low $r_{DS(ON)}$ and Gate Charge allowing the development of low loss Power Subsystems. StarPower Gold FETs combine this electrical capability with total dose radiation hardness up to 100K RADs while maintaining the guaranteed performance for Single Event Effects (SEE) which the Intersil FS families have always featured.

The Intersil family of StarPower FETs includes a series of devices in various voltage, current and package styles. The portfolio consists of StarPower and StarPower Gold products. StarPower FETs are optimized for total dose and $r_{DS(ON)}$ while exhibiting SEE capability at full rated voltage up to an LET of 37. StarPower Gold FETs have been optimized for SEE and Gate Charge combining SEE performance to 80% of the rated voltage for an LET of 82 with extremely low gate charge characteristics.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specifically designed and processed to be radiation tolerant. The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, power distribution, motor drives and relay drivers as well as other power control and conditioning applications. As with conventional MOSFETs these Radiation Hardened MOSFETs offer ease of voltage control, fast switching speeds and ability to parallel switching devices.

Reliability screening is available as either TXV or Space equivalent of MIL-PRF-19500.

Formerly available as type TA45233W.

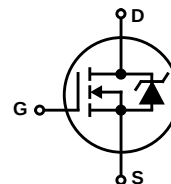
Ordering Information

RAD LEVEL	SCREENING LEVEL	PART NUMBER/BRAND
10K	Engineering samples	FSGJ264D1
100K	TXV	FSGJ264R3
100K	Space	FSGJ264R4

Features

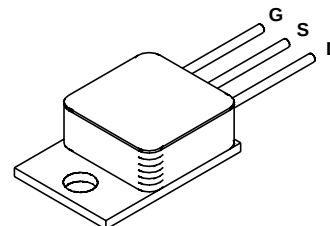
- 42A, 250V, $r_{DS(ON)} = 0.049\Omega$
- UIS Rated
- Total Dose
 - Meets Pre-RAD Specifications to 100K RAD (Si)
- Single Event
 - Safe Operating Area Curve for Single Event Effects
 - SEE Immunity for LET of 82MeV/mg/cm² with V_{DS} up to 80% of Rated Breakdown and V_{GS} of 5V Off-Bias
- Dose Rate
 - Typically Survives 3E9 RAD (Si)/s at 80% BV_{DSS}
 - Typically Survives 2E12 if Current Limited to I_{AS}
- Photo Current
 - 21nA Per-RAD (Si)/s Typically
- Neutron
 - Maintain Pre-RAD Specifications for 1E13 Neutrons/cm²
 - Usable to 1E14 Neutrons/cm²

Symbol



Packaging

TO-254AA



CAUTION: Beryllia Warning per MIL-PRF-19500 refer to package specifications.

Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

	FSGJ264R	UNITS
Drain to Source Voltage V_{DS}	250	V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) V_{DGR}	250	V
Continuous Drain Current		
$T_C = 25^{\circ}\text{C}$ I_D	42	A
$T_C = 100^{\circ}\text{C}$ I_D	27	A
Pulsed Drain Current I_{DM}	160	A
Gate to Source Voltage V_{GS}	± 30	V
Maximum Power Dissipation		
$T_C = 25^{\circ}\text{C}$ P_T	192	W
$T_C = 100^{\circ}\text{C}$ P_T	77	W
Linear Derating Factor	1.54	W/ $^{\circ}\text{C}$
Single Pulsed Avalanche Current, $L = 100\mu\text{H}$, (See Test Figure) I_{AS}	85	A
Continuous Source Current (Body Diode) I_S	42	A
Pulsed Source Current (Body Diode) I_{SM}	160	A
Operating and Storage Temperature T_J, T_{STG}	-55 to 150	$^{\circ}\text{C}$
Lead Temperature (During Soldering) T_L (Distance $>0.063\text{in}$ (1.6mm) from Case, 10s Max)	300	$^{\circ}\text{C}$
Weight (Typical)	9.3 (Typical)	g

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 1\text{mA}$, $V_{GS} = 0\text{V}$	250	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 1\text{mA}$	$T_C = -55^{\circ}\text{C}$	-	5.5	V
			$T_C = 25^{\circ}\text{C}$	2.0	4.5	V
			$T_C = 125^{\circ}\text{C}$	1.0	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 200\text{V}$, $V_{GS} = 0\text{V}$	$T_C = 25^{\circ}\text{C}$	-	25	μA
			$T_C = 125^{\circ}\text{C}$	-	250	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 30\text{V}$	$T_C = 25^{\circ}\text{C}$	-	100	nA
			$T_C = 125^{\circ}\text{C}$	-	200	nA
Drain to Source On-State Voltage	$V_{DS(ON)}$	$V_{GS} = 12\text{V}$, $I_D = 42\text{A}$	-	-	2.18	V
Drain to Source On Resistance	$r_{DS(ON)12}$	$I_D = 27\text{A}$, $V_{GS} = 12\text{V}$	$T_C = 25^{\circ}\text{C}$	-	0.041	Ω
			$T_C = 125^{\circ}\text{C}$	-	0.096	Ω
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 125\text{V}$, $I_D = 42\text{A}$, $R_L = 3.0\Omega$, $V_{GS} = 12\text{V}$, $R_{GS} = 2.35\Omega$	-	-	35	ns
Rise Time	t_r		-	-	70	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	-	70	ns
Fall Time	t_f		-	-	15	ns
Total Gate Charge	$Q_{g(12)}$	$V_{GS} = 0\text{V}$ to 12V	$V_{DD} = 125\text{V}$, $I_D = 42\text{A}$	-	100	nC
Gate Charge Source	Q_{gs}			-	35	nC
Gate Charge Drain	Q_{gd}			-	35	nC
Gate Charge at 20V	$Q_{g(20)}$	$V_{GS} = 0\text{V}$ to 20V		-	160	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0\text{V}$ to 2V		-	12	nC
Plateau Voltage	$V_{(PLATEAU)}$	$I_D = 42\text{A}$, $V_{DS} = 15\text{V}$	-	7.5	-	V
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	-	5600	-	pF
Output Capacitance	C_{OSS}		-	875	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	35	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	0.65	$^{\circ}\text{C/W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 42A$	-	-	1.2	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 42A, dI_{SD}/dt = 100A/\mu s$	-	-	590	ns
Reverse Recovery Charge	Q_{RR}		-	6.8	-	μC

Electrical Specifications up to 100K RAD $T_C = 25^\circ C$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Drain to Source Breakdown Volts (Note 3)	BV _{DSS}	V _{GS} = 0, I _D = 1mA	250	-	V
Gate to Source Threshold Volts (Note 3)	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 1mA	2.0	4.5	V
Gate to Body Leakage (Notes 2, 3)	I _{GSS}	V _{GS} = ±30V, V _{DS} = 0V	-	100	nA
Zero Gate Leakage (Note 3)	I _{DSS}	V _{GS} = 0, V _{DS} = 200V	-	25	μA
Drain to Source On-State Volts (Notes 1, 3)	V _{DS(ON)}	V _{GS} = 12V, I _D = 42A	-	2.18	V
Drain to Source On Resistance (Notes 1, 3)	r _{DS(ON)12}	V _{GS} = 12V, I _D = 27A	-	0.049	Ω

NOTES:

1. Pulse test, 300 μs Max.
2. Absolute value.
3. Insitu Gamma bias must be sampled for both $V_{GS} = 12V, V_{DS} = 0V$ and $V_{GS} = 0V, V_{DS} = 80\% BV_{DSS}$.

Single Event Effects (SEB, SEGR) Note 4

TEST	SYMBOL	ENVIRONMENT (NOTE 5)			APPLIED V_{GS} BIAS (V)	(NOTE 6) MAXIMUM V_{DS} BIAS (V)
		ION SPECIES	TYPICAL LET (MeV/mg/cm)	TYPICAL RANGE (μ)		
Single Event Effects Safe Operating Area	SEESOAS	Br	37	36	-20	250
		I	60	32	-10	250
		Au	82	28	-5	200
		Au	82	28	-10	150

NOTES:

4. Testing conducted at Brookhaven National Labs.
5. Fluence = 1E5 ions/cm² (Typical), $T = 25^\circ C$.
6. Does not exhibit Single Event Burnout (SEB) or Single Event Gate Rupture (SEGR).

Performance Curves Unless Otherwise Specified

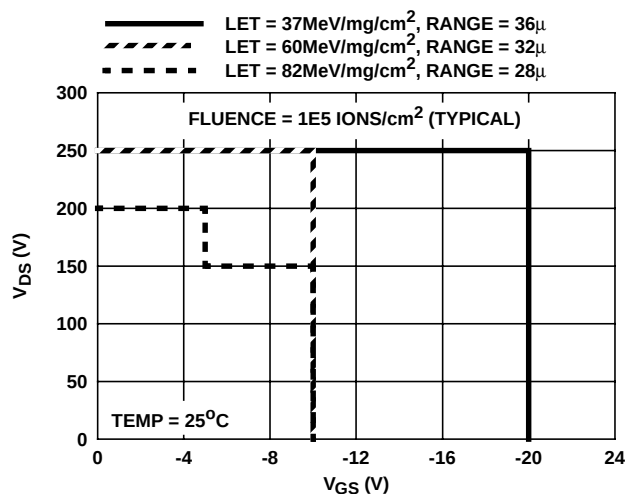


FIGURE 1. SINGLE EVENT EFFECTS SAFE OPERATING AREA

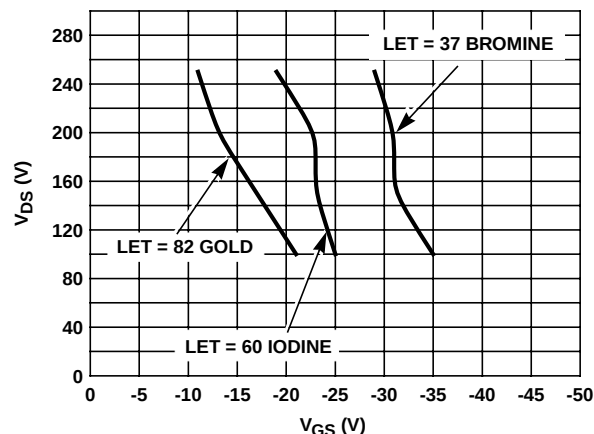


FIGURE 2. TYPICAL SEE SIGNATURE CURVE

Performance Curves Unless Otherwise Specified (Continued)

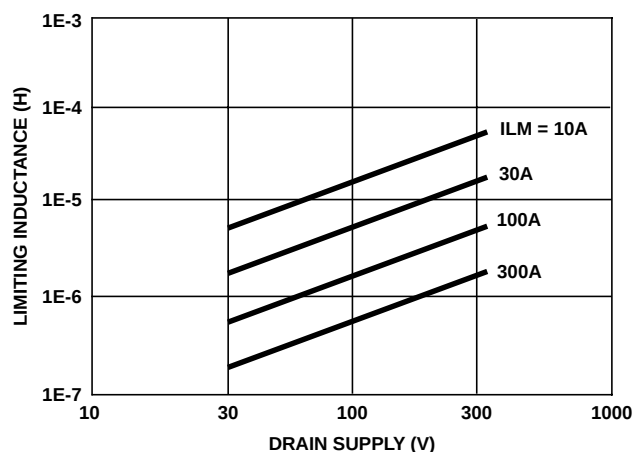


FIGURE 3. TYPICAL DRAIN INDUCTANCE REQUIRED TO LIMIT GAMMA DOT CURRENT TO I_{AS}

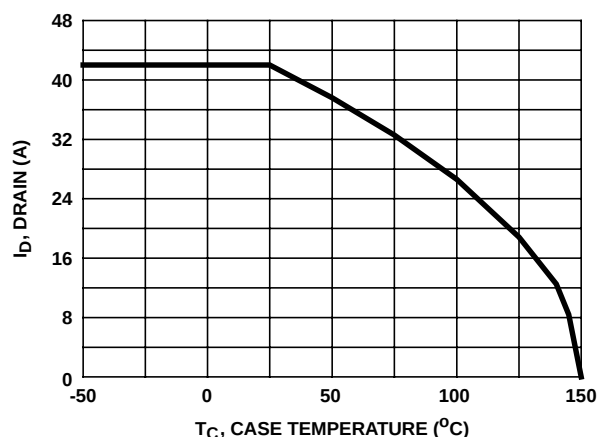


FIGURE 4. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

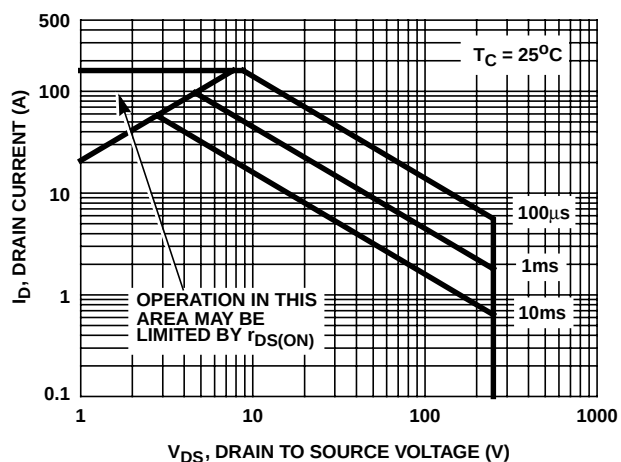


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA

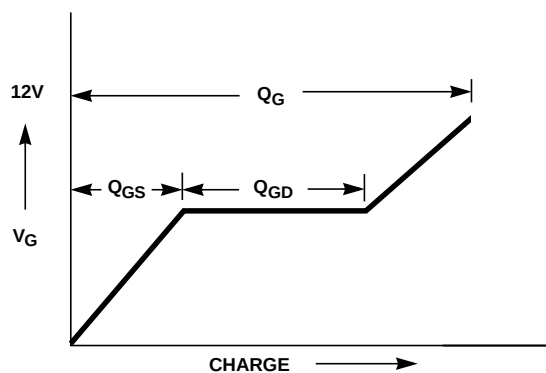


FIGURE 6. BASIC GATE CHARGE WAVEFORM

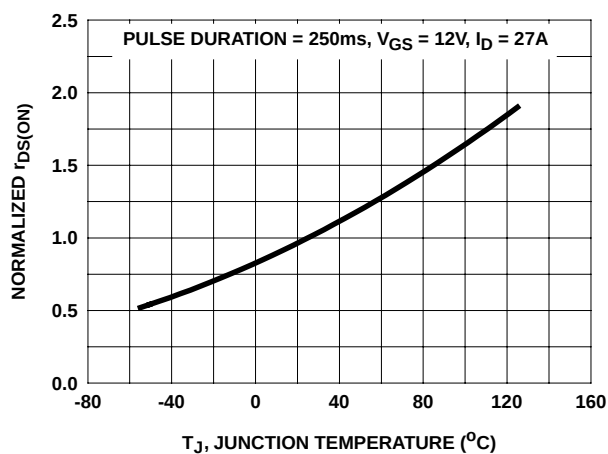


FIGURE 7. TYPICAL NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

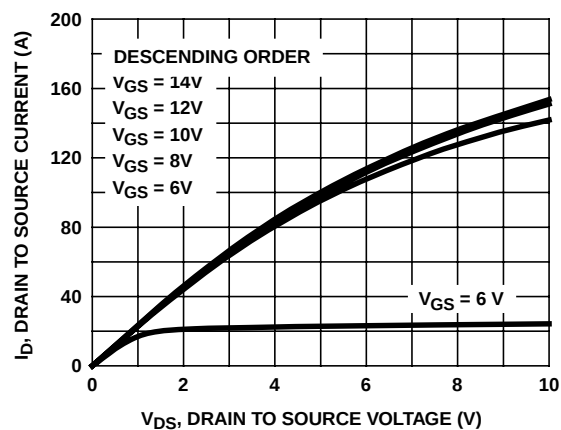


FIGURE 8. TYPICAL OUTPUT CHARACTERISTICS

Performance Curves Unless Otherwise Specified (Continued)

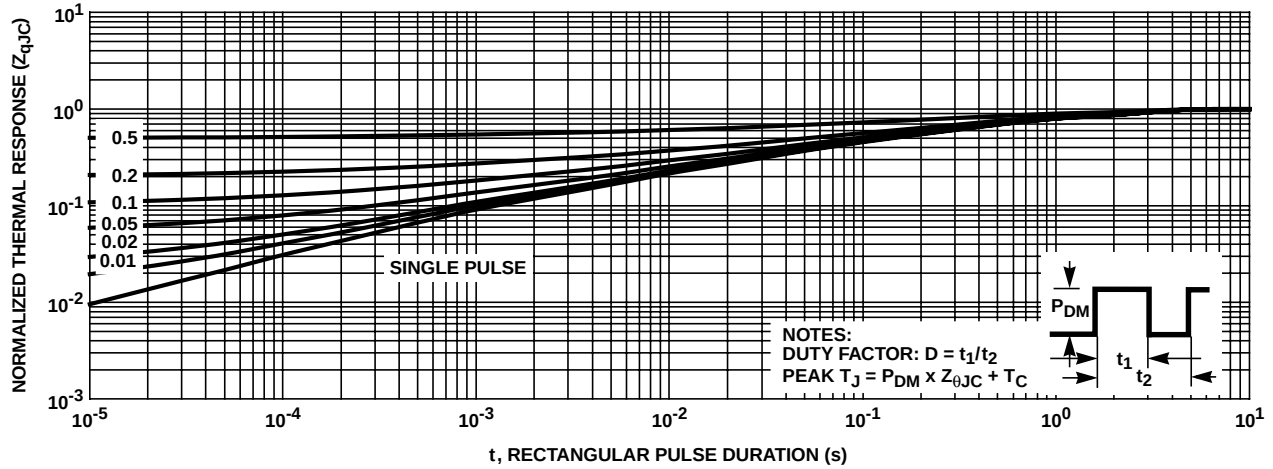


FIGURE 9. NORMALIZED MAXIMUM TRANSIENT THERMAL RESPONSE

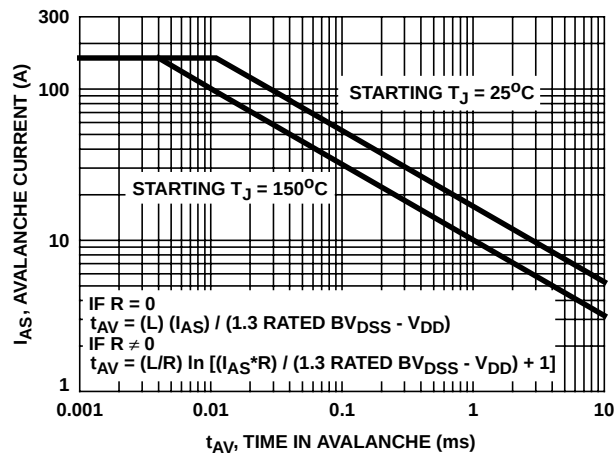


FIGURE 10. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

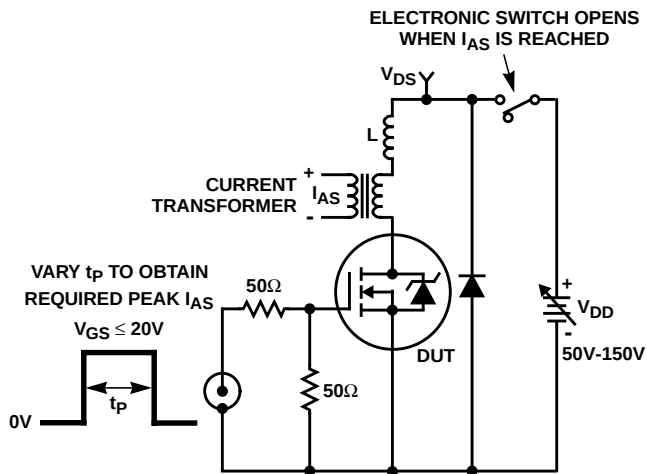


FIGURE 11. UNCLAMPED ENERGY TEST CIRCUIT

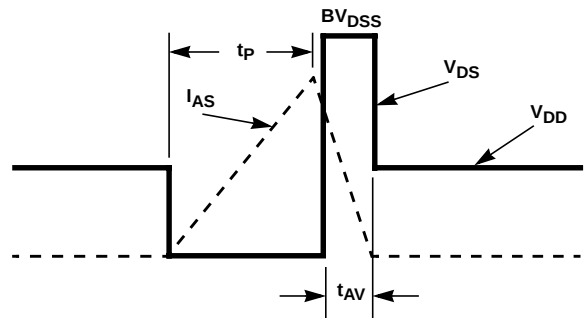


FIGURE 12. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

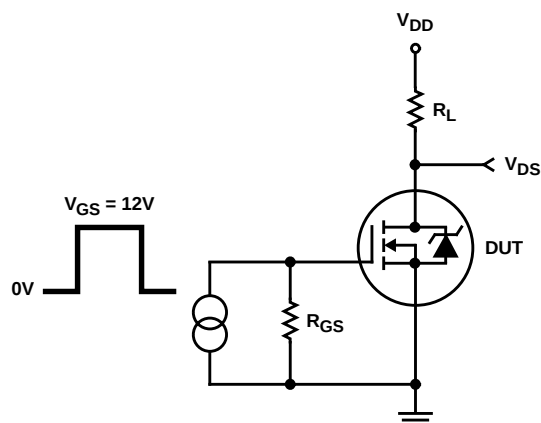


FIGURE 13. RESISTIVE SWITCHING TEST CIRCUIT

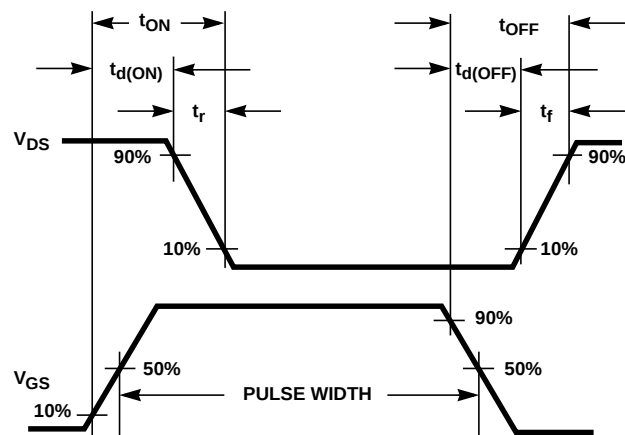


FIGURE 14. RESISTIVE SWITCHING WAVEFORMS

Screening Information

Screening is performed in accordance with the latest revision in effect of MIL-PRF-19500, (Screening Information Table).

Delta Tests and Limits (JANTXV Equivalent, JANS Equivalent) $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 30\text{V}$	± 20 (Note 7)	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\%$ Rated Value	± 25 (Note 7)	μA
Drain to Source On Resistance	$r_{DS(ON)}$	$T_C = 25^\circ\text{C}$ at Rated I_D	$\pm 20\%$ (Note 8)	Ω
Gate Threshold Voltage	$V_{GS(TH)}$	$I_D = 1.0\text{mA}$	$\pm 20\%$ (Note 8)	V

NOTES:

7. Or 100% of Initial Reading (whichever is greater).
8. Of Initial Reading.

Screening Information

TEST	JANTXV EQUIVALENT	JANS EQUIVALENT
Unclamped Inductive Switching	$V_{GS(PEAK)} = 20\text{V}$, $L = 0.1\text{mH}$; Limit = 85A	$V_{GS(PEAK)} = 20\text{V}$, $L = 0.1\text{mH}$; Limit = 85A
Thermal Response	$t_H = 100\text{ms}$; $V_H = 25\text{V}$; $I_H = 4\text{A}$; LIMIT = 100mV	$t_H = 100\text{ms}$; $V_H = 25\text{V}$; $I_H = 4\text{A}$; LIMIT = 100mV
Gate Stress	$V_{GS} = 45\text{V}$, $t = 250\mu\text{s}$	$V_{GS} = 45\text{V}$, $t = 250\mu\text{s}$
Pind	Optional	Required
Pre Burn-In Tests (Note 9)	MIL-PRF-19500 Group A, Subgroup 2 (All Static Tests at 25°C)	MIL-PRF-19500 Group A, Subgroup 2 (All Static Tests at 25°C)
Steady State Gate Bias (Gate Stress)	MIL-PRF-750, Method 1042, Condition B $V_{GS} = 80\%$ of Rated Value, $T_A = 150^\circ\text{C}$, Time = 48 hours	MIL-PRF-750, Method 1042, Condition B $V_{GS} = 80\%$ of Rated Value, $T_A = 150^\circ\text{C}$, Time = 48 hours
Interim Electrical Tests (Note 9)	All Delta Parameters Listed in the Delta Tests and Limits Table	All Delta Parameters Listed in the Delta Tests and Limits Table
Steady State Reverse Bias (Drain Stress)	MIL-PRF-750, Method 1042, Condition A $V_{DS} = 80\%$ of Rated Value, $T_A = 150^\circ\text{C}$, Time = 160 hours	MIL-PRF-750, Method 1042, Condition A $V_{DS} = 80\%$ of Rated Value, $T_A = 150^\circ\text{C}$, Time = 240 hours
PDA	10%	5%
Final Electrical Tests (Note 9)	MIL-PRF-19500, Group A, Subgroup 2	MIL-PRF-19500, Group A, Subgroups 2 and 3

NOTE:

9. Test limits are identical pre and post burn-in.

Additional Tests

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Safe Operating Area	SOA	$V_{DS} = 200\text{V}$, $t = 10\text{ms}$	0.8	A
Thermal Impedance	ΔV_{SD}	$t_H = 500\text{ms}$; $V_H = 25\text{V}$; $I_H = 4\text{A}$	200	mV

Rad Hard Data Packages - Intersil Power Transistors

TXV Equivalent

1. RAD HARD TXV EQUIVALENT - STANDARD DATA PACKAGE

- A. Certificate of Compliance
- B. Assembly Flow Chart
- C. Preconditioning - Attributes Data Sheet
- D. Group A - Attributes Data Sheet
- E. Group B - Attributes Data Sheet
- F. Group C - Attributes Data Sheet
- G. Group D - Attributes Data Sheet

2. RAD HARD TXV EQUIVALENT - OPTIONAL DATA PACKAGE

- A. Certificate of Compliance
- B. Assembly Flow Chart
- C. Preconditioning - Attributes Data Sheet
 - Pre and Post Burn-In Read and Record Data
- D. Group A - Attributes Data Sheet
- E. Group B - Attributes Data Sheet
 - Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup B3)
 - Bond Strength Data (Subgroup B3)
 - Pre and Post High Temperature Operating Life Read and Record Data (Subgroup B6)
- F. Group C - Attributes Data Sheet
 - Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup C6)
 - Bond Strength Data (Subgroup C6)
- G. Group D - Attributes Data Sheet
 - Pre and Post RAD Read and Record Data

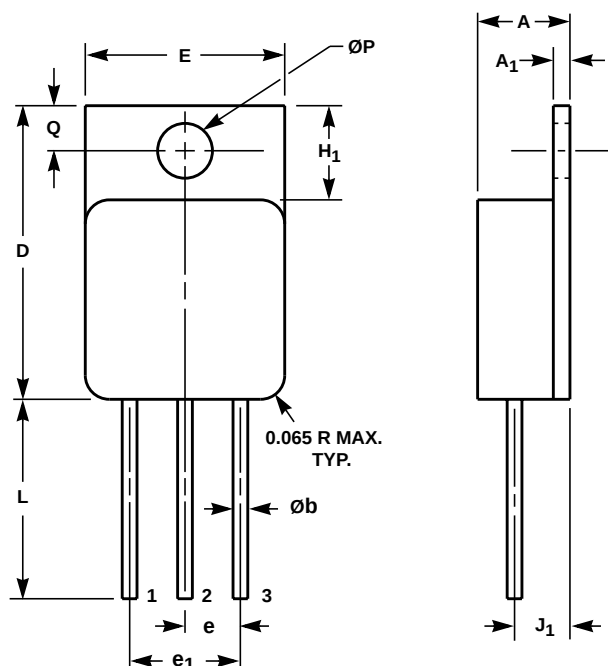
Class S - Equivalents

1. RAD HARD "S" EQUIVALENT - STANDARD DATA PACKAGE

- A. Certificate of Compliance
- B. Serialization Records
- C. Assembly Flow Chart
- D. SEM Photos and Report
- E. Preconditioning - Attributes Data Sheet
 - HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data
 - HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data
- F. Group A - Attributes Data Sheet
- G. Group B - Attributes Data Sheet
- H. Group C - Attributes Data Sheet
- I. Group D - Attributes Data Sheet

2. RAD HARD MAX. "S" EQUIVALENT - OPTIONAL DATA PACKAGE

- A. Certificate of Compliance
- B. Serialization Records
- C. Assembly Flow Chart
- D. SEM Photos and Report
- E. Preconditioning - Attributes Data Sheet
 - HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data
 - HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data
 - X-Ray and X-Ray Report
- F. Group A - Attributes Data Sheet
 - Subgroups A2, A3, A4, A5 and A7 Data
- G. Group B - Attributes Data Sheet
 - Subgroups B1, B3, B4, B5 and B6 Data
- H. Group C - Attributes Data Sheet
 - Subgroups C1, C2, C3 and C6 Data
- I. Group D - Attributes Data Sheet
 - Pre and Post Radiation Data

TO-254AA**3 LEAD JEDEC TO-254AA HERMETIC METAL PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.249	0.260	6.33	6.60	-
A_1	0.040	0.050	1.02	1.27	-
$\varnothing b$	0.035	0.045	0.89	1.14	2, 3
D	0.790	0.800	20.07	20.32	-
E	0.535	0.545	13.59	13.84	-
e	0.150 TYP		3.81 TYP		4
e_1	0.300 BSC		7.62 BSC		4
H_1	0.245	0.265	6.23	6.73	-
J_1	0.140	0.160	3.56	4.06	4
L	0.520	0.560	13.21	14.22	-
$\varnothing P$	0.139	0.149	3.54	3.78	-
Q	0.110	0.130	2.80	3.30	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC outline TO-254AA dated 11-86.
2. Add typically 0.002 inches (0.05mm) for solder coating.
3. Lead dimension (without solder).
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Die to base BeO isolated, terminals to case ceramic isolated.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

WARNING!**BERYLLIA WARNING PER MIL-PRF-19500**

Packages containing beryllium oxide (BeO) shall not be ground, machined, sandblasted, or subject to any mechanical operation which will produce dust containing any beryllium compound. Packages containing any beryllium compound shall not be subjected to any chemical process (etching, etc.) which will produce fumes containing beryllium or its' compounds.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site **www.intersil.com**

Sales Office Headquarters**NORTH AMERICA**

Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE

Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Intersil Ltd.
8F-2, 96, Sec. 1, Chien-kuo North,
Taipei, Taiwan 104
Republic of China
TEL: 886-2-2515-8508
FAX: 886-2-2515-8369