

FSAT66

Low Voltage Single SPST Normally Open Analog Switch with TTL Compatible Control Input

General Description

The FSAT66 is a high speed single pole/single throw normally open Analog Switch with a TTL compatible control input and is fabricated on a sub-micron CMOS process.

The low On Resistance of the switch allows input to be connected to output with minimal propagation delay and without generating additional ground bounce noise. The device is organized as a 1-bit switch with a switch enable (OE) signal. When OE is HIGH, the switch is on and Port A is connected to Port B. When OE is LOW, the switch is open and a high-impedance state exists between the two ports.

Features

- Space saving SOT23 or SC70 5-lead package
- Ultra small MicroPak™ leadless package
- Broad V_{CC} Operating Range 1.65V to 5.5V
- Rail-to-rail signal handling
- 5Ω switch connection between two ports
- Minimal propagation delay through the switch
- Low I_{CC}
- Zero bounce in flow-through mode
- Control input compatible with TTL input levels
- >250 MHz–3dB bandwidth

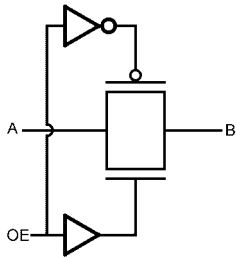
Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
FSAT66M5X (Preliminary)	MA05B	AT66	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3K Units on Tape and Reel
FSAT66P5X	MAA05A	T66	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3K Units on Tape and Reel
FSAT66L6X (Preliminary)	MAC06A	EF	6-Lead MicroPak, 1.0mm Wide	5K Units on Tape and Reel

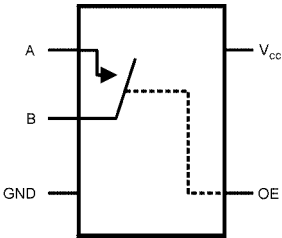
MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

FSAT66 Low Voltage Single SPST Normally Open Analog Switch with TTL Compatible Control Input

Logic Symbol



Analog Symbol



Pin Descriptions

Pin Names	Description
OE	Switch Enable Input
A	Bus A I/O
B	Bus B I/O
NC	No Connect

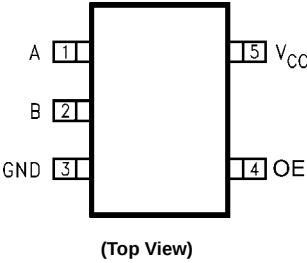
Function Table

OE	B ₀	Function
L	High-Z State	Disconnect
H	A ₀	Connect

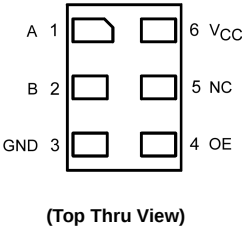
H = HIGH Logic Level
L = LOW Logic Level

Connection Diagrams

Pin Assignments for SOT23 and SC70



Pad Assignments for MicroPak



Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Switch Voltage (V_S)	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage (V_{IN}) (Note 2)	-0.5V to +7.0V
DC Input Diode Current @ (I_{IK}) $V_{IN} < 0V$	-50 mA
DC Output (I_{OUT}) Sink Current	± 128 mA
DC V_{CC} or Ground Current (I_{CC}/I_{GND})	± 100 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
Junction Lead Temperature under Bias (T_J)	+150°C
Junction Lead Temperature (T_L) (Soldering, 10 Seconds)	+260°C
Power Dissipation (P_D) @ +85°C	
SOT23-5	200mW
SC70-5	150 mW
MicroPak-6	200 mW

Recommended Operating Conditions (Note 3)

Power Supply Voltage (V_{CC})	1.65V to 5.5V
Control Input Voltage (V_{IN})	0V to 5.5V
Switch Input Voltage (V_{IN})	0V to V_{CC}
Switch Output Voltage (V_{OUT})	0V to V_{CC}
Input Rise and Fall Time (t_r, t_f)	
Control Input $V_{CC} = 2.3V$ to 3.6V	0 ns/V to 10 ns/V
Control Input $V_{CC} = 4.5V$ to 5.5V	0 ns/V to 5 ns/V
Switch I/O	0 ns/V to DC
Operating Temperature (T_A)	-40°C to +85°C
Thermal Resistance (θ_{JA})	
SOT23-5	300°C/Watt
SC70-5	425°C/Watt
MicroPak-6	325°C/Watt

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = -40°C to +85°C			T _A = +25°C			Units	Conditions
			Min	Typ (Note 4)	Max	Min	Typ	Max		
V _{IH}	HIGH Level Input Voltage	4.5 to 5.5 1.65 to 3.6	2.0 (0.25 V _{CC} + 0.75)						V	
V _{IL}	LOW Level Input Voltage	4.5 to 5.5 1.65 to 3.6	0.8 0.165 V _{CC}						V	
I _{IN}	Control Input Leakage Current	0 to 5.5	±1.0						μA	0 ≤ V _{IN} ≤ 5.5V
I _{OFF}	OFF Leakage Current	1.65 to 5.5	±10.0						μA	0 ≤ A, B ≤ V _{CC}
R _{ON}	Switch On Resistance (Note 5)	4.5	3.0		7.0				Ω	V _{IN} = 0V, I _{IN} = 30 mA
			5.0		12.0					V _{IN} = 2.4V, I _{IN} = 15 mA
			7.0		15.0					V _{IN} = 4.5V, I _{IN} = 30 mA
		3.0	4.0		9.0					V _{IN} = 0V, I _{IN} = 24 mA
			10.0		20.0					V _{IN} = 3V, I _{IN} = 24 mA
			5.0		12.0					V _{IN} = 0V, I _{IN} = 8 mA
		2.3	13.0		30.0					V _{IN} = 2.3V, I _{IN} = 8 mA
			7.0		28.0					V _{IN} = 0V, I _{IN} = 4 mA
			25.0		60.0					V _{IN} = 1.65V, I _{IN} = 4 mA
R _{flat}	On Resistance Flatness (Note 5)(Note 6) (Note 7)	5.0				6.0			Ω	I _A = -30 mA, 0 ≤ V _{Bn} ≤ V _{CC}
		3.3				12.0				I _A = -24 mA, 0 ≤ V _{Bn} ≤ V _{CC}
		2.5				28.0				I _A = -8 mA, 0 ≤ V _{Bn} ≤ V _{CC}
		1.8				125				I _A = -4 mA, 0 ≤ V _{Bn} ≤ V _{CC}
I _{CC}	Quiescent Supply Current	1.65 to 5.5	10.0						μA	V _{IN} = V _{CC} or GND I _{OUT} = 0

Note 4: All typical values are at the specified V_{CC} , and $T_A = 25^\circ C$.

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 6: Parameter is characterized but not tested in production.

Note 7: Flatness is defined as the difference between the minimum and maximum value of On Resistance over the specified range of conditions.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = -40°C to +85°C			Units	Conditions	Figure Number
			Min	Typ (Note 8)	Max			
t _{PHL} , t _{PLH}	Propagation Delay Bus to Bus (Note 9)	1.65 to 1.95		2.0	4.3	ns	V _{IN} = OPEN	Figures 1, 2
		2.3 to 2.7		1.1	2.5			
		3.0 to 3.6		0.7	1.5			
		4.5 to 5.5		0.35	1.0			
t _{PZL} , t _{PZH}	Output Enable Time	1.65 to 1.95	1.5	4.0	12.0	ns	V _{IN} = 2 x V _{CC} for t _{PZL} V _{IN} = 0V for t _{PZH}	Figures 1, 2
		2.3 to 2.7	1.2	2.5	7.0			
		3.0 to 3.6	0.8	2.0	5.5			
		4.5 to 5.5	0.5	1.5	4.5			
t _{PLZ} , t _{PHZ}	Output Disable Time	1.65 to 1.95	2.5	7.5	15.0	ns	V _{IN} = 2 x V _{CC} for t _{PLZ} V _{IN} = 0V for t _{PHZ}	Figures 1, 2
		2.3 to 2.7	2.0	5.5	9.0			
		3.0 to 3.6	1.5	4.5	7.0			
		4.5 to 5.5	1.0	3.5	5.5			
Q	Charge Injection (Note 10)	1.65 to 5.5		0.05		pC	C _L = 0.1 nF, V _{GEN} = 0V, R _{GEN} = 0 Ω, f = 1 MHz	Figure 3
OIRR	Off Isolation (Note 11)	1.65 to 5.5		-50.0		dB	R _L = 50 Ω, C _L = 5 pF, f = 10 MHz	Figure 4
BW	-3dB Bandwidth	1.65 to 5.5		>250		MHz	R _L = 50 Ω	Figure 5
THD	Total Harmonic Distortion (Note 8)	5.0		.011		%	R _L = 600Ω 0.5 V _{p-p} f = 600 Hz to 20 KHz	

Note 8: All typical values are at the specified V_{CC}, and T_A = 25°C.

Note 9: This parameter is guaranteed by design but is not tested. The switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

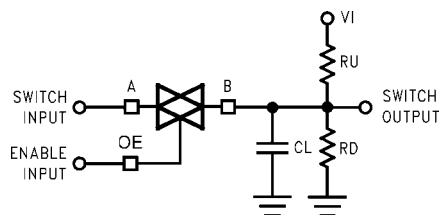
Note 10: Guaranteed by design.

Note 11: Off Isolation = 20 log₁₀ [V_A/V_{BN}]

Capacitance

Symbol	Parameter	Typ	Max	Units	Conditions
C _{IN}	Control Pin Input Capacitance	2.0		pF	V _{CC} = 0V
C _{I/O OFF}	Input/Output Capacitance	6.0		pF	V _{CC} = 5.0V, OE = 0.0V
C _{I/O ON}	Input/Output Capacitance	12.0		pF	V _{CC} = 5.0V, OE = V _{CC}

AC Loading and Waveforms



Input driven by 50Ω source terminated in 50Ω
 C_L includes load and stray capacitance.
 Input PRR = 1.0 MHz; $t_w = 500$ ns

FIGURE 1. AC Test Circuit

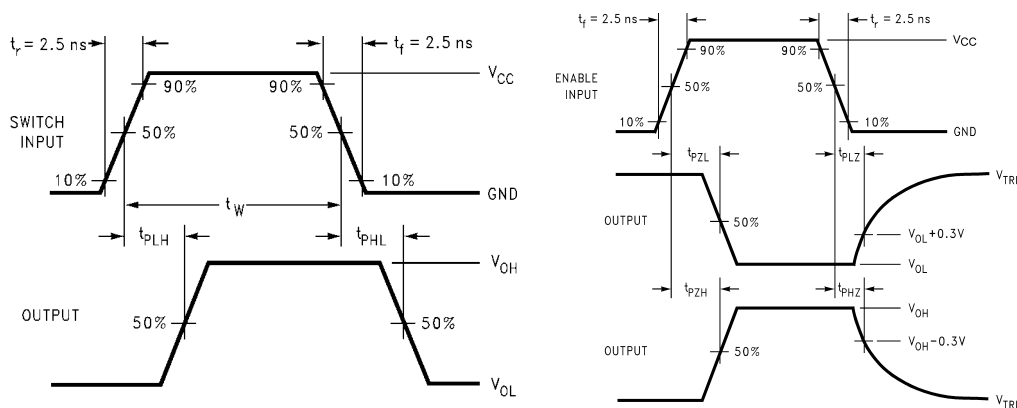


FIGURE 2. AC Waveforms

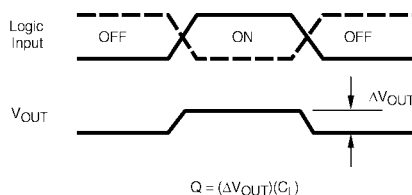
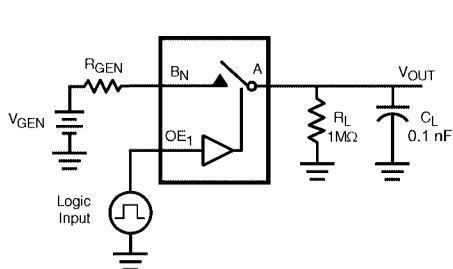


FIGURE 3. Charge Injection Test

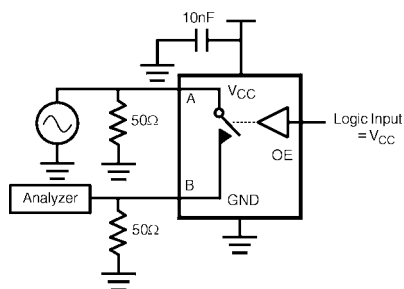


FIGURE 4. Off Isolation

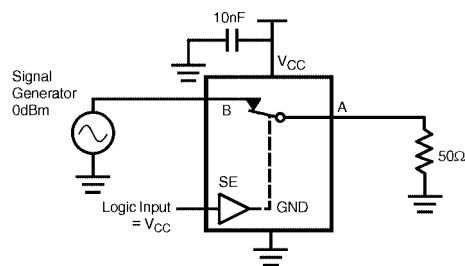


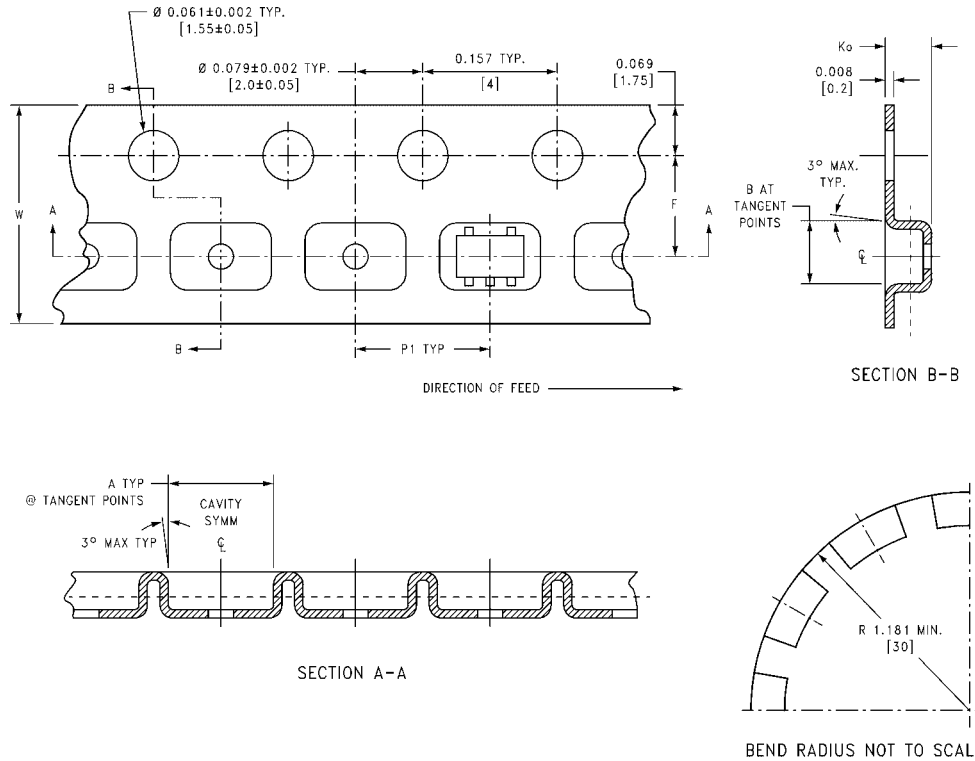
FIGURE 5. Crosstalk

Tape and Reel Specification

TAPE FORMAT FOR SOT23, SC70

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
M5X, P5X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)

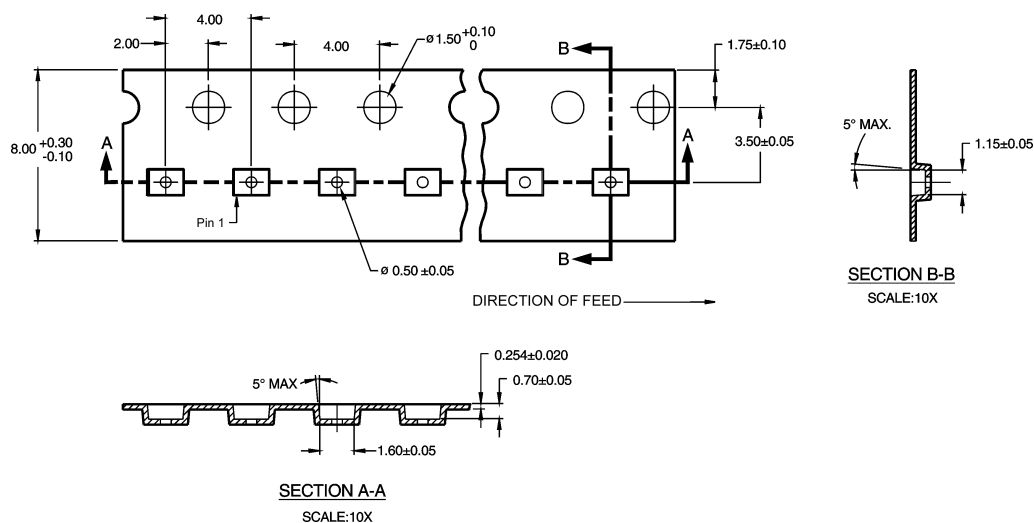


Package	Tape Size	DIM A	DIM B	DIM F	DIM K ₀	DIM P1	DIM W
SC70-5	8 mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)
SOT23-5	8 mm	0.130 (3.3)	0.130 (3.3)	0.138 ± 0.002 (3.5 ± 0.05)	0.055 ± 0.004 (1.4 ± 0.11)	0.157 (4)	0.315 ± 0.012 (8 ± 0.3)

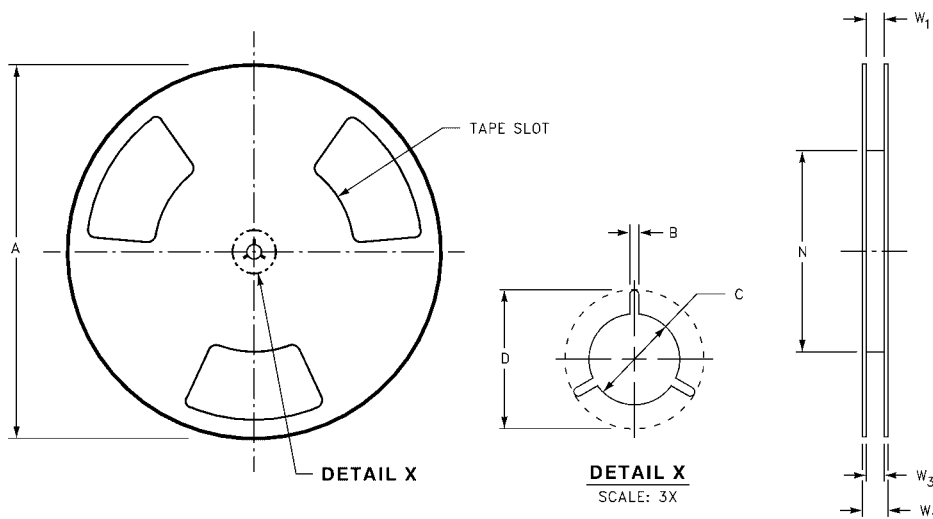
Tape and Reel Specification (Continued)

TAPE FORMAT FOR MicroPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

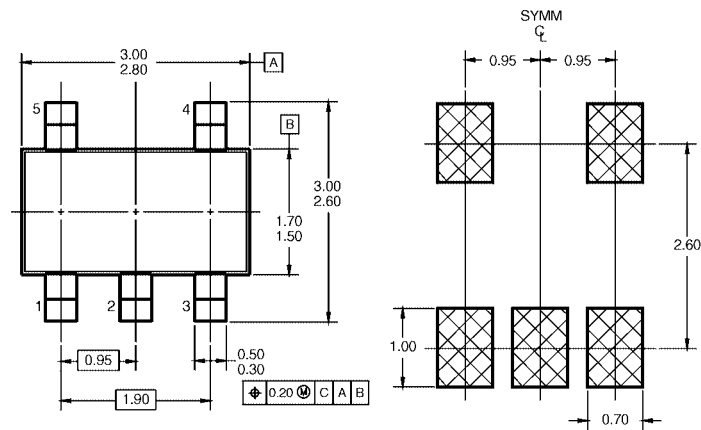


REEL DIMENSIONS inches (millimeters)

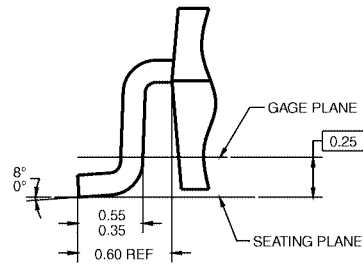
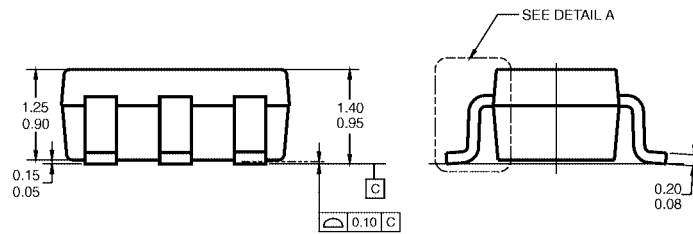


Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/-0.000 (8.40 + 1.50/-0.00)	0.567 (14.40)	W1 + 0.078/-0.039 (W1 + 2.00/-1.00)

Physical Dimensions inches (millimeters) unless otherwise noted



LAND PATTERN RECOMMENDATION



DETAIL A

- NOTES: UNLESS OTHERWISE SPECIFIED
 A) THIS PACKAGE CONFORMS TO JEDEC MO-178, ISSUE B, VARIATION AA, DATED JANUARY 1999.
 B) ALL DIMENSIONS ARE IN MILLIMETERS.

MA05BRevC

5-Lead SOT23, JEDEC MO-178, 1.6mm
 Package Number MA05B

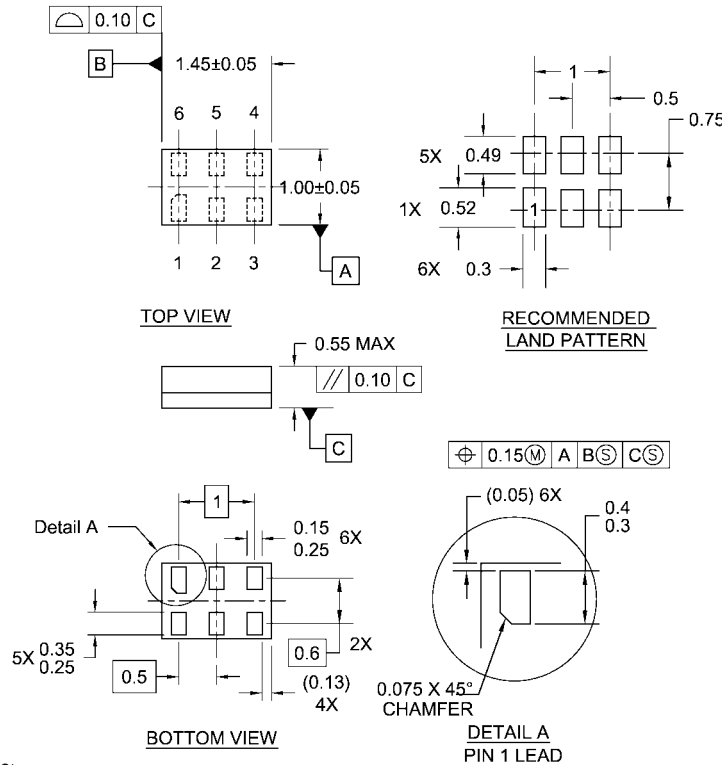


- A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88A.
B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
C. DIMENSIONS ARE IN MILLIMETERS.

MAA05ARevC

**5-Lead SC70, EIAJ SC-88a, 1.25mm Wide
Package Number MAA05A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

**6-Lead MicroPak, 1.0mm Wide
Package Number MAC06A**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com