Integrated Circuit Systems, Inc.

ICS9217
Preliminary Product Preview

667MHz Direct Rambus™ Clock Generator II

General Description

The **ICS9217** is a high-speed clock generator providing a differential clock source up to 667 MHz for a 2nd generation Direct RambusTM memory system. It includes signals to synchronize the Direct RambusTM Channel clock to an external system clock.

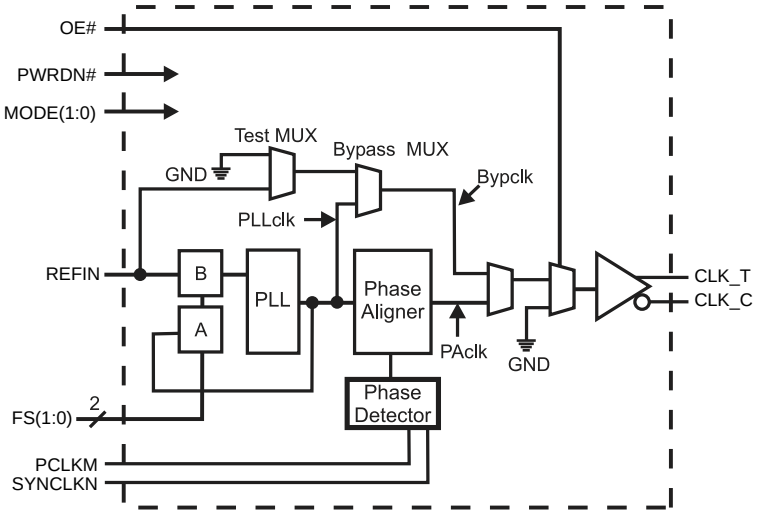
The **ICS9217** provides two power management mechanisms. A “Clock Stop” mode is controlled by the OE# pin. When OE# is asserted, the internal clock circuitry remains running, but the CLK_T/CLK_C output buffers are disabled. A “Power Down” mode, controlled by the PWRDN# pin turns off the internal circuitry and drives both clock outputs to ground. The internal resistor divider networks are also disconnected to further reduce power consumption.

The **ICS9217** is Spread Spectrum compatible.

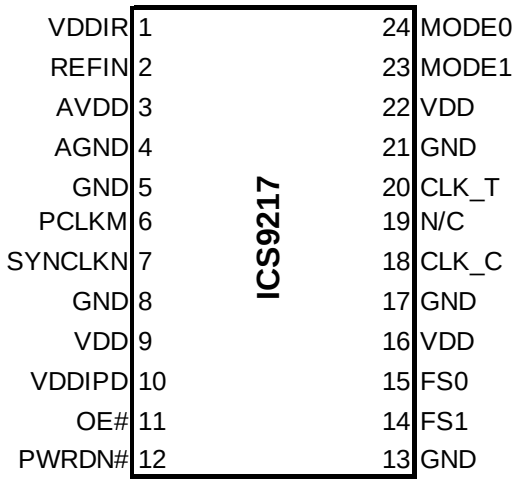
Features

- Up to 667 MHz differential clock source for 2nd generation Direct Rambus™ system
- Supports 4, 6, 8, and 16/3 frequency multipliers
- Cycle–to–cycle jitter less than +/- 20 ps
- Supports both systems needing to synchronize Rambus™ channel clocks to system clocks and system that do not require such synchronization
- Power management features
- Space saving 24-pin SSOP package
- Flexible input voltage levels

Block Diagram



Pin Configuration



24-Pin SSOP

Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	VDDIR	PWR	Reference supply for REFIN input
2	REFIN	IN	Reference Clock input
3	AVDD	PWR	3.3V Analog Power pin for Core PLL
4	AGND	PWR	Analog Ground pin for Core PLL
5	GND	PWR	Ground pin.
6	PCLKM	IN	Phase detector input
7	SYNCLKN	IN	Phase detector input
8	GND	PWR	Ground pin.
9	VDD	PWR	Power supply, nominal 3.3V
10	VDDIPD	PWR	Reference supply for PCLKM, SYNCLKN, OE#, MODE(0:1)
11	OE#	IN	Active low input for enabling outputs. 1 = tri-state outputs, 0 = enable outputs
12	PWRDN#	IN	Active-low input pin used to place the device into a low power state. The VCO is stopped, the resistor divider networks are disconnected and the outputs are both low, when in power down mode.
13	GND	PWR	Ground pin.
14	FS1	IN	Frequency select pin.
15	FS0	IN	Frequency select pin.
16	VDD	PWR	Power supply, nominal 3.3V
17	GND	PWR	Ground pin.
18	CLK_C	OUT	"Complimentary" clock of differential pair
19	N/C	N/C	No Connection.
20	CLK_T	OUT	"True" clock of differential pair
21	GND	PWR	Ground pin.
22	VDD	PWR	Power supply, nominal 3.3V
23	MODE1	IN	Mode Select Pin
24	MODE0	IN	Mode Select Pin

Output Frequency for FS(0:1) and REFIN Inputs

Inputs		Fdbk/Prescaler		REFIN (MHz)				
FS0	FS1	A	B	50.00	66.67	83.375	100.00	133.00
0	0	4	1	Reserved	266.68	333.50	400.00	532.00
0	1	6	1	300.00	400.02	500.25	600.00	798.00
1	0	16	3	266.67	355.57	444.67	533.33	709.33
1	1	8	1	400.00	533.36	667.00	800.00	1064.00

NOTE
1. Output Frequency = (REFIN x A)/B
2. Device operation not guaranteed at settings in shaded areas

Bypass and Test Mode Selection

Mode	MODE0	MODE1	CLK_T	CLK_C
Normal	0	0	PA CLK	PA CLK#
Bypass	1	0	PLL CLK	PLL CLK#
Test	1	1	REFIN	REFIN#
Output Test (OE)	0	1	Hi-Z	Hi-Z

NOTES
1. PA CLK is clock from phase aligner
2. PLL CLK is the full speed PLL clock with the Phase Aligner bypassed

Power Management Modes

State	PWRDN#	OE#	CLK_T	CLK_C
Normal	1	1	PA CLK	PA CLK#
Clock Stop	1	0	$V_{X,STOP}$	$V_{X,STOP}$
Powerdown	0	X	GND	GND

NOTES
1. PA CLK = clock from phase aligner

PLL Divider Selection for 600/667 MHz DRCG

MULT0	MULT1	A	B
0	0	4	1
0	1	6	1
1	1	8	1
1	0	16	3

Absolute Maximum Ratings

Supply Voltage (AVDD, VDD, VDDIR, VDDIPD) GND - 0.5 V to 4.0 V

Logic Input Voltage[1] ..... GND - 0.5 V to VDD_X + 0.5 V

Ambient Operating Temperature ..... 0°C to +70°C

Storage Temperature ..... -65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only, and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum operating conditions for extended periods may affet product reliability.

Electrical Characteristics - DC

TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/- 0.5% or 3.45V +/- 0.15 V (unless otherwise stated)

Parameters	Symbol	Min	Max	Unit
Supply Voltage (fout = 667 MHz)	V_{DD1}	3.3	3.6	V
Supply Voltage (fout <= 600 MHz)	V_{DD2}	3.135	3.465	V
Input supply reference for REFIN	$V_{DD,IR}$	1.235	3.6	V
Input supply reference for PWRDN# inputs	$V_{DDI,PD}$	1.235	2.625	V
Operating Supply Current (fout = 667 MHz)	I_{DD1}		250	mA
Operating Supply Current (fout = 660 MHz)	I_{DD2}		210	mA
Operating Supply Current (fout = 533 MHz)	I_{DD3}		200	mA
Operating Supply Current (fout = 400 MHz)	I_{DD4}		170	mA
Output disabled operating supply current[2]	I_{DDPD}		50	mA
Reference current in Power Down mode	$I_{REF,PWDN}$		50	µA
Reference current in Normal or Output Disabled mode	$I_{REF,NORM}$		2	mA
Power down operating supply current[3]	I_{DDPD}		200	µA
Input capacitance at PCLKM, SYNCLKN & REFIN	$C_{IN,PD}$	-	7	pF
Input Capacitance matching at PCLKM & SYNCLKN	$\Delta C_{IN,PD}$	-	0.5	pF
Input capacitance at CMOS pins	$C_{IN,CMOS}$	-	10	pF
Input (CMOS) signal low voltage	V_{IL}	-	0.3	V_{DD}
Input (CMOS) signal high voltage	V_{IH}	0.7	-	V_{DD}
REFIN input low voltage	$V_{IL,R}$	-	0.3	V_{DD}IR
REFIN input high voltage	$V_{IH,R}$	0.7	-	V_{DD}IR
Input signal low voltage for MULT(1:0)	$V_{IL,M}$	-	0.3	V_{DD}IPD
Input signal high voltage for MULT(1:0)	$V_{IH,M}$	0.7	-	V_{DD}IPD
Input signal low voltage for PWRDN# and OE# inputs	$V_{IL,PD}$	-	0.3	V_{DD}IPD
Input signal high voltage for PWRDN# and OE# inputs	$V_{IH,PD}$	0.7	-	V_{DD}IPD
Input leakage current	I_{IN}	-50	50	µA
Output crossing-point voltage	V_X	1.3	1.675	V
Difference in Output crossing-point voltage	ΔV_X	0	|0.2|	V
Output voltage during Clk Stop	$V_{X,STOP}$	1.1	1.675	V
Output voltage swing (peak to peak, single ended)[1]	V_{COS}	0.6	0.8	V
Output high voltage	V_{OH}	-	2.35	V
Output low voltage	V_{OL}	0.9	-	V
Output low voltage	V_{OL}	0.9	-	V
Difference in Zout between CLK_T and CLK_C	ΔZ_O	-	10	Ω
Output leakage current during Hi-Z	I_{OZ}		50	µA
Output leakage current during Clock stop	$I_{OZ,STOP}$		500	µA

Notes:

1. $V_{COS} = V_{OH} - V_{OL}$

Electrical Characteristics - AC 667 MHz Operation

TA = 0 - 70°C; Supply Voltage VDD = 3.45 V +/- 0.15 V (unless otherwise stated)

Parameters	Symbol	Min	Max	Unit
REFIN Input cycle time	$t_{CYCLE,IN}$	7.5	20[1]	ns
Input cycle-to-cycle Jitter[2]	$t_{J,IN}$	-	|200|	ps
Input duty cycle over 10,000 cycles	DC_{IN}	40%	60%	t_{CYCLE}
Input modulation frequency[3]	$f_{M,IN}$	30	33	kHz
Modulation index for triangular modulation[3]	$P_{M,IN}$	-	0.6	%
Modulation index for non-triangular modulation[3]		-	0.5	%
Phase detector input cycle time at PCLKM & SYNCLKN	$t_{CYCLE,PD}$	24	100	ns
Phase detector input cycle-to-cycle jitter[4]	t_{JPD}	-	3.5	ns
Initial phase error at phase detector inputs	$t_{ERR,INT}$	-0.5	0.5	$t_{CYCLE,PD}$
Phase detector input duty cycle over 10k cycles	$D_{CIN,PD}$	25%	75%	$t_{CYCLE,PD}$
Input slew rate (measured at 20%-80% of input voltage) for PCLKM, SYNCLKN & REFIN	t_{ISR}	1	4	V/ns
Clock cycle time	t_{CYCLE}	1.5	2.5	ns
Total jitter over 1 - 6 cycles (667 MHz)	t_J	-20	20	ps
Phase aligner phase step size (CLK_T/CLK_C)	t_{STEP}	2	-	ps
Phase Detector phase error between PCLKM and SYNCLKN (rising edges)[5]	$t_{ERR,PD}$	-100	100	ps
PLL output phase error when tracking spread spectrum clocks	$t_{ERR,SSC}$	-100	100	ps
Output cycle-to-cycle duty cycle error	$t_{DC,ERR}$	-20	20	ps
Output rise & fall times (measured at 20%-80% of output voltage)	t_{CR},t_{CF}	140	285	ps
Difference between rise and fall times on a single device(20%-80%)	$\Delta t_{CR,CF}$	-	100	ps
Cycle-to-Cycle jitter during Test Mode	t_{JT}	-	500	ps
Average output duty cycle over 10,000 cycles during Test Mode	DC_T	45%	55%	$t_{CYCLE,PD}$
Output rise & fall times (measured at 20%-80% of output voltage) during Test Mode	t_{CRT},t_{CFT}	250	900	ps

NOTES

1. Maximum REFIN cycle time does not apply to Test Mode
2. REFIN jitter is measured at (nominal $V_{DD,IR}$)/2 and is the absolute value of the worst case +/- deviation, not the peak-to-peak jitter.
3. If input modulation is used; input modulation is not required.
4. The input jitter for the Phase Detector inputs is defined from cycle-to-cycle on one input signal (not between the two Phase Detector inputs), and is measured at (nominal $V_{DDI,PD}$)/2.
5. Phase detector phase error is a component specification and not an external distributed loop in a system. This specification applies to average phase error and does not include input clock jitter.

Electrical Characteristics - AC 600MHz or Less Operation

TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/- 5% (unless otherwise stated)

Parameters	Symbol	Min	Max	Unit
REFIN Input cycle time	$t_{CYCLE,IN}$	7.5	20[1]	ns
Input cycle-to-cycle Jitter[2]	$t_{J,IN}$	-	|200|	ps
Input duty cycle over 10,000 cycles	DC_{IN}	40%	60%	t_{CYCLE}
Input modulation frequency[3]	$f_{M,IN}$	30	33	kHz
Modulation index for triangular modulation[3]	$P_{M,IN}$	-	0.6	%
Modulation index for non-triangular modulation[3]		-	0.5	%
Phase detector input cycle time at PCLKM & SYNCLKN	$t_{CYCLE,PD}$	24	100	ns
Phase detector input cycle-to-cycle jitter[4]	t_{JPD}	-	3.5	ns
Initial phase error at phase detector inputs	$t_{ERR,INT}$	-0.5	0.5	$t_{CYCLE,PD}$
Phase detector input duty cycle over 10k cycles	$D_{CIN,PD}$	25%	75%	$t_{CYCLE,PD}$
Input slew rate (measured at 20%-80% of input voltage) for PCLKM, SYNCLKN & REFIN	t_{ISR}	1	4	V/ns
Clock cycle time	t_{CYCLE}	1.667	2.5	ns
Total jitter over 1 - 6 cycles (<= 600 MHz)	t_J	-20	20	ps
Phase aligner phase step size (CLK_T/CLK_C)	t_{STEP}	2	-	ps
Phase Detector phase error between PCLKM and SYNCLKN (rising edges)[5]	$t_{ERR,PD}$	-100	100	ps
PLL output phase error when tracking spread spectrum clocks	$t_{ERR,SSC}$	-100	100	ps
Output cycle-to-cycle duty cycle error	$t_{DC,ERR}$	-20	20	ps
Output rise & fall times (measured at 20%-80% of output voltage)	t_{CR},t_{CF}	140	285	ps
Difference between rise and fall times on a single device(20%-80%)	$\Delta t_{CR,CF}$	-	100	ps
Cycle-to-Cycle jitter during Test Mode	t_{JT}	-	500	ps
Average output duty cycle over 10,000 cycles during Test Mode	DC_T	45%	55%	$t_{CYCLE,PD}$
Output rise & fall times (measured at 20%-80% of output voltage) during Test Mode	t_{CRT},t_{CFT}	250	900	ps

NOTES

1. Maximum REFIN cycle time does not apply to Test Mode
2. REFIN jitter is measured at (nominal $V_{DD,IR}$)/2 and is the absolute value of the worst case +/- deviation, not the peak-to-peak jitter.
3. If input modulation is used; input modulation is not required.
4. The input jitter for the Phase Detector inputs is defined from cycle-to-cycle on one input signal (not between the two Phase Detector inputs), and is measured at (nominal $V_{DDI,PD}$)/2.
5. Phase detector phase error is a component specification and not an external distributed loop in a system. This specification applies to average phase error and does not include input clock jitter.

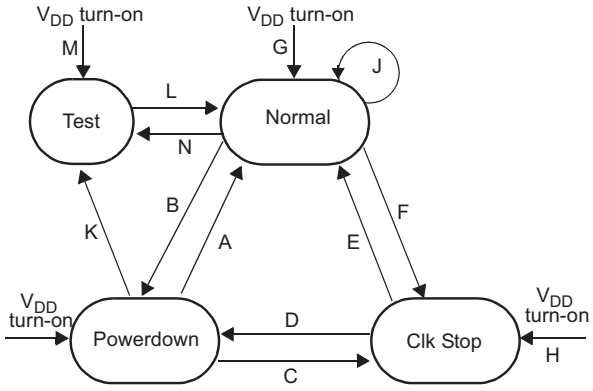


Figure 1: DRCG State Diagram

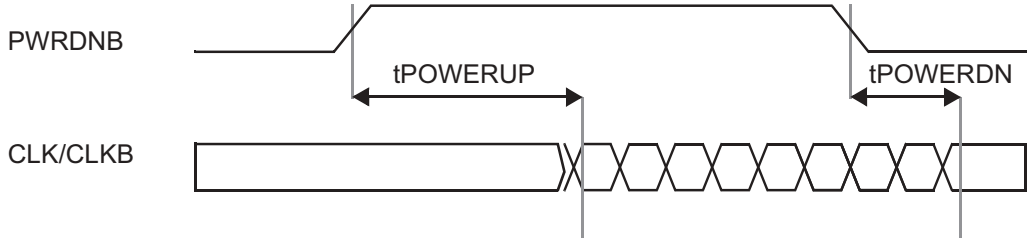


Figure 2: PWRDNB Transition Timings

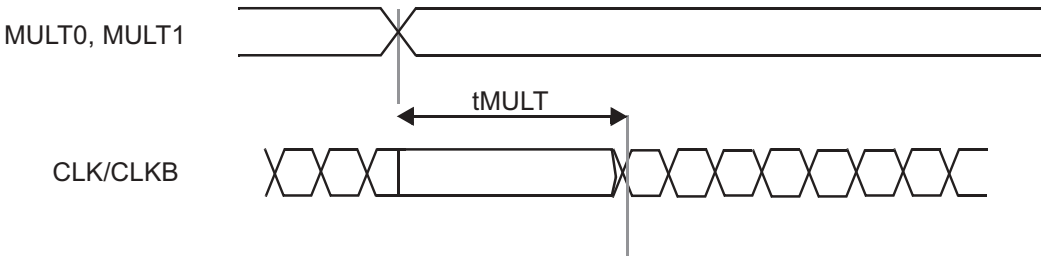


Figure 3: MULT Transition Timings

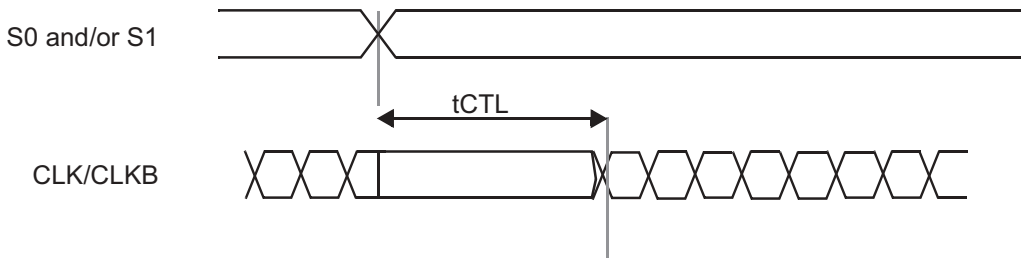


Figure 4: S0 and S1 Transition Timings

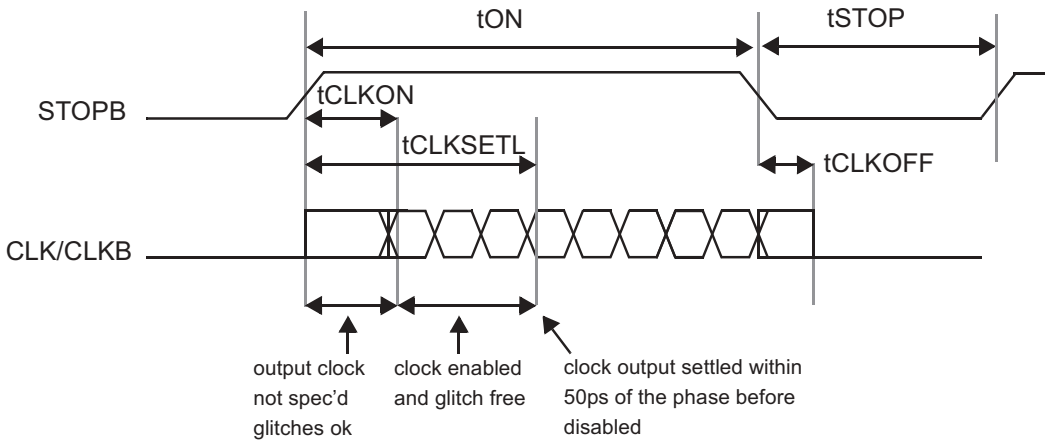


Figure 5: StopB Transition Timings

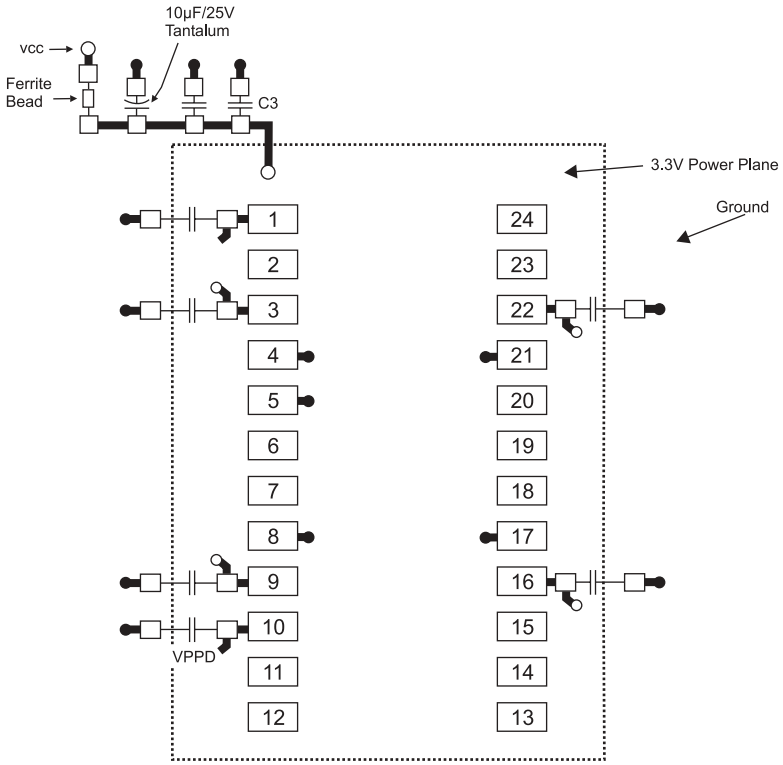
State Transition Latency Specifications

Transition	From	To	Transition Latency		Description
			Symbol	Max	
A	Power-down	Normal	tPOWERUP	3 ms	Time from PWRDNB to CLK/CLKB output settled (excluding tDISTLOCK).
C	Power-down	Clk Stop	tPOWERUP	3 ms	Time from PWRDNB until the internal PLL and clock has turned ON and settled.
K	Power-down	Test	tPOWERUP	3 ms	Time from PWRDNB to CLK/CLKB output settled (excluding tDISTLOCK).
G	V_{DD} ON	Normal	tPOWERUP	3 ms	Time from when V_{DD} is applied and settled until CLK/CLKB output is settled (excluding tDISTLOCK).
H	V_{DD} ON	Clk Stop	tPOWERUP	3 ms	Time from when V_{DD} is applied and settled until the internal PLL and clock has turned ON and settled.
M	V_{DD} ON	Test	tPOWERUP	3 ms	Time from when V_{DD} is applied and settled until the output clock has turned ON and settled.
J	Normal	Normal	tMULT	1 ms	Time from when MULT0 or MULT1is changed until CLK/CLKB output has re-settled (excluding tDISTLOCK).
E	Clk Stop	Normal	tCLKON	10 ns	Time from STOPB until CLK/CLKB provides glitch-free clock edges.
E	Clk Stop	Normal	tCLKSETL	20 cycles	Time from STOPB to CLK/CLKB output settled to within 50ps of the phase before CLK/CLKB was disabled.
F	Normal	Clk Stop	tCLKOFF	5 ns	Time from STOPB to CLK/CLKB output disabled.
L	Test	Normal	tCTL	3 ms	Time from when S0 or S1 is changed until CLK/CLKB output has re-settled (excluding tDISTLOCK).
N	Normal	Test	tCTL	3 ms	Time from when S0 or S1 is changed until CLK/CLKB output has re-settled (excluding tDISTLOCK).
B,D	Normal or Clk Stop	Power-down	tPOWERDN	1 ms	Time from PWRDNB to the device in Powerdown Mode.

Recommended Layout

General Layout Precautions:
1) Use a ground plane on the top layer of the PCB in all areas not used by traces.

2) Make all power traces and vias as wide as possible to lower inductance.



● = Ground Plane Connection

○ = Power Plane Connection

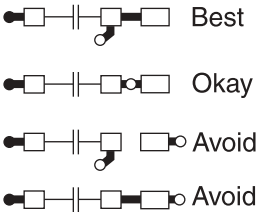
□ = Solder Pads

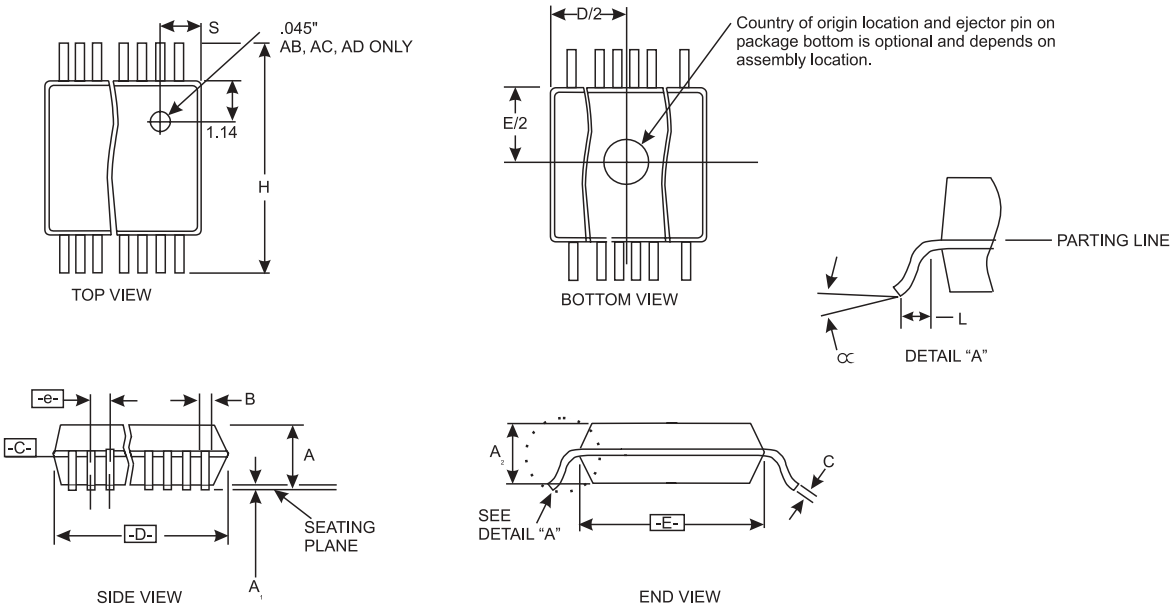
Capacitor Values:

C3 : 100pF ceramic

All unmarked capacitors are 0.01µF ceramic

Connections to VDD:





SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			S			
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	N
A	.061	.064	.068	AA	.189	.194	.196	.0020	.0045	.0076	16
A1	.004	.006	.0098	AB	.337	.342	.344	.0500	.0525	.0550	20
A2	.055	.058	.061	AC	.337	.342	.344	.0250	.0275	.0300	24
B	.008	.010	.012	AD	.386	.391	.393	.0250	.0280	.0300	28
C	.0075	.008	.0098								
D	SEE VARIATIONS										
E	.150	.155	.157								
e	.025 BSC										
H	.230	.236	.244								
L	.010	.013	.016								
N	SEE VARIATIONS										
S	SEE VARIATIONS										
µ	0°	5°	8°								
X	0.85	0.93	.100								

150 mil SSOP Package

Diminisions are in inches

Ordering Information

ICS9217yF - LF

Example:

ICS XXXX y F - PPLF T

- **Designation for tape and reel packaging**
- **Lead Free (if required)**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device

0816B—10/06/03