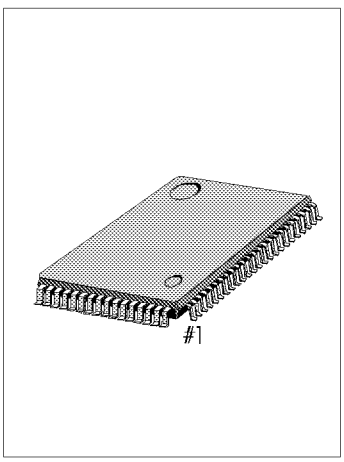
INTRODUCTION

80 QFP-1420C



The KS0103 is a LCD driver LSI which is fabricated by low power CMOS high voltage process technology. This device consists of 68 bit bidirectional shift register. 68 bit level shifter and 68 bit 4-level driver. To use for a wide LCD panel, more than two KS0103 are connected in series.

FUNCTION

- Dot matrix LCD common driver with 68 channel output
- Input/Output signal
  - Input : • frame signal and control pulse from controller.
    • bias voltage (V_1, V_2, V_5)
  - Output ; 68 channel waveform for LCD driving

FEATURES

- Power supply voltage : + 5V±10%
- Supply voltage for display : 8 ~ 28V (V_{DD}, V_{EE})
- Applicable LCD duty : 1/64 ~ 1/256
- Interface

Driver	
COM (cascade)	SEGMENT
Other KS0103	KS0104/B, KS0083/84, KS0086

(Three chips of the KS0103 are required to drive 1/200 duty LCD)

- High voltage CMOS process
- 80 QFP and bare chip available.

BLOCK DIAGRAM

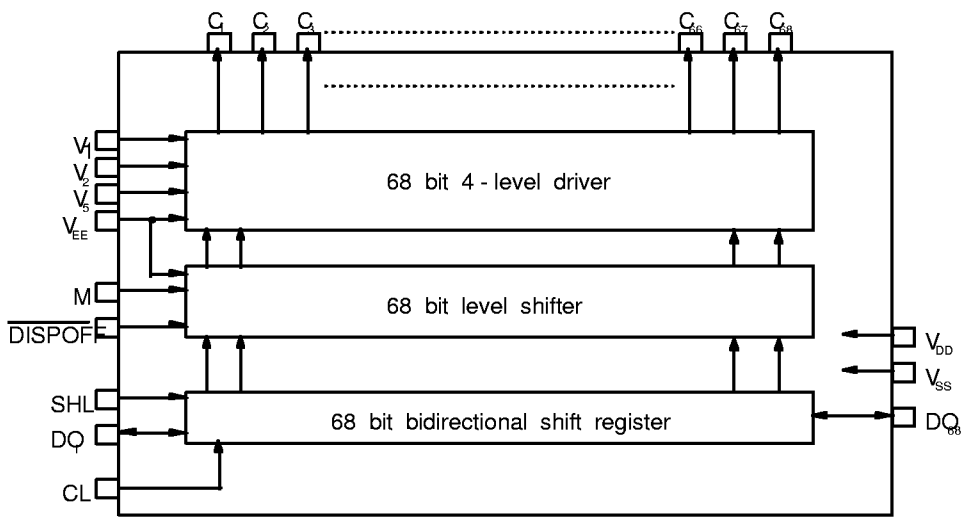


Fig 1. KS0103 Functional block diagram

PIN CONFIGURATION

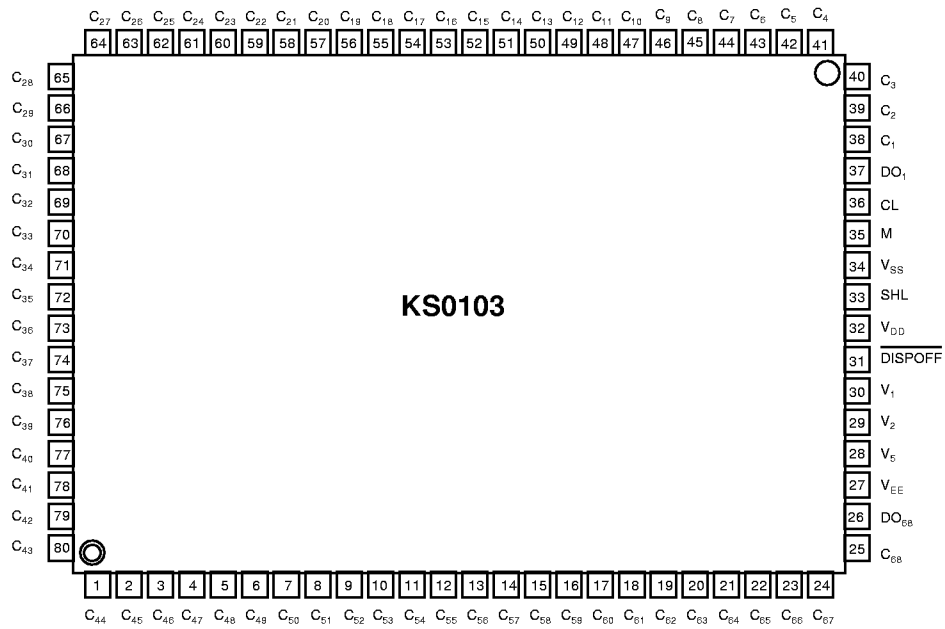


Fig 2. 80 QFP Top View

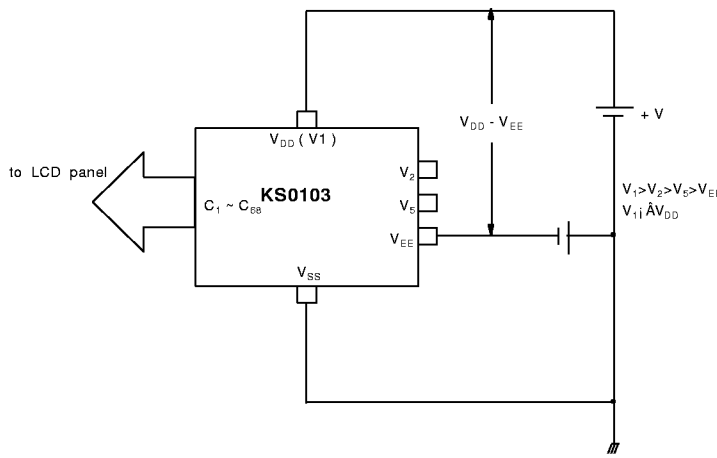
PIN DESCRIPTION

<table>
<tr><th>PIN (No)</th><th>INPUT/ OUTPUT</th><th>NAME</th><th>DESCRIPTION</th><th>INTERFACE</th></tr>
<tr><td>V_{DD}(32)</td><td rowspan="3">Power</td><td>Operating Voltage</td><td>For logical circit (+5V±10%)</td><td rowspan="3">Power Supply</td></tr>
<tr><td>V_{SS}(34)</td><td></td><td>0V (GND)</td></tr>
<tr><td>V_{EE}(27)</td><td>Negative Supply Voltage</td><td>For LCD driver circuit.</td></tr>
<tr><td>V_5, V_2, V_1 (28-30)</td><td>Input</td><td>LCD driver output voltage level</td><td>Bias supply voltage terminals to drive the LCD.
Bias voltage divided by the resistance usually used as supply voltage source (refer to note1)
<table>
<tr><th>select level</th><th>non select level</th></tr>
<tr><td>$V_1 \leftrightarrow V_{EE}$</td><td>$V_2 \leftrightarrow V_5$</td></tr>
</table></td><td>Power</td></tr>
<tr><td>C_1 ~ C_{68} (1-25, 38-80)</td><td>Output</td><td>LCD driver output</td><td>Display data output terminals which correspond to 68 bit shift register contents. (refer to note 2)</td><td>LCD</td></tr>
<tr><td>CL(36)</td><td>Input</td><td>Data shift Clock</td><td>Clock pulse input pin for 68 bit bidiretional shift register.
The data is shifted to 68 bit shift register at the falling edge of clock pulse(↓)</td><td>Controller</td></tr>
<tr><td>M(35)</td><td>Input</td><td>Alternated signal for LCD driver output</td><td>Alternate signal input for LCD driving.
Normal frame inversion signal is input</td><td>Controller</td></tr>
<tr><td>$\overline{DISPOFF}$ (31)</td><td>Input</td><td>Output level control</td><td>Control input pin for display data output level (C_1 ~ C_{68}).
V_1 level is output from C_1 ~ C_{68} terminal during “L” level input.
LCD becomes non-selected by V_1 level output from every output of segment drivers and common drivers. (refer to note 2)</td><td>Controller</td></tr>
<tr><td>SHL(33)</td><td>Input</td><td>Data interface</td><td>DO1 and DO68 are 68 bit bidirectional shift register input/output terminals
The shifting direction is selected by the SHL terminal (refer to note 3)</td><td>V_{DD} or V_{SS}</td></tr>
<tr><td>D_{O1}, D_{O68} (37,26)</td><td>Input Output</td><td colspan="2">
<table>
<tr><th>SHL</th><th>Shifting direction</th><th colspan="3">Description</th></tr>
<tr><td rowspan="2">L</td><td rowspan="2">$C_1 \rightarrow C_{68}$</td><td>Input</td><td>DO_1</td><td>The scanning data from the LCD controller LSI is input from DO_1 synchronized with the clock pulse. (refer to note 3)</td></tr>
<tr><td>Output</td><td>DO_{68}</td><td>Shift register contents output terminal. The data which was input from DO_1 in output from DO_{68} with 68 bit’s delay, synchronized with the clock pulse.</td></tr>
<tr><td rowspan="2">H</td><td rowspan="2">$C_{68} \rightarrow C_1$</td><td>Input</td><td>DO_{68}</td><td>The scanning data from the LCD controller LSI is input from DO_{68} synchronized with the clock pulse.</td></tr>
<tr><td>Output</td><td>DO_1</td><td>Shift register contents output terminal. The data which was input from DO_{68} in output from DO_1 with 68 bit’s delay, synchronized with the clock pulse.</td></tr>
</table>
</td><td>Controller or KS0103</td></tr>
</table>

MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{DD}	-0.3 ~ 6.0	V
Driver Supply Voltage	V_{LCD}	0 ~ 30	V
Input Voltage	V_{IN}	-0.3 ~ V_{DD}+0.3	V
Operating Temperature	T_{OPR}	-30 ~ +85	µA
Storage Temperature	T_{STG}	-55 ~ +150	µA

* Voltage greater than above may result in damage to the circuit.



ELECTERICAL CHARACTERISTICS

DC Characteristics (V_{DD}=5V±10%, V_{SS}=0V, Ta=-30~ +85°C, C_L=15pF)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	-	4.5	-	5.5	V
Driver Supply Voltage	V_{DD}-V_{EE}	-	8	-	28	
Input Voltage (*1)	V_{IH}	-	0.8V_{DD}	-	-	
	V_{IL}	-	-	-	0.2V_{DD}	
Input Current	I_{IH}	V_{IH}=V_{DD}, V_{DD}=5.5V	-	-	1	µA
	I_{IL}	V_{IH}=0V, V_{DD}=5.5V	-	-	-1	
Output Voltage (*2)	V_{OH}	I_O=-0.4mA, V_{DD}=4.5V	V_{DD}-0.4	-	-	V
	V_{OL}	I_O=0.4mA, V_{DD}=4.5V	-	-	0.4	
On Resistance(*3)	R_{ON}	V_{DD}-V_{EE}=23V, V_{DD}=4.5V, (*4)¡¢Vn-Vo¡¢=0.25V	-	1.5	3	KΩ
Operating Current	I_{DD}	CL=14kHz, V_{DD}=5.5V V_{DD}-V_{EE}=23V (no load)	-	-	100	µA
Input Capacitance	Ci	f=1MHz	-	5	-	pF

*1; Applicable pin; CL, DO_1, DO_{68}, SHL, M, $\overline{DISPOFF}$
*2; Applicable pin; DO_1, DO_{60}
*3; Applicable pin; C1-C68
*4; V_n=V_{DD} ~ V_{EE}, V_5=1/15 (V_{DD}-V_{EE}), V_2=14/15 (V_{DD}-V_{EE}, V_{DD}=V_1)

AC Characteristics (V_{DD}=+5V±10%, V_{SS}=0V, T_a=-30 ~ +85°C, C_L=15pF)

Characteristic	Symbol	Conditions	Min	Type	Max	Unit
Delay Time	t_D	-	-	-	250	ns
Clock Frequency	f_{CK}	-	1	-	-	MHz
Clock Pulse Width(CL)	t_{WCK}	-	125	-	-	ns
Data Set-up Time	t_{SU}	DO_1 (DO_{68})→CL	100	-	-	ns
Data Hold Time	t_{DH}	DO_1 (DO_{68})→CL	100	-	-	ns
Clock Rise/Fall Time (CL)	t_R, t_F	-	-	-	50	ns

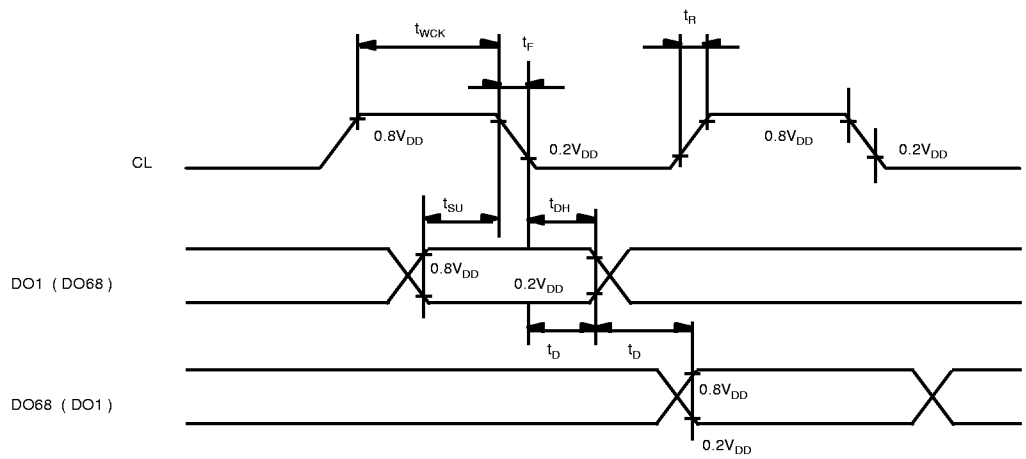
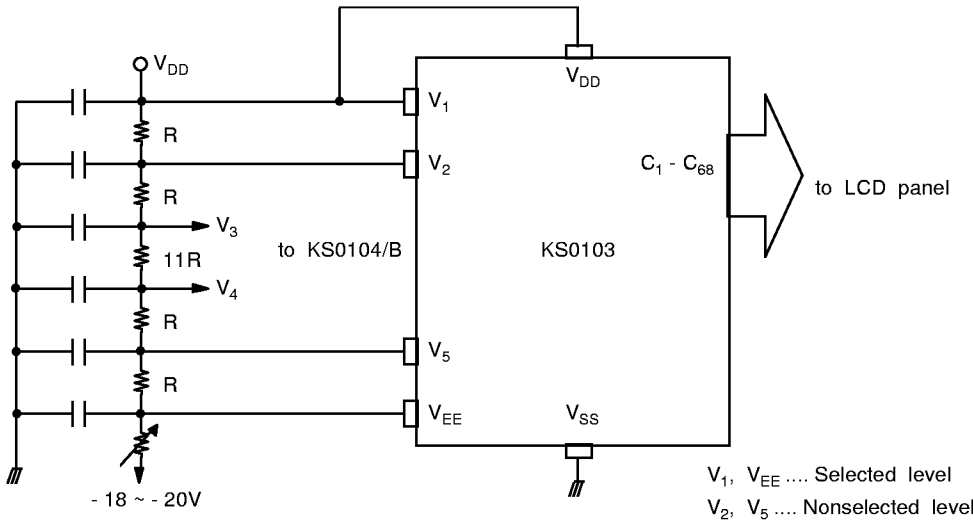


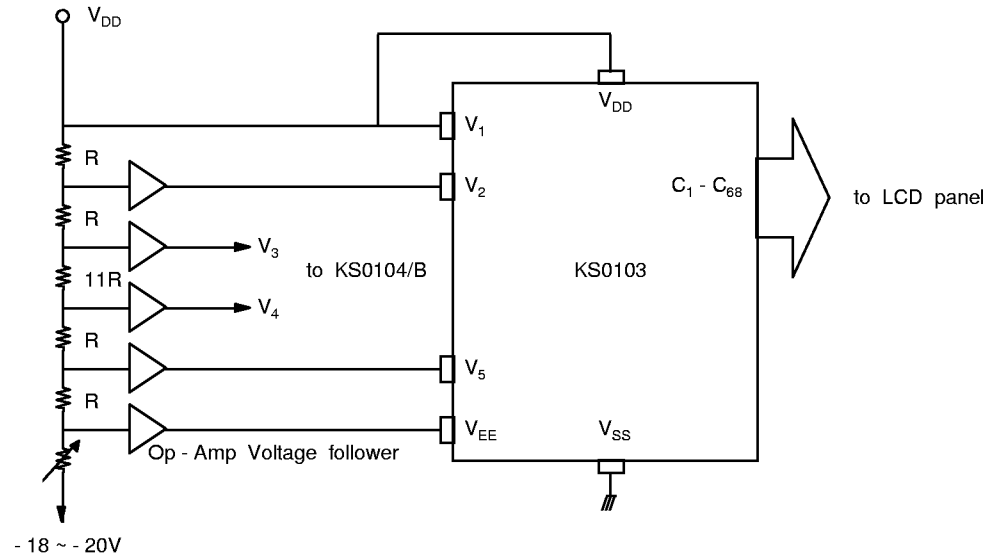
Fig. 3. Timing Characteristic

NOTE 1

The below figure shows when the bias voltage is devided by the resistance. (V1 is not necessarily connected to V_{DD}. 1/15 bias 1/200 duty)



The below figure shows when the bias voltage is supplied by the OP-Amp.(1/15 bias, 1/200 duty)



NOTE 2

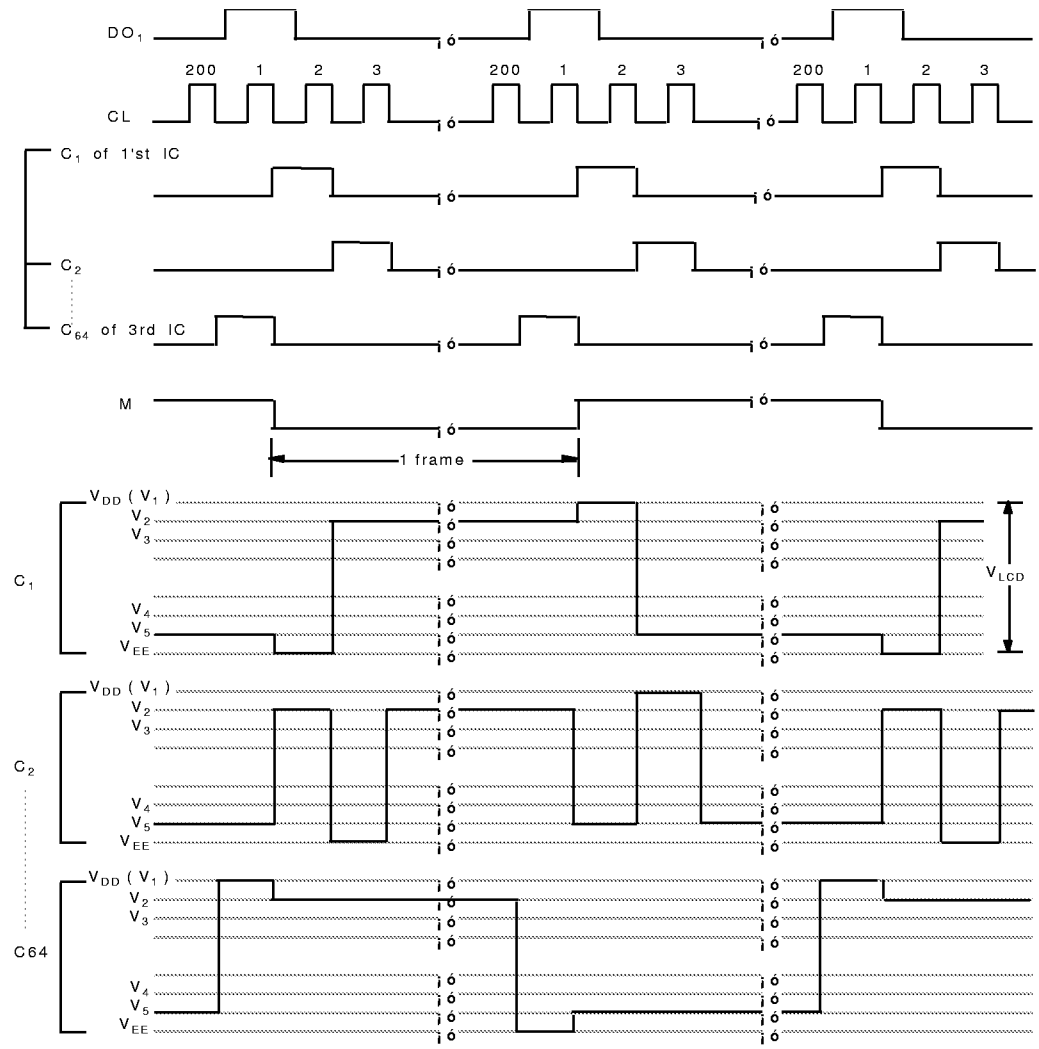
M	Latched Data level	$\overline{DISPOFF}$	Display data output level (C_1~C_{68})
L	L	H	V_2
L	H	H	V_{EE}
H	L	H	V_5
H	H	H	V_1
X	X	L	V_1

NOTE 3

The combination of the scanning data, DO_1 or DO_{68} and the LCD driving output, C_1 ~ C_{68}, is shown in the table below.

DO1, DO68	LCD driving output
H	Selected level (V_1, V_{EE})
L	Non-selected level (V_2, V_5)

LCD OUTPUT WAVEFORMS (1/15 bias, 1/200 duty)



$V_1 = V_{DD}$

$V_2 = V_{DD} - 1/15\ V_{LCD}$

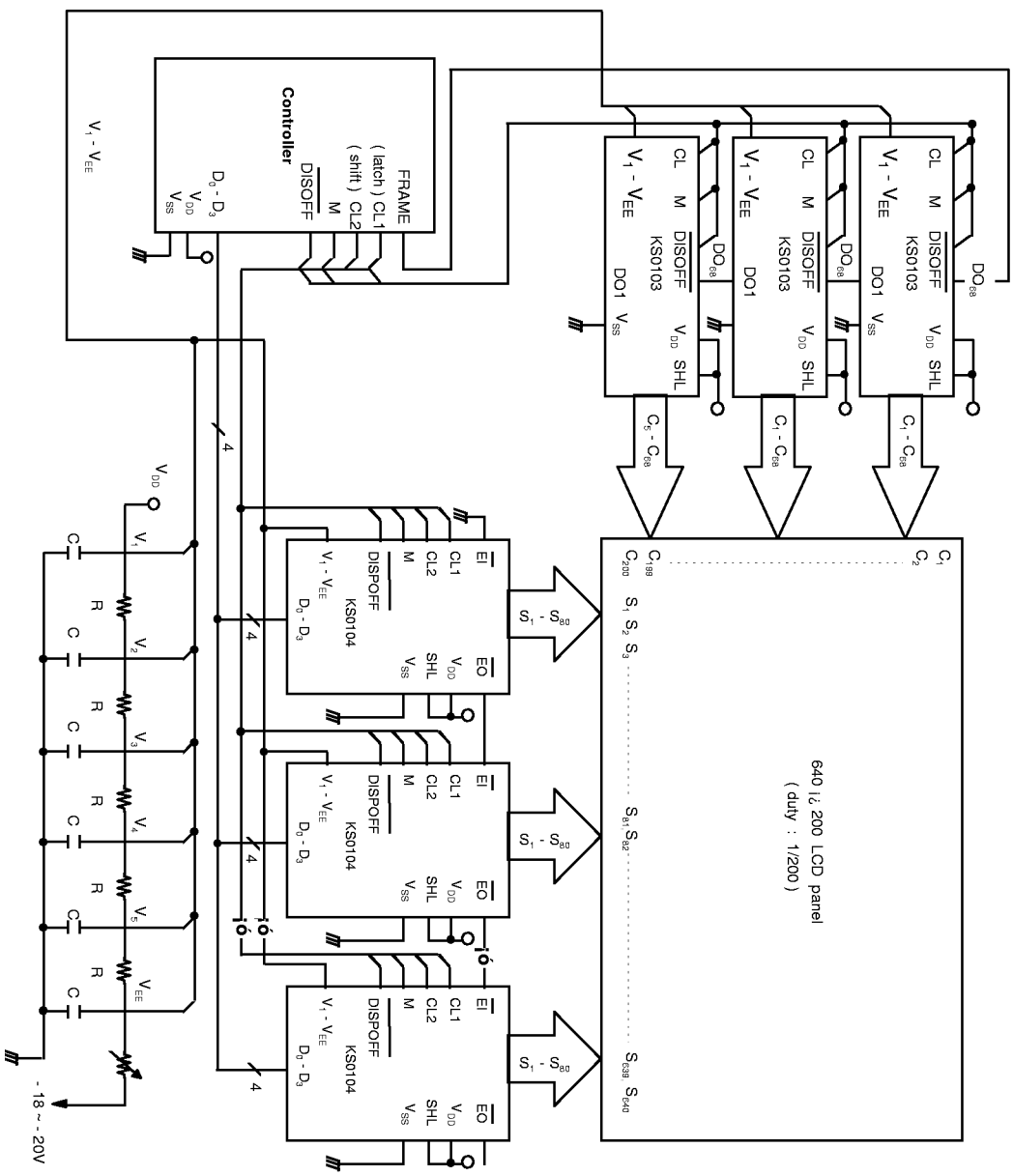
$V_3 = V_{DD} - 2/15\ V_{LCD}$

$V_4 = V_{DD} - 13/15\ V_{LCD}$

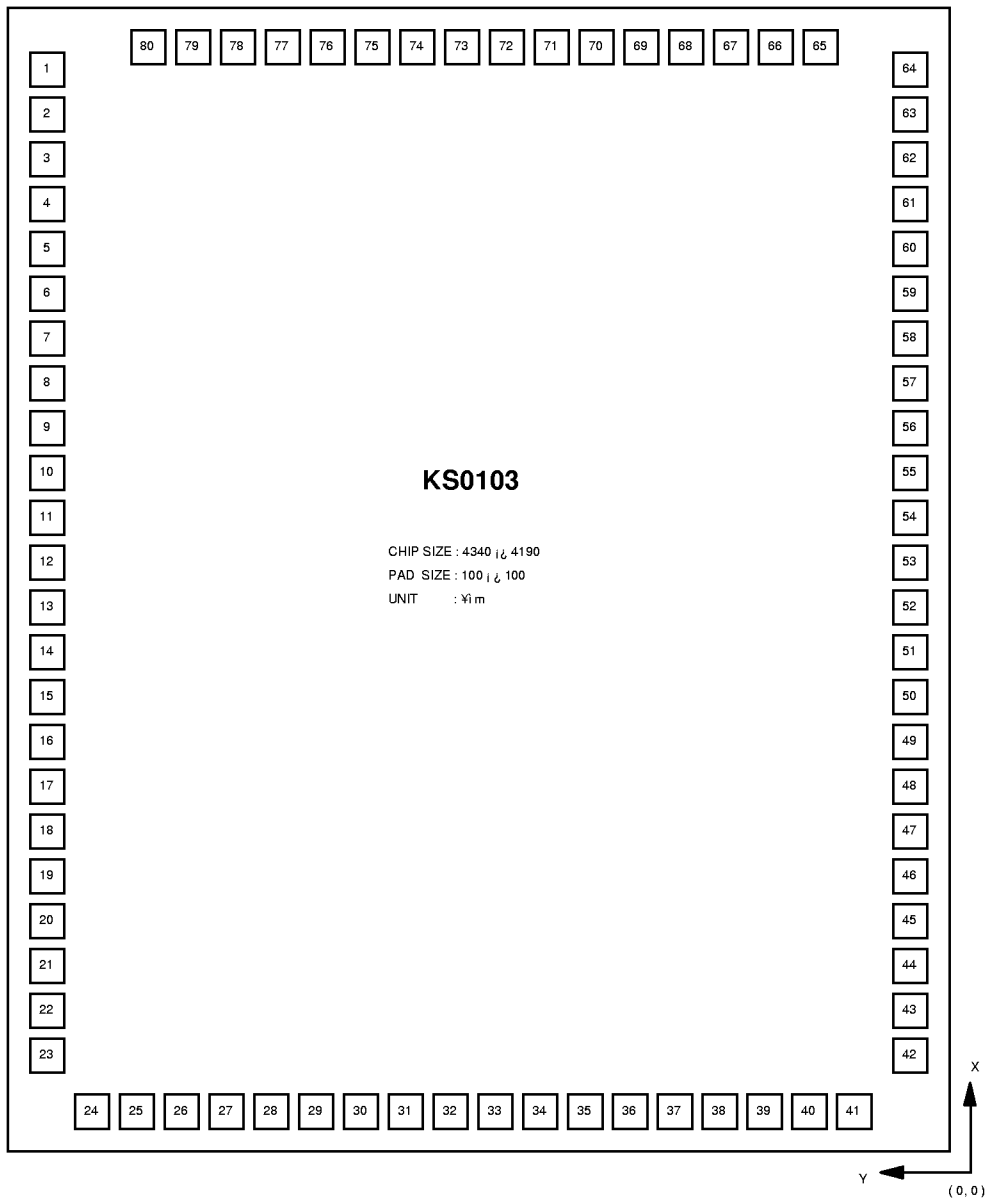
$V_5 = V_{DD} - 14/15\ V_{LCD}$

$V_{LCD} = V_{DD} - V_{EE}$

APPLICATION CIRCUIT



PAD DIAGRAM


80 79 78 77 76 75 74 73 72 71 70 69 68 67 66 65
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42
24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41
KS0103
CHIP SIZE : 4340 ¡¿ 4190
PAD SIZE : 100 ¡ ¿ 100
UNIT : ¥i m
X
Y
(0, 0)

PAD LOCATION

UNIT(μm)

PAD NUMBER	PAD NAME	COORDINATE X	COORDINATE Y	PAD NUMBER	PAD NAME	COORDINATE X	COORDINATE Y	PAD NUMBER	PAD NAME	COORDINATE X	COORDINATE Y
1	C44	4115	4055	28	V5	135	3115	55	C18	2585	135
2	C45	3945	4055	29	V2	135	2875	56	C19	2755	135
3	C46	3775	4055	30	V1	135	2635	57	C20	2925	135
4	C47	3605	4055	31	DISPOFF	135	2405	58	C21	3095	135
5	C48	3435	4055	32	VDD	135	2165	59	C22	3265	135
6	C49	3265	4055	33	SHL	135	1935	60	C23	3435	135
7	C50	3095	4055	34	VSS	135	1695	61	C24	3605	135
8	C51	2925	4055	35	M	135	1455	62	C25	3775	135
9	C52	2755	4055	36	CL	135	1225	63	C26	3945	135
10	C53	2585	4055	37	DO1	135	955	64	C27	4115	135
11	C54	2415	4055	38	C1	135	745	65	C28	4205	365
12	C55	2245	4055	39	C2	135	575	66	C29	4205	595
13	C56	2075	4055	40	C3	135	405	67	C30	4205	825
14	C57	1905	4055	41	C4	135	235	68	C31	4205	1055
15	C58	1735	4055	42	C5	375	135	69	C32	4205	1285
16	C59	1565	4055	43	C6	545	135	70	C33	4205	1515
17	C60	1395	4055	44	C7	715	135	71	C34	4205	1745
18	C61	1225	4055	45	C8	885	135	72	C35	4205	1975
19	C62	1055	4055	46	C9	1055	135	73	C36	4205	2215
20	C63	885	4055	47	C10	1225	135	74	C37	4205	2445
21	C64	715	4055	48	C11	1395	135	75	C38	4205	2675
22	C65	545	4055	49	C12	1565	135	76	C39	4205	2905
23	C66	375	4055	50	C13	1735	135	77	C40	4205	3145
24	C67	135	3985	51	C14	1905	135	78	C41	4205	3385
25	C68	135	3815	52	C15	2075	135	79	C42	4205	3625
26	DO68	135	3605	53	C16	2245	135	80	C43	4205	3865
27	VEE	135	3355	54	C17	2415	135				

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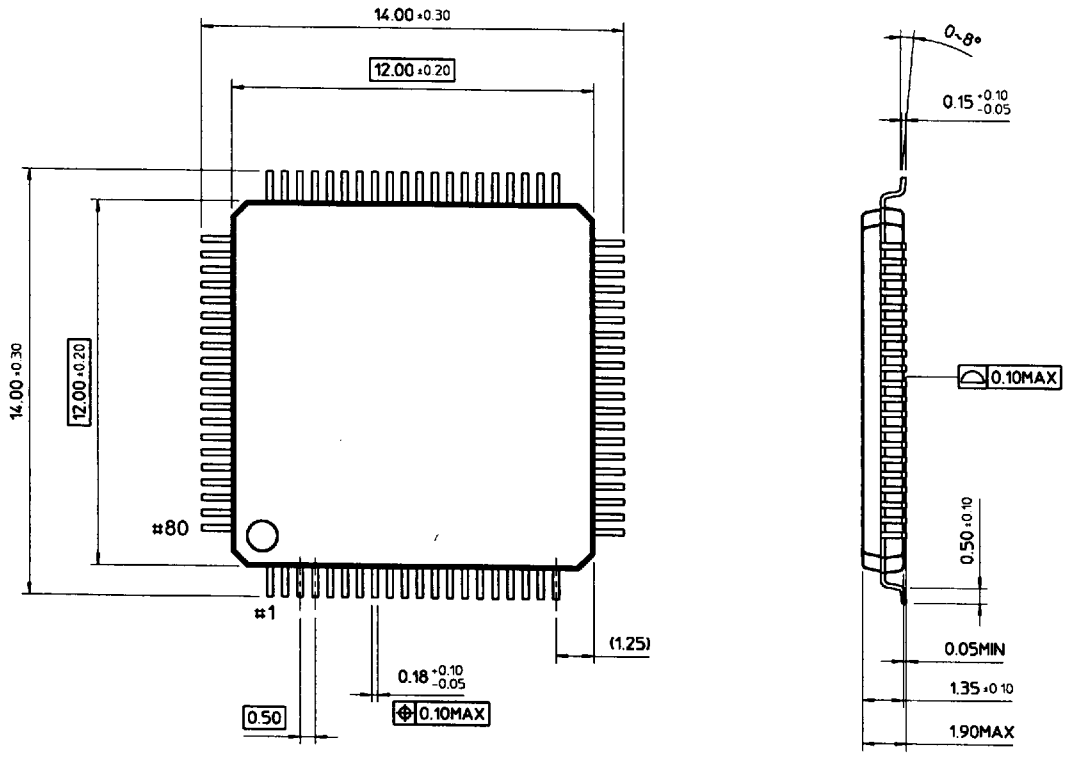

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