SIEMENS

Microcomputer Components

8-Bit CMOS Microcontroller

C515C-8E

Addendum to C515C User's Manual 08.96

Rev. 1.0 05.97

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1 Introduction

The C515C-8E is the OTP version in the C515C-8R microcontroller with a one-time programmable 64K byte program memory. With the C515C-8E fast programming cycles are achieved (1 byte in 100 µsec). Also several levels of OTP memory protection can be selected. The basic functionality of the C515C-8E as a microcontroller is upward compatible to the C515C-8R (ROM part) or C515C-L (romless part) functionality.
Additionally, the functionality of the C515C-8E has been upgraded by two features :

- the wake-up from software power down mode can, additionally to the external pin P3.2/$\overline{\text{INT0}}$ wake-up capability, also be triggered alternatively by a second pin P4.7/RXDC.
- for power consumption reasons the on-chip CAN controller can be switched off during normal operating mode of the C515C-8E.

This document describes in detail the C515C-8E programming interface. The description of the detailed microcontroller functions of the C515C is given in the “C515C User’s Manual 08.96“.

2 Extended Functionality of the C515C-8E

2.1 Second Pin for Wake-up from Software Power Down

Additionally to pin P3.2/$\overline{\text{INT0}}$ of the C515C-8R, the C515C-8E provides a second pin (P4.7/RXDC) which can be used alternatively for the wake-up from software power down mode operation. The selection of the port pin for the wake-up function is controlled by bit WS in SFR PCON1. PCON1 is a mapped SFR at address 88_H and can only be accessed when bit RMAP (bit 4 in SFR SYSCON ($B1_H$)) is set.

See pages 9-7 and 9-8 of the C515C User's Manual 08.96 for detailed description of the wake-up sequence. The timing for the wake-up sequence of pin P4.7/RXDC is identical to the timing for pin P3.2/$\overline{\text{INT0}}$.

Special Function Register PCON1 (Mapped Address $88_{H)}$ **Reset Value : $0XX0XXXX_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
88_H	EWPD	–	–	WS	–	–	–	–	PCON1

Symbol	Function
EWPD	External wake-up from power down enable bit Setting EWPD before entering software power down mode, enables the external wake-up from software power down mode capability of the C515C-8E.
WS	Wake-up from software power down mode source select WS = 0 : wake-up via pin P3.2/$\overline{\text{INT0}}$ selected (default after reset) WS = 1 : wake-up via pin P4.7/RXDC selected
–	Reserved bits for future use. Read by CPU returns undefined values.

2.2 Switch-off Capability of the CAN Controller

For power consumption reasons the on-chip CAN controller can be switched off during normal operating mode of the C515C-8E by setting bit CSWO in SFR SYSCON. When the CAN controller is switched off its clock signal is turned off and the operation of the CAN controller is stopped. This switch-off state of the CAN controller is equal to its state in software power down mode. Any message transfer is interrupted. In order to ensure that the CAN controller is not stopped while sending a dominant level (“0”) on the CAN bus, the microcontroller should set bit INIT in the Control Register prior to setting bit CSWO. The C515C-8E can check, if a transmission is in progress by reading bits TXRQ and NEWDAT in the message objects and bit TXOK in the Control Register. After clearing bit CSWO again the CAN controller has to be reconfigured.

Special Function Register SYSCON (Address $B1_H$) **Reset Value : $XX100001_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$B1_H$	–	PMOD	EALE	RMAP	–	CSWO	XMAP1	XMAP0	SYSCON

The functions of the shaded bits are not described in this section.

Bit	Function
–	Reserved bits for future use. Read by CPU returns undefined values.
CSWO	CAN controller switch-off bit CSWO = 0 : CAN controller is enabled (default after reset). CSWO = 1 : CAN controller is switched off.

When the C515C-8E is put into software power down mode, bit CSWO is not affected. This means, when software power down mode is entered with CAN controller switched off, the CAN controller stays in switch-off state after the wake-up from software power down mode has been left*.

3 Programming Configuration

During normal program execution the C515C-8E behaves like the C515C-8R/C515C-L. For programming of the device, the C515C-8E must be put into the programming mode. This typically is done not in-system but in a special programming hardware. In the programming mode the C515C-8E operates as a slave device similar as an EPROM standalone memory device and must be controlled with address/data information, control lines, and an external 11.5 V programming voltage.

In the programming mode port 0 provides the bidirectional data lines and port 2 is used for the multiplexed address inputs. The upper address information at port 2 is latched with the signal PALE. For basic programming mode selection the inputs $\overline{\text{RESET}}$, $\overline{\text{PSEN}}$, $\overline{\text{EA}}/V_{PP}$, ALE, PMSEL1/0, and PSEL are used. Further, the inputs PMSEL1,0 are required to select the access types (e.g. program/verify data, write lock bits, ...) in the programming mode. In programming mode V_{CC}/V_{SS} and a clock signal at the XTAL pins must be applied to the C515C-8E. The 11.5 V external programming voltage is applied to the $\overline{\text{EA}}/V_{PP}$ pin.

Figure 1 shows the pins of the C515C-8E which are required for controlling of the OTP programming mode.

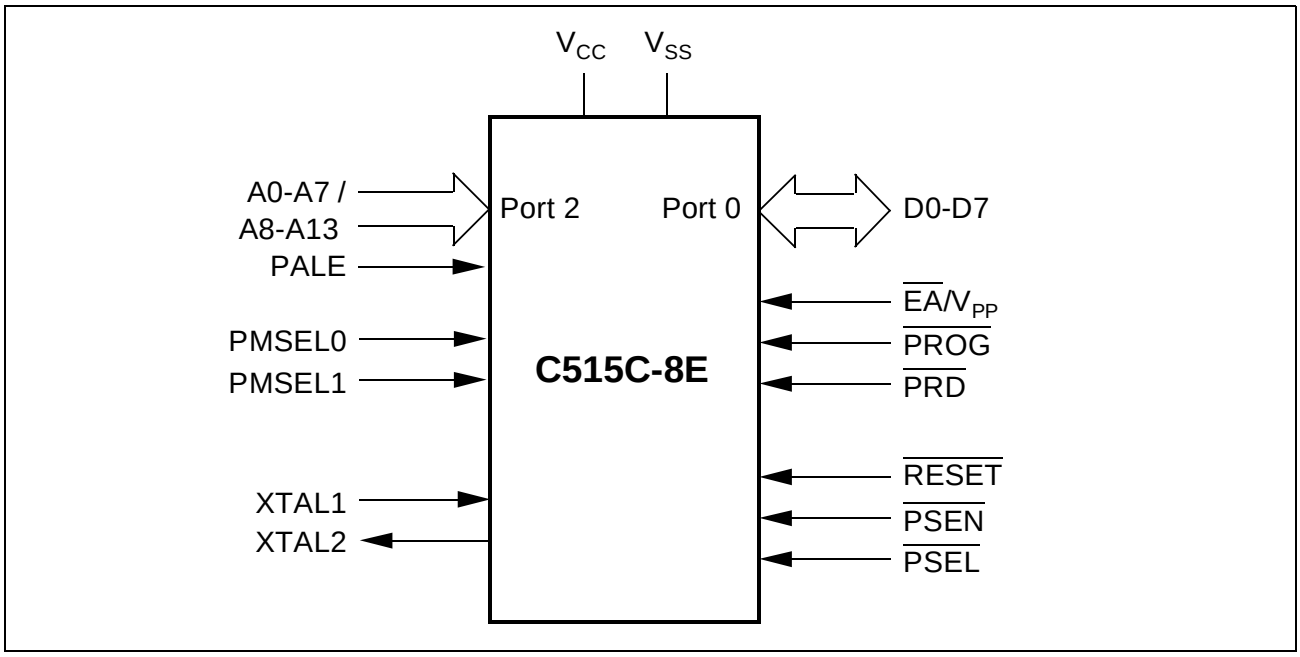


Figure 1
Programming Mode Configuration

3.1 Pin Configuration of OTP Programming Mode

Figure 2 shows the detailed pin configuration (P-MQFP-44-2 package) of the C515C-8E in programming mode.

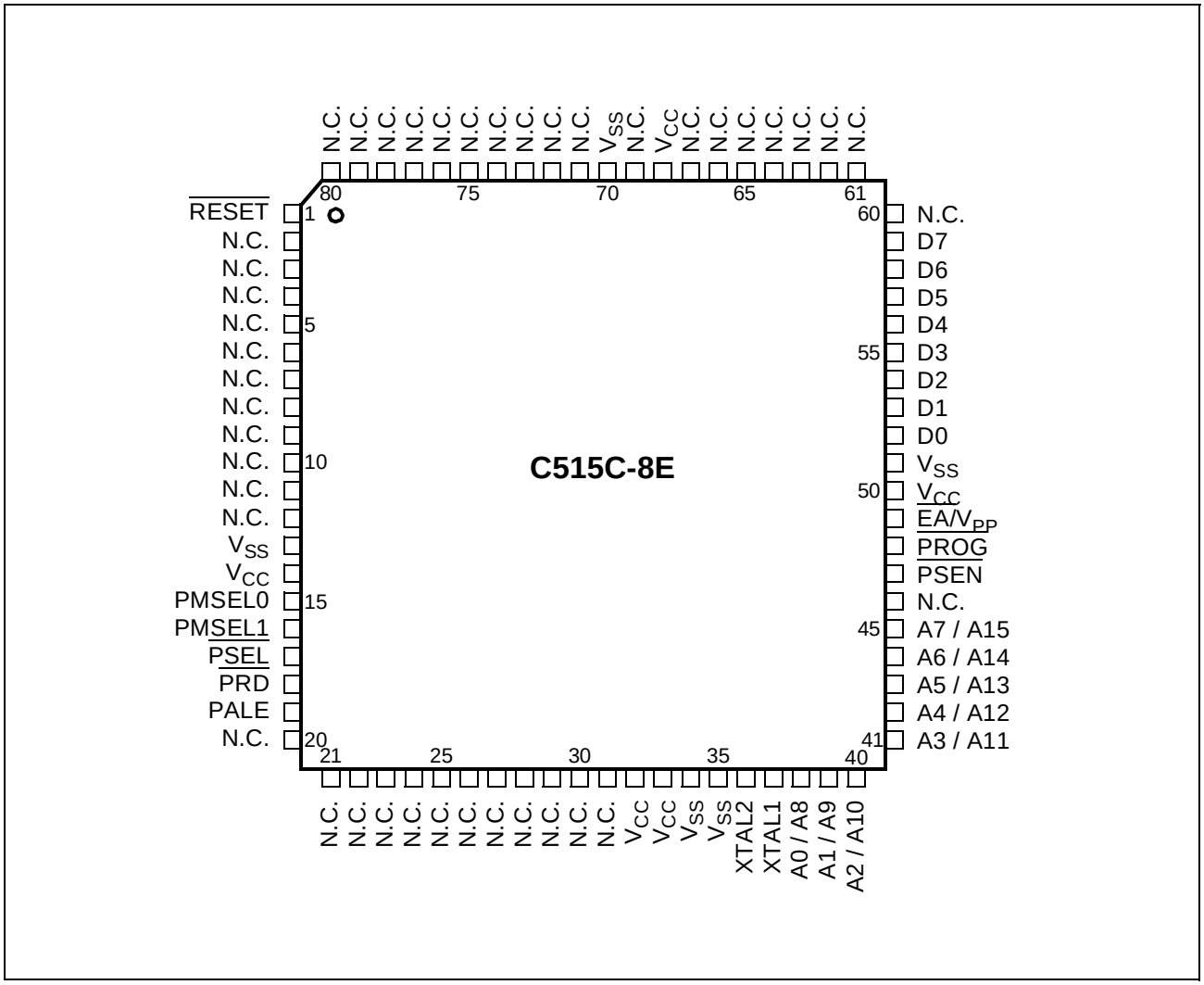


Figure 2
Pin Configuration of the C515C-8E in OTP Programming Mode (Top View)

3.2 Pin Definitions in OTP Programming Mode

The following **table 1** contains the functional description of all C515C-8E pins which are required for OTP memory programming

Table 1
Pin Definitions and Functions in Programming Mode

<table>
<tr><th>Symbol</th><th>Pin Number</th><th>I/O*)</th><th>Function</th></tr>
<tr><td>$\overline{\text{RESET}}$</td><td>1</td><td>I</td><td>Reset
This input must be at static “0“ (active) level during the whole programming mode.</td></tr>
<tr><td>PMSEL0
PMSEL1</td><td>15
16</td><td>I
I</td><td>Programming mode selection pins
These pins are used to select the different access modes in programming mode. PMSEL1,0 must satisfy a setup time to the rising edge of PALE. When the logic level of PMSEL1,0 is changed, PALE must be at low level.
<table>
<tr><th>PMSEL1</th><th>PMSEL0</th><th>Access Mode</th></tr>
<tr><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>Read version bytes</td></tr>
<tr><td>1</td><td>0</td><td>Program/read lock bits</td></tr>
<tr><td>1</td><td>1</td><td>Program/read OTP memory byte</td></tr>
</table></td></tr>
<tr><td>$\overline{\text{PSEL}}$</td><td>17</td><td>I</td><td>Basic programming mode select
This input is used for the basic programming mode selection and must be switched according figure 3.</td></tr>
<tr><td>$\overline{\text{PRD}}$</td><td>18</td><td>I</td><td>Programming mode read strobe
This input is used for read access control for OTP memory read, version byte read, and lock bit read operations.</td></tr>
<tr><td>PALE</td><td>19</td><td>I</td><td>Programming address latch enable
PALE is used to latch the high address lines. The high address lines must satisfy a setup and hold time to/from the falling edge of PALE. PALE must be at low level whenever the logic level of PMSEL1,0 is changed.</td></tr>
<tr><td>XTAL2</td><td>36</td><td>I</td><td>XTAL2
Input to the oscillator amplifier.</td></tr>
<tr><td>XTAL1</td><td>37</td><td>O</td><td>XTAL1
Output of the inverting oscillator amplifier.</td></tr>
<tr><td>A0/A8 -
A7/A15</td><td>38 - 45</td><td>I</td><td>Address lines
P2.0-7 are used as multiplexed address input lines A0-A7 and A8-A15. A8-A15 must be latched with PALE.</td></tr>
</table>

*) I = Input
O = Output

Table 1
Pin Definitions and Functions in Programming Mode (cont'd)

Symbol	Pin Number	I/O*)	Function
$\overline{\text{PSEN}}$	47	I	**$\overline{\text{Program store enable}}$** This input must be at static "0" level during the whole programming mode.
$\overline{\text{PROG}}$	48	I	**$\overline{\text{Programming mode write strobe}}$** This input is used in programming mode as a write strobe for OTP memory program and lock bit write operations. During basic programming mode selection a low level must be applied to $\overline{\text{PROG}}$.
$\overline{\text{EA}}/V_{PP}$	49	I	**$\overline{\text{External Access}}$ / Programming voltage** This pin must be at 11.5 V (V_{PP}) voltage level during programming of an OTP memory byte or lock bit. During an OTP memory read operation this pin must be at high level (V_{IH}). This pin is also used for basic programming mode selection. At basic programming mode selection a low level must be applied to $\overline{\text{EA}}/V_{PP}$.
D0 - 7	52 - 58	I/O	**Data lines 0-7** During programming mode, data bytes are read or written from or to the C515C-8E via the bidirectional D0-7 which are located at port 0.
V_{SS}	13, 34, 35, 51, 70	–	**Circuit ground potential** must be applied to these pins in programming mode.
V_{CC}	14, 32, 33, 50, 69	–	**Power supply terminal** must be applied to these pins in programming mode.
N.C.	2-12, 20-31, 46, 60-67, 69, 71-80	–	**Not Connected** These pins should not be connected in programming mode.

*) I = Input
O = Output

4 Programming Mode Selection

The selection for the OTP programming mode can be separated into two different parts :

- Basic programming mode selection
- Access mode selection

With the basic programming mode selection the device is put into the mode in which it is possible to access the OTP memory through the programming interface logic. Further, after selection of the basic programming mode, OTP memory accesses are executed by using one of the access modes. These access modes are OTP memory byte program/read, version byte read, and program/read lock byte operations.

4.1 Basic Programming Mode Selection

The basic programming mode selection scheme is shown in **figure 3**.

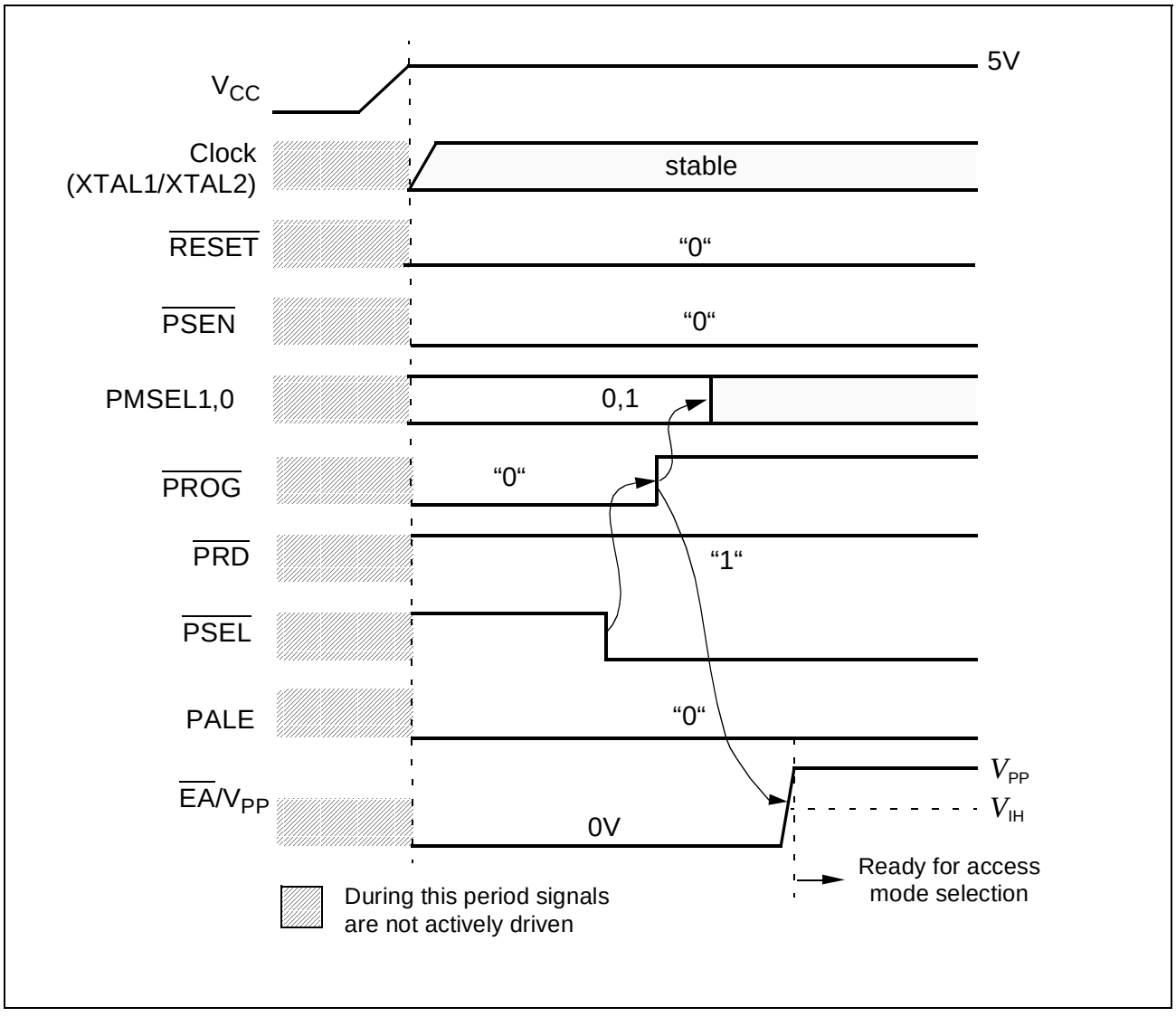


Figure 3
Basic Programming Mode Selection

The basic programming mode is selected by executing the following steps :

- With a stable V_{CC} and a clock signal applied to the XTAL pins; the $\overline{\text{RESET}}$ and $\overline{\text{PSEN}}$ pins are set to “0“ level.
- $\overline{\text{PROG}}$, PALE, PMSEL1 and $\overline{\text{EA}}/V_{PP}$ are set to “0“ level; $\overline{\text{PRD}}$, $\overline{\text{PSEL}}$, and PMSEL0 are set to “1“ level.
- $\overline{\text{PSEL}}$ is set to from “1“ to “0“ level and thereafter $\overline{\text{PROG}}$ is switched to “1“ level.
- PMSEL1,0 can now be changed; after $\overline{\text{EA}}/V_{PP}$ has been set to V_{IH} high level or to V_{PP} the OTP memory is ready for access.

The pins $\overline{\text{RESET}}$ and $\overline{\text{PSEN}}$ must stay at static “0“ signal level during the whole programming mode. With a falling edge of $\overline{\text{PSEL}}$ the logic state of $\overline{\text{PROG}}$ and $\overline{\text{EA}}/V_{PP}$ is internally latched. These two signals are now used as programming write pulse signal ($\overline{\text{PROG}}$) and as programming voltage input pin V_{PP}. After the falling edge of $\overline{\text{PSEL}}$, $\overline{\text{PSEL}}$ must stay at “0“ state during all programming operations.

4.2 OTP Memory Access Mode Selection

When the C515C-8E has been put into the programming mode using the basic programming mode selection, several access modes of the OTP memory programming interface are available. The conditions for the different control signals of these access modes are listed in **table 2**.

Table 2
Access Modes Selection

Access Mode	$\overline{\text{EA}}/V_{PP}$	$\overline{\text{PROG}}$	$\overline{\text{PRD}}$	PMSEL		Address (Port 2)	Data (Port 0)
				1	0		
Program OTP memory byte	V_{PP}	⊓	H	H	H	A0-7 A8-15	D0-7
Read OTP memory byte	V_{IH}	H	⊓				
Program OTP lock bits	V_{PP}	⊓	H	H	L	–	D1,D0 see **table 3**
Read OTP lock bits	V_{IH}	H	⊓				
Read OTP version byte	V_{IH}	H	⊓	L	H	Byte addr. of sign. byte	D0-7

The access modes from the table above are basically selected by setting the two PMSEL1,0 lines to the required logic level. The $\overline{\text{PROG}}$ and $\overline{\text{PRD}}$ signal are the write and read strobe signal. Data is transferred via port 0 and addresses are applied to port 2.

The following sections describe the details of the different access modes.

4.2.1 Program / Read OTP Memory Bytes

The program/read OTP memory byte access mode is defined by PMSEL1,0 = 1,1. It is initiated when the PMSEL1,0 = 1,1 is valid at the rising edge of PALE. With the falling edge of PALE the upper addresses A8-A15 of the 16-bit OTP memory address are latched. After A8-A15 has been latched, A0-A7 is put on the address bus (port 2). A0-A7 must be stable when $\overline{PROG}$ is low or $\overline{PRD}$ is low. If subsequent OTP address locations are accessed with constant address information at the high address lines A8-15, A8-A15 must only be latched once (page address mechanism).

Figure 4 shows a typical OTP memory programming cycle with a following OTP memory read operation. In this example A0-A15 of the read operation are identical to A8-A15 of the preceeding programming operation.

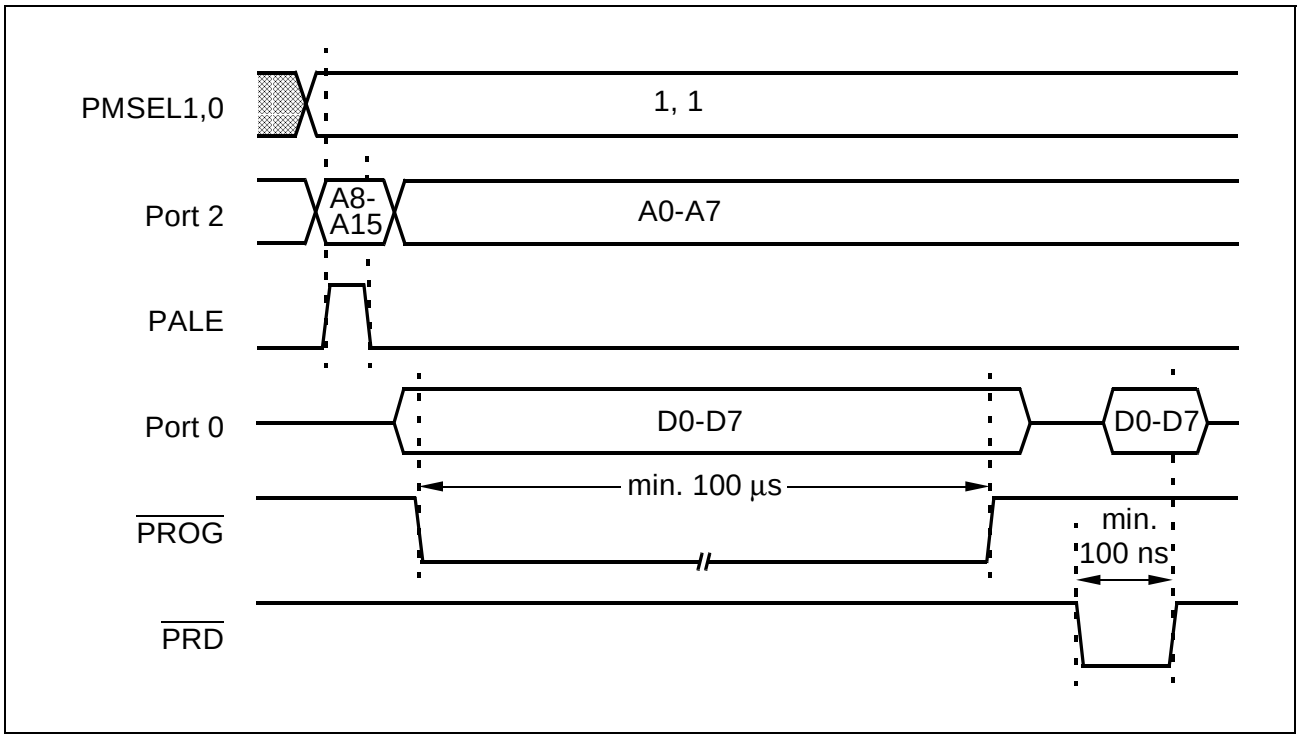


Figure 4
Programming / Verify OTP Memory Access Waveform

If the address lines A8-A15 must be updated, PALE must be activated for the latching of the new A8-A15 value. Control, address, and data information must only be switched when the $\overline{PROG}$ and $\overline{PRD}$ signals are at high level. The PALE high pulse must always be executed if a different access mode has been used prior to the actual access mode.

Figure 5 shows a waveform example of the program/read mode access for several OTP memory bytes. In this example OTP memory locations $3FD_H$ to 400_H are programmed. Thereafter, OTP memory locations 400_H and $3FD_H$ are read.

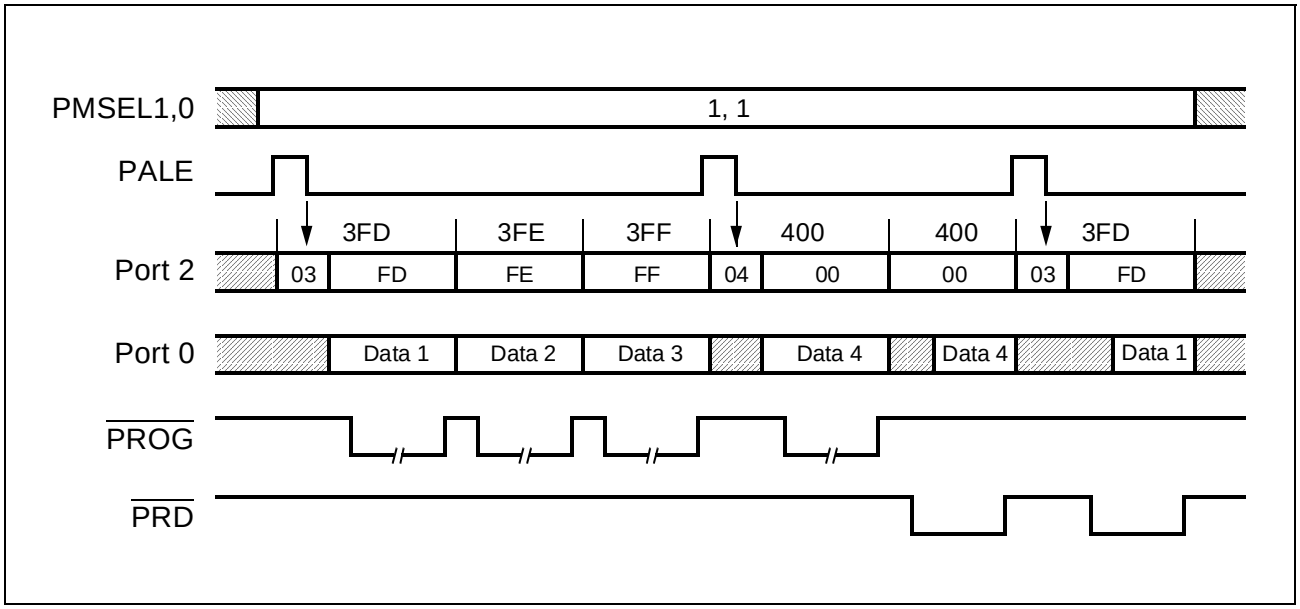


Figure 5
Typical OTP Memory Programming/Verify Access Waveform

4.2.2 Lock Bits Programming / Read

The C515C-8E has two programmable lock bits which, when programmed according **table 3**, provide four levels of protection for the on-chip OTP code memory. The state of the lock bits can also be read.

Table 3
Lock Bit Protection Types

Lock Bits at D1,D0		Protection Level	Protection Type
D1	**D0**		
1	1	Level 0	The OTP lock feature is disabled. During normal operation of the C515C-8E, the state of the $\overline{EA}$ pin is not latched on reset.
1	0	Level 1	During normal operation of the C515C-8E, MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset. An OTP memory read operation is only possible according to ROM verification mode 2, as it is defined for a protected ROM version of the C515C-8R (see OTP verification mode 2 on page 27). Further programming of the OTP memory is disabled (reprogramming security).
0	1	Level 2	Same as level 1, but also OTP memory read operation using ROM verification mode 2 is disabled.
0	0	Level 3	Same as level 2; but additionally external code execution by setting $\overline{EA}$=low during normal operation of the C515C-8E is no more possible. External code execution, which is initiated by an internal program (e.g. by an internal jump instruction above the ROM boundary), is still possible.

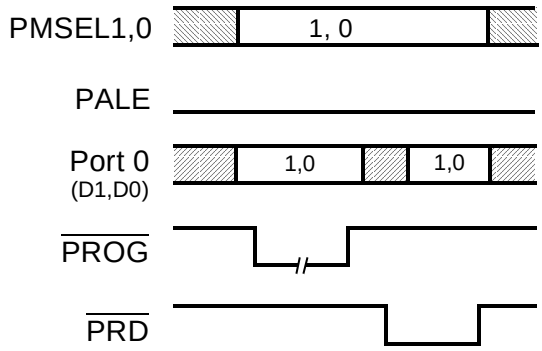
Note : A 1 means that the lock bit is unprogrammed. 0 means that lock bit is programmed.

For a OTP verify operation at protection level 1, the C515C-8E must be put into the ROM verification mode 2. This mode is selected as defined in the C515C User' Manual 08.96 at pages 4-11 and 4-12.

If a device is programmed with protection level 2 or 3, it is no more possible to verify the OTP content of a customer rejected (FAR) OTP device.

When a protection level has been activated by programming of the lock bits, the basic programming mode must be left for activation of the protection mechanisms. This means, after the activation of a protection level further OTP program/verify operations are still possible if the basic programming mode is maintained.

Figure 6 shows the waveform of a lock bit write/read access. For a simple drawing, the $\overline{PROG}$ pulse is shortened. In reality, for Lock Bit programming, a 100µs $\overline{PROG}$ low puls must be applied.



The example shows the programming and reading of a protection level 1.

Figure 6
Write/Read Lock Bit Waveform

4.2.3 Access of Version Bytes

The C515C-8E provides three version bytes at address locations FC_H, FD_H, and FE_H. The information stored in the version bytes, is defined by the mask of each microcontroller step, Therefore, the version bytes can be read but not written. The three version bytes hold information as manufacturer code, device type, and stepping code.

For reading of the version bytes the control lines must be used according **table 2** and **figure 7**. The address of the version byte must be applied at the port 1 address lines. PALE must not be activated.

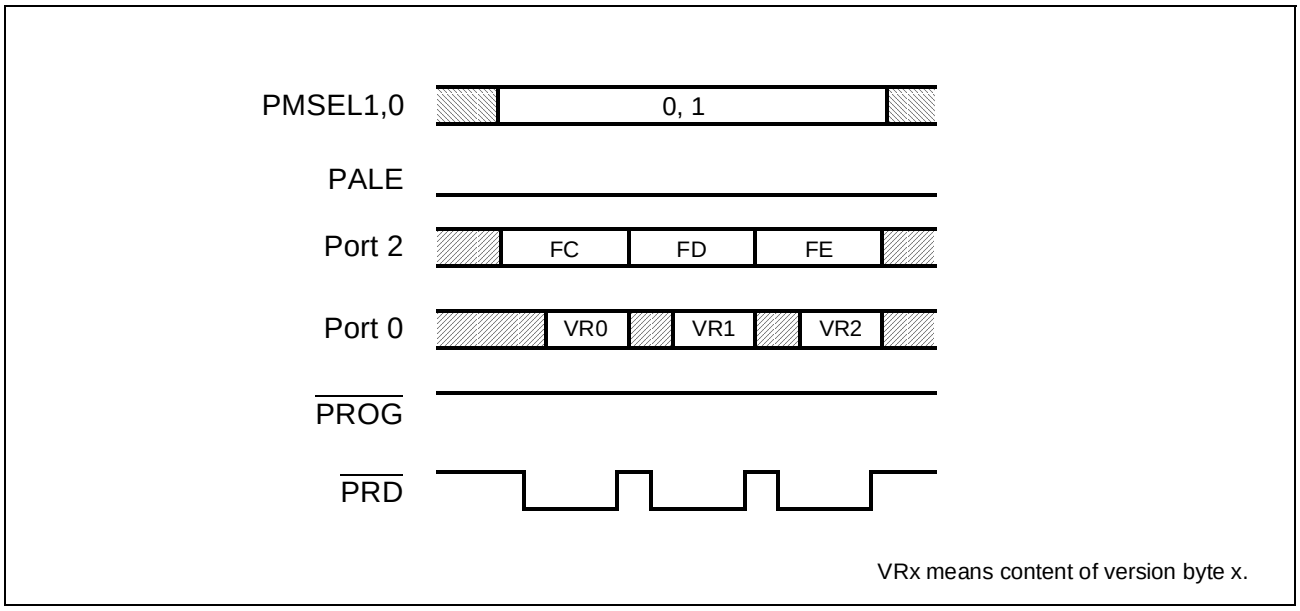


Figure 7
Read Version Byte(s) Waveform

Version bytes are typically used by programming systems for adapting the programming firmware to specifc device characteristics such as OTP size etc.

Note: The 3 version bytes are implemented in a way that they can be also read during normal program execution mode as a mapped SFR when bit RMAP in SFR SYSCON is set. The SFR addresses of the version bytes in normal mode are identical to the addresses which are used in programming mode. Therefore, in normal operating mode of the C515C-8E, the SFR locations which hold the signature bytes are also referenced as version registers.

The first step of the C515C-8E will contain the following information at the signature bytes :

Name	Address	Value
Version Byte 0 = Version Register 0	FC_H	$C5_H$
Version Byte 1 = Version Register 1	FD_H	95_H
Version Byte 2 = Version Register 2	FE_H	01_H

Future steppings of the C515C-8E will typically have a different version byte 2 (incremented value).

5 Device Specifications

5.1 Absolute Maximum Ratings

Ambient temperature under bias (T_A) ..... 0 °C to + 110 °C
Storage temperature (T_{ST}).....– 65 °C to + 150 °C

Voltage on V_{CC} pins with respect to ground (V_{SS}) .....– 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS}).....– 0.5 V to V_{CC} + 0.5 V

Input current on any pin during overload condition.....– 10 mA to + 10 mA
Absolute sum of all input currents during overload condition .....| 100 mA |

Power dissipation.....TBD

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

5.2 DC Characteristics

V_{CC} = 5 V + 10%, – 15%; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB-C515C-8E
T_A = – 40 to 85 °C for the SAF-C515C-8E
T_A = – 40 to 110 °C for the SAH-C515C-8E

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltages					
all exc. $\overline{EA}$/V_{PP}, $\overline{RESET}$, $\overline{HWPD}$	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
$\overline{EA}$/V_{PP} pin	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
$\overline{RESET}$ and $\overline{HWPD}$ pins	V_{IL2}	– 0.5	0.2 V_{CC} + 0.1	V	–
Port 5 in CMOS mode	V_{ILC}	– 0.5	0.3 V_{CC}	V	–
Input high voltages					
all except XTAL2, $\overline{RESET}$, and $\overline{HWPD}$)	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
XTAL2 pin	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	–
$\overline{RESET}$ and $\overline{HWPD}$ pins	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–
Port 5 in CMOS mode	V_{IHC}	0.7 V_{CC}	V_{CC} + 0.5	V	–
Output low voltages					
Ports 1, 2, 3, 4, 5, 7 (incl. CMOS)	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA [1]
Port 0, ALE, $\overline{PSEN}$, $\overline{CPUR}$	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA [1]
P4.1, P4.3 in push-pull mode	V_{OL3}	–	0.45	V	I_{OL} = 3.75 mA [1]
Output high voltages					
Ports 1, 2, 3, 4, 5, 7	V_{OH}	2.4	–	V	I_{OH} = – 80 µA
		0.9 V_{CC}	–	V	I_{OH} = – 10 µA []
Port 0 in external bus mode,	V_{OH2}	2.4	–	V	I_{OH} = – 800 µA [2]
ALE, $\overline{PSEN}$, $\overline{CPUR}$		0.9 V_{CC}	–	V	I_{OH} = – 80 µA [2]
Port 5 in CMOS mode	V_{OHC}	0.9 V_{CC}	–	V	I_{OH} = – 800 µA
P4.1, P4.3 in push-pull mode	V_{OH3}	0.9 V_{CC}	–	V	I_{OH} = – 833 µA
Logic 0 input current					
Ports 1, 2, 3, 4, 5, 7	I_{IL}	– 10	– 70	µA	V_{IN} = 0.45 V
Logical 0-to-1 transition current	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Ports 1, 2, 3, 4, 5, 7					
Input leakage current Port 0,					
$\overline{EA}$/V_{PP}, P6, $\overline{HWPD}$, AIN0-7	I_{LI}	–	± 1	µA	0.45 < V_{IN} < V_{CC}
Input low current					
To $\overline{RESET}$ for reset	I_{LI2}	–	– 100	µA	V_{IN} = 0.45 V
XTAL2	I_{LI3}	–	– 15	µA	V_{IN} = 0.45 V
$\overline{PE}$/SWD	I_{LI4}	–	– 20	µA	V_{IN} = 0.45 V
Pin capacitance	C_{IO}	–	10	pF	f_c = 1 MHz, T_A = 25 °C
Overload current	I_{OV}	–	± 5	mA	[7] [8]
Programming voltage	V_{PP}	10.9	12.1	V	11.5 V ± 5%

Parameter	Symbol	Limit Values		Unit	Test Condition
		typ. [9]	max.		
Power supply current:					
Active mode, 6 MHz [6]	I_{CC}	TBD	TBD	mA	V_{CC} = 5 V, [4]
Idle mode, 6 MHz [6]	I_{CC}	TBD	TBD	mA	V_{CC} = 5 V, [5]
Active mode, 10 MHz [6]	I_{CC}	TBD	TBD	mA	V_{CC} = 5 V, [4]
Idle mode, 10 MHz [6]	I_{CC}	TBD	TBD	mA	V_{CC} = 5 V, [5]
Power-down mode	I_{PD}	–	50	µA	V_{CC} = 2…5.5 V [3]
Power supply current at $\overline{EA}/V_{PP}$ in programming mode	I_{CCP}	–	30	mA	

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address lines are stabilizing.

3) I_{PD} (power-down mode) is measured under following conditions:
EA = $\overline{RESET}$ = Port 0 = Port 6 = V_{CC} ; XTAL1 = N.C.; XTAL2 = V_{SS} ; $\overline{PE}$/SWD = V_{SS} ; $\overline{HWPD}$ = V_{CC} ; V_{AGND} = V_{SS} ; V_{AREF} = V_{CC} ; all other pins are disconnected.
I_{PD} (hardware power-down mode) is independent of any particular pin connection.

4) I_{CC} (active mode) is measured with:
XTAL2 driven with t_{CLCH} , t_{CHCL} = 5 ns , V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL1 = N.C.;
EA = PE/SWD = Port 0 = Port 6 = V_{CC} ; HWPD = V_{CC} ; $\overline{RESET}$ = V_{SS} ; all other pins are disconnected.

5) I_{CC} (idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL2 driven with t_{CLCH} , t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL1 = N.C.;
$\overline{RESET}$ = V_{CC} ; EA = V_{SS} ; Port0 = V_{CC} ; all other pins are disconnected;

6) $I_{CC\ max}$ at other frequencies is given by:
active mode: TBD
idle mode: TBD
where f_{osc} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V.

7) Overload conditions occur if the standard operating conditions are exceeded, ie. the voltage on any pin exceeds the specified range (i.e. V_{OV} > V_{CC} + 0.5 V or V_{OV} < V_{SS} - 0.5 V). The supply voltage V_{CC} and V_{SS} must remain within the specified limits. The absolute sum of input currents on all port pins may not exceed 50 mA.

8) Not 100% tested, guaranteed by design characterization

9) The typical I_{CC} values are periodically measured at T_A = +25 °C but not 100% tested.

5.3 A/D Converter Characteristics

V_{CC} = 5 V + 10%, – 15%; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB-C515C-8E
T_A = – 40 to 85 °C for the SAF-C515C-8E
T_A = – 40 to 110 °C for the SAH-C515C-8E

4 V ≤ V_{AREF} ≤ V_{CC}+0.1 V ; V_{SS}-0.1 V ≤ V_{AGND} ≤ V_{SS}+0.2 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	1)
Sample time	t_S	–	16 x t_{IN} 8 x t_{IN}	ns	Prescaler ÷ 8 Prescaler ÷ 4 2)
Conversion cycle time	t_{ADCC}	–	96 x t_{IN} 48 x t_{IN}	ns	Prescaler ÷ 8 Prescaler ÷ 4 3)
Total unadjusted error	T_{UE}	–	± 2	LSB	V_{SS}+0.5V ≤ V_{IN} ≤ V_{CC}-0.5V 4)
Internal resistance of reference voltage source	R_{AREF}	–	t_{ADC} / 250 - 0.25	kΩ	t_{ADC} in [ns] 5) 6)
Internal resistance of analog source	R_{ASRC}	–	t_S / 500 - 0.25	kΩ	t_S in [ns] 2) 6)
ADC input capacitance	C_{AIN}	–	50	pF	6)

Notes see next page.

Clock calculation table :

Clock Prescaler Ratio	ADCL	t_{ADC}	t_S	t_{ADCC}
÷ 8	1	8 x t_{IN}	16 x t_{IN}	96 x t_{IN}
÷ 4	0	4 x t_{IN}	8 x t_{IN}	48 x t_{IN}

Further timing conditions : t_{ADC} min = 500 ns
t_{IN} = 1 / f_{OSC} = t_{CLP}

Notes:

1) V_{AIN} may exeed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

2) During the sample time the input capacitance C_{AIN} can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

3) This parameter includes the sample time t_S, the time for determining the digital result and the time for the calibration. Values for the conversion clock t_{ADC} depend on programming and can be taken from the table on the previous page.

4) T_{UE} is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{CC} = 4.9 V. It is guaranteed by design characterization for all other voltages within the defined voltage range.
If an overload condition occurs on maximum 2 not selected analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA, an additional conversion error of 1/2 LSB is permissible.

5) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference source must allow the capacitance to reach their final voltage level within the indicated time. The maximum internal resistance results from the programmed conversion timing.

6) Not 100% tested, but guaranteed by design characterization.

5.4 AC Characteristics

V_{CC} = 5 V + 10%, – 15%; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB-C515C-8E
T_A = – 40 to 85 °C for the SAF-C515C-8E
T_A = – 40 to 110 °C for the SAH-C515C-8E

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		10-MHz clock Duty Cycle 0.4 to 0.6		Variable Clock 1/CLP = 2 MHz to 10 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	60	–	CLP - 40	–	ns
Address setup to ALE	t_{AVLL}	15	–	TCL_{Hmin} -25	–	ns
Address hold after ALE	t_{LLAX}	15	–	TCL_{Hmin} -25	–	ns
ALE to valid instruction in	t_{LLIV}	–	113	–	2 CLP - 87	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	20	–	TCL_{Lmin} -20	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	115	–	CLP+ TCL_{Hmin} -30	–	ns
$\overline{\text{PSEN}}$ to valid instruction in	t_{PLIV}	–	75	–	CLP+ TCL_{Hmin}- 65	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	30	–	TCL_{Lmin} -10	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	35	–	TCL_{Lmin} - 5	–	ns
Address to valid instruction in	t_{AVIV}	–	180	–	2 CLP + TCL_{Hmin} -60	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0		0	–	ns

*) Interfacing the C515C to devices with float times up to 35 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		10-MHz clock Duty Cycle 0.4 to 0.6		Variable Clock 1/CLP= 2 MHz to 10 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	230	–	3 CLP - 70	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	230	–	3 CLP - 70	–	ns
Address hold after ALE	t_{LLAX2}	48	–	CLP - 15	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	150	–	2 CLP+ TCL_{Hmin} - 90	ns
Data hold after $\overline{RD}$	t_{RHDX}	0		0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	80	–	CLP - 20	ns
ALE to valid data in	t_{LLDV}	–	267	–	4 CLP - 133	ns
Address to valid data in	t_{AVDV}	–	285	–	4 CLP + TCL_{Hmin} -155	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	90	190	CLP + TCL_{Lmin} - 50	CLP+ TCL_{Lmin}+ 50	ns
Address valid to $\overline{WR}$	t_{AVWL}	103	–	2 CLP - 97	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	15	65	TCL_{Hmin} - 25	TCL_{Hmin} + 25	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	TCL_{Lmin} - 35	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	218	–	3 CLP + TCL_{Lmin} - 122	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	13	–	TCL_{Hmin} - 27	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

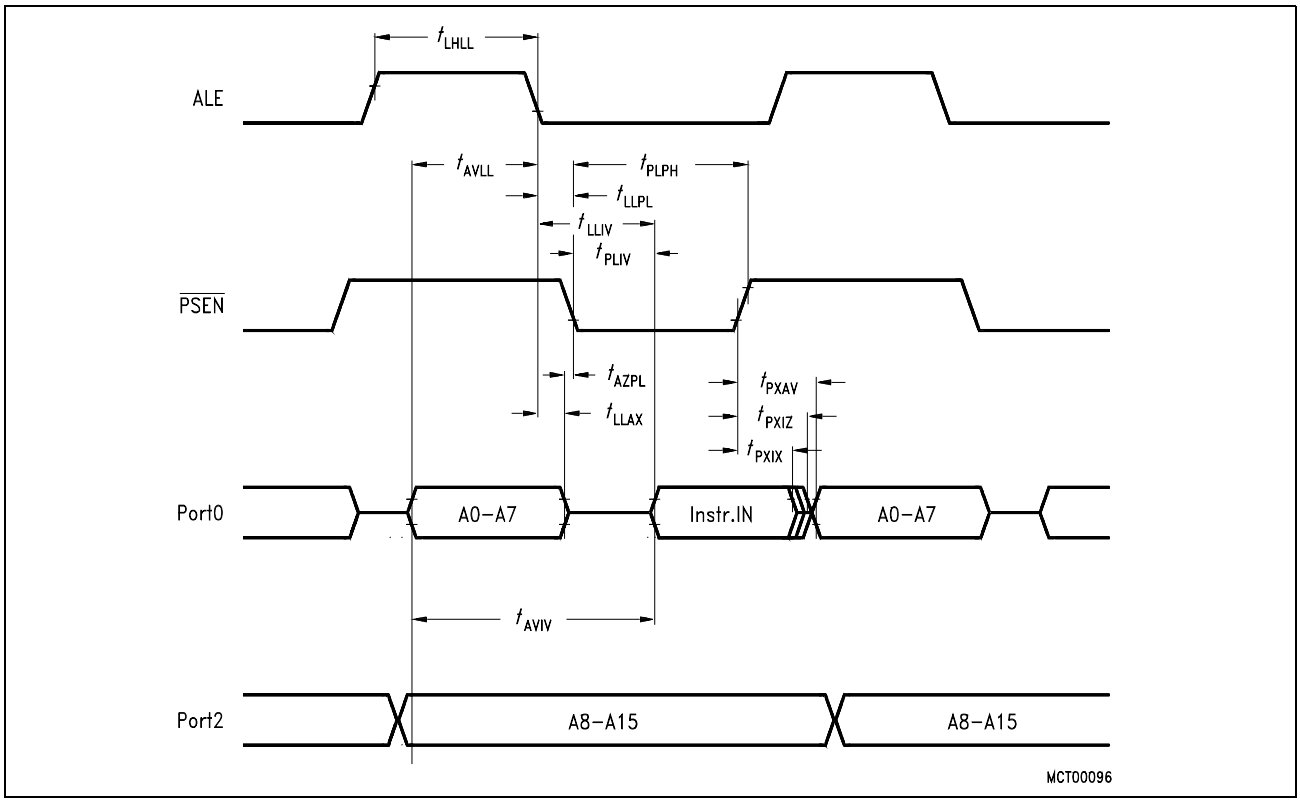
SSC Interface Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock Cycle Time : Master Mode Slave Mode	t_{SCLK} t_{SCLK}	0.8 1.0	– –	µs µs
Clock high time	t_{SCH}	360	–	ns
Clock low time	t_{SCL}	360	–	ns
Data output delay	t_{D}	–	100	ns
Data output hold	t_{HO}	0	–	ns
Data input setup	t_{S}	100	–	ns
Data input hold	t_{HI}	100	–	ns
TC bit set delay	t_{DTC}	–	8 CLP	ns

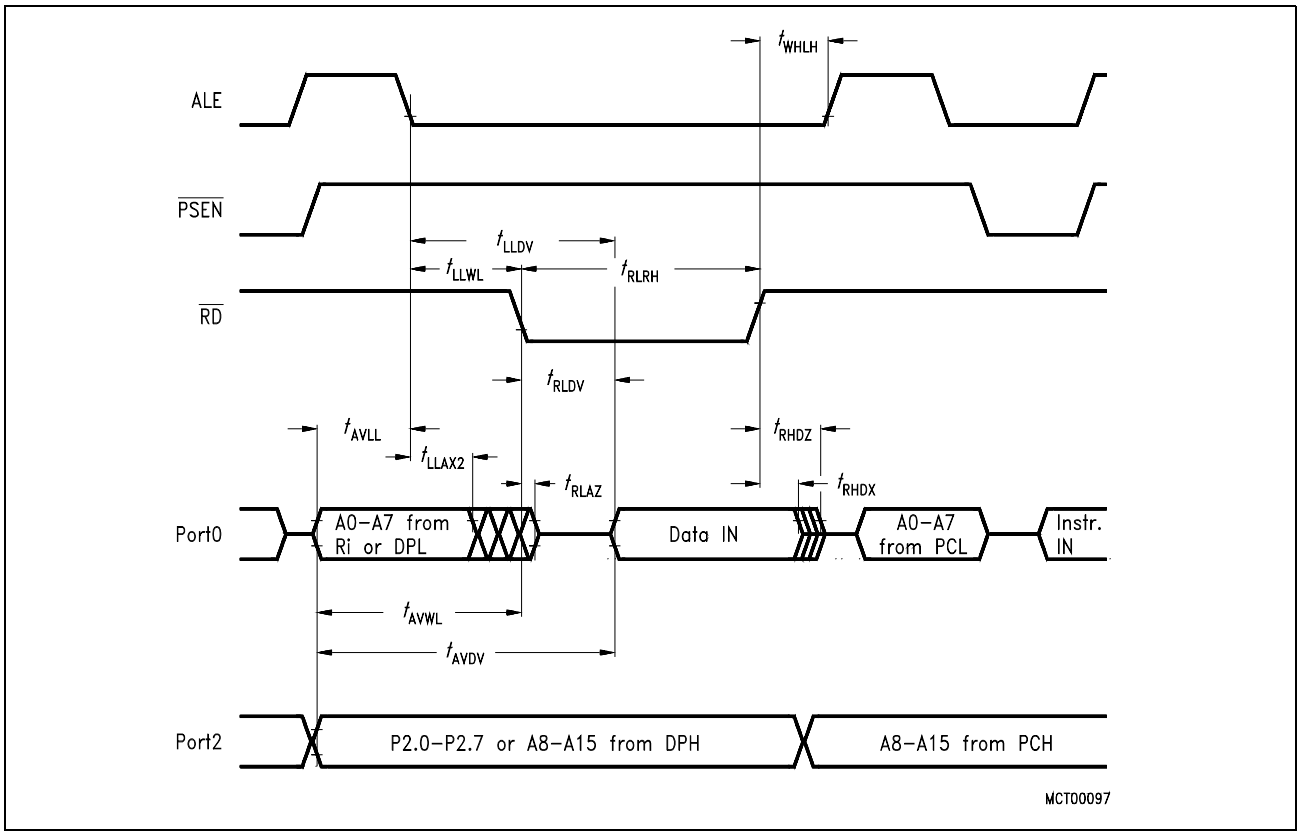
External Clock Drive at XTAL2

Parameter	Symbol	CPU Clock = 10 MHz Duty cycle 0.4 to 0.6		Variable CPU Clock 1/CLP = 2 to 10 MHz		Unit
		min.	max.	min.	max.	
Oscillator period	CLP	100	100	100	500	ns
High time	TCL_H	40	–	40	$CLP-TCL_L$	ns
Low time	TCL_L	40	–	40	$CLP-TCL_H$	ns
Rise time	t_R	–	12	–	12	ns
Fall time	t_F	–	12	–	12	ns
Oscillator duty cycle	DC	0.4	0.6	40 / CLP	1 - 40 / CLP	–
Clock cycle	TCL	40	60	$CLP * DC_{min}$	$CLP * DC_{max}$	ns

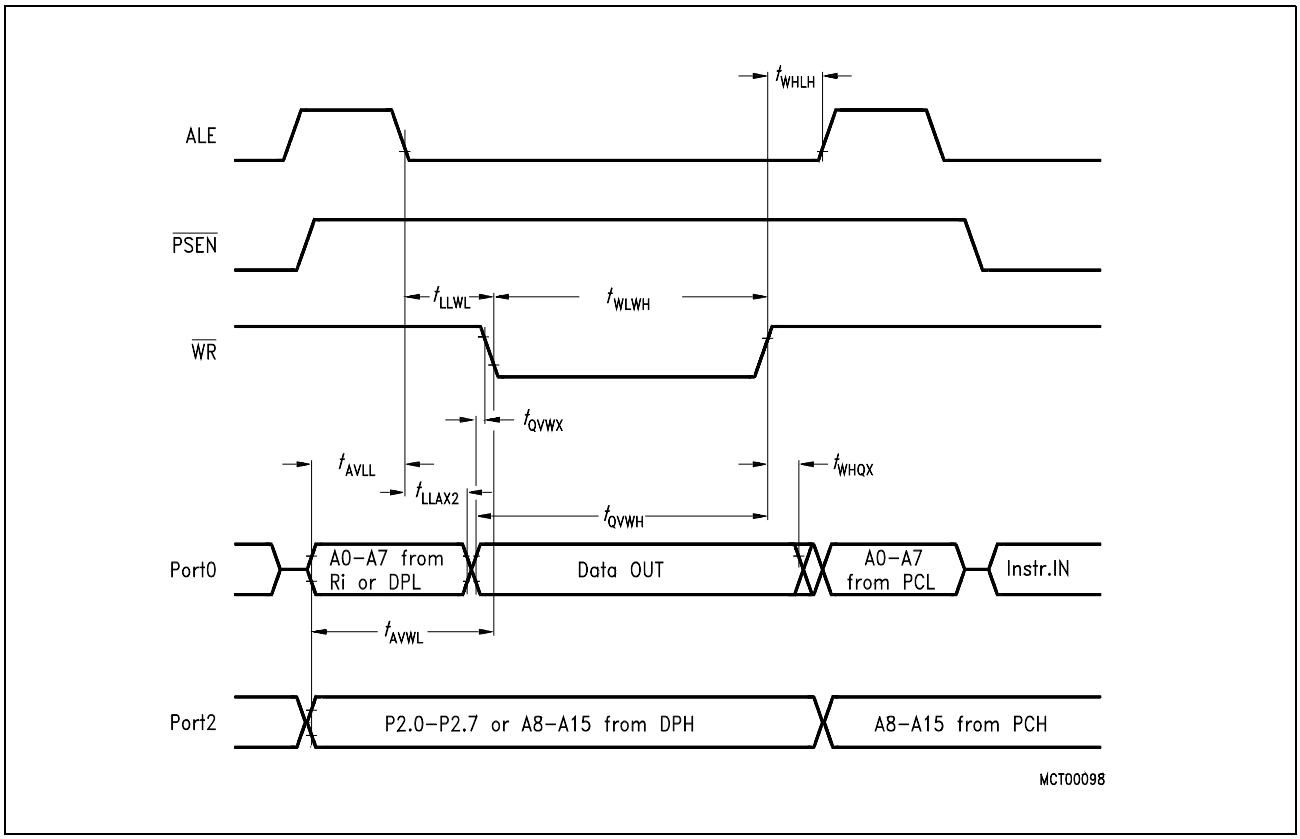
Note: The 10 MHz values in the tables are given as an example for a typical duty cycle variation of the oscillator clock from 0.4 to 0.6.



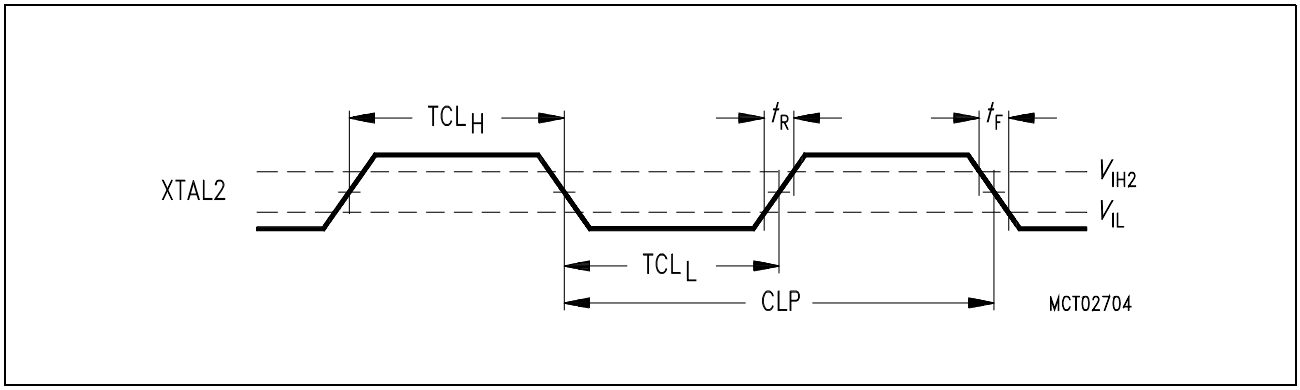
Program Memory Read Cycle



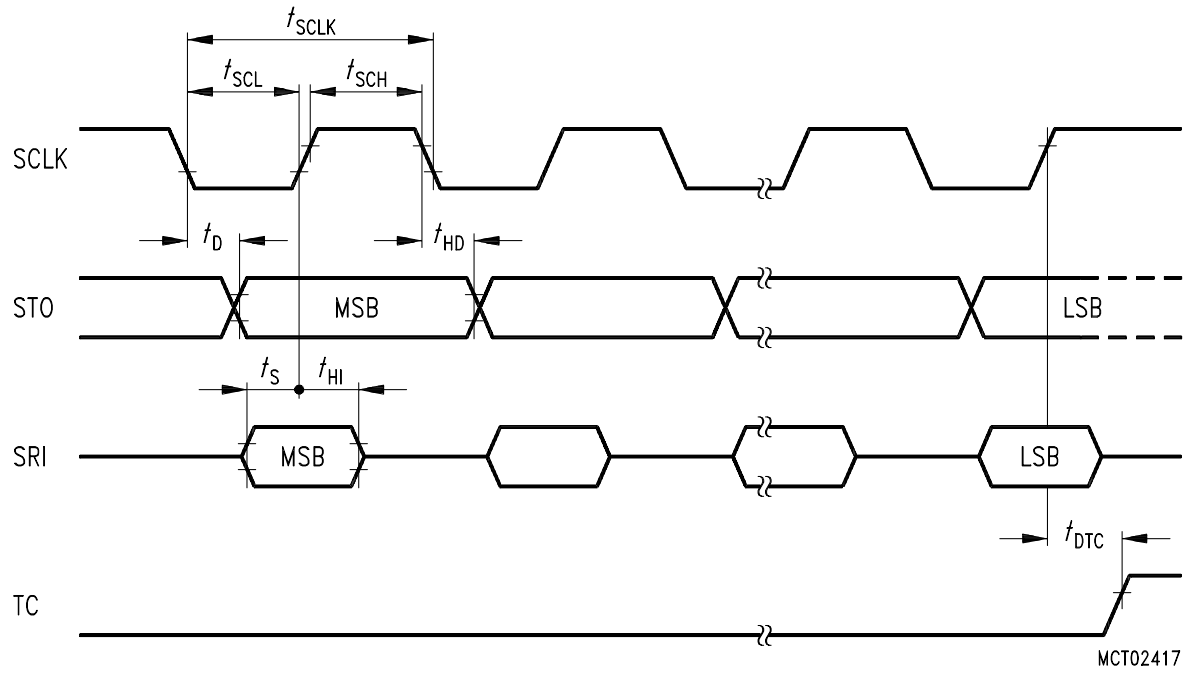
Data Memory Read Cycle



Data Memory Write Cycle



External Clock Cycle



Notes : Shown is the data/clock relationship for CPOL=CPHA=1. The timing diagram is valid for the other cases accordingly.

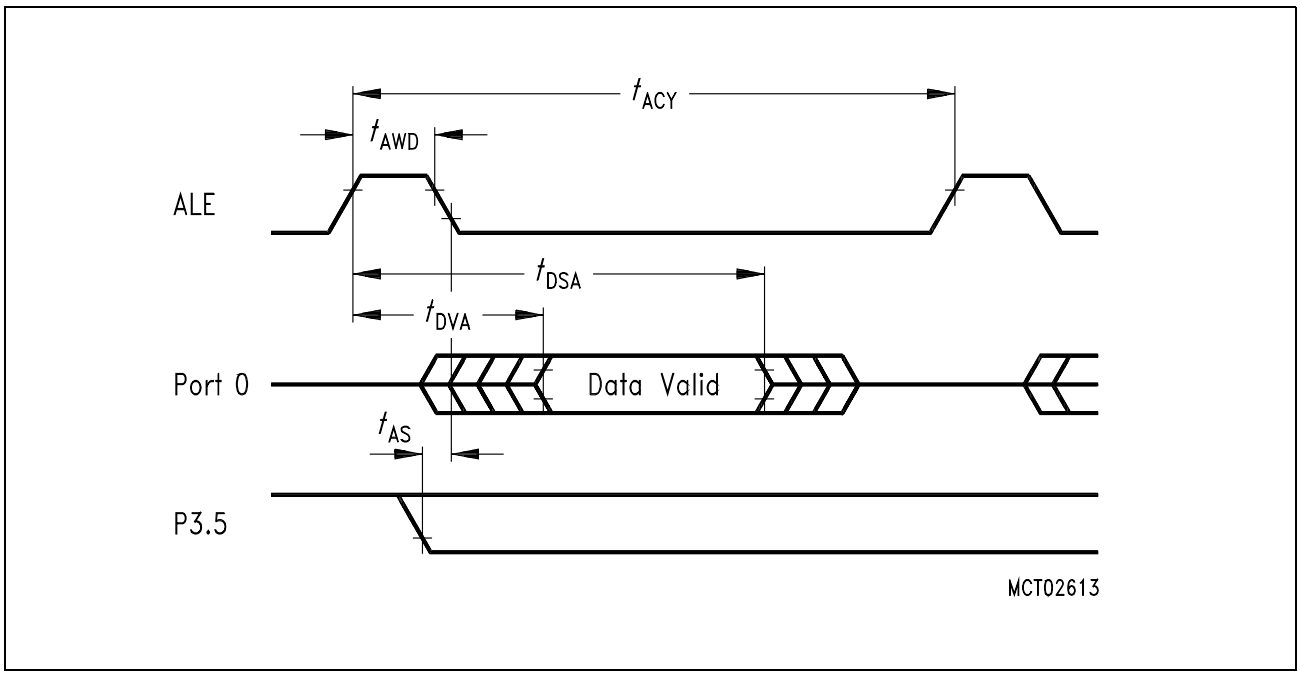
In the case of slave mode and CPHA=0, the output delay for the MSB applies to the falling edge of $\overline{SLS}$ (if transmitter is enabled).

In the case of master mode and CPHA=0, the MSB becomes valid after the data has been written into the shift register, i.e. at least one half SCLK clock cycle before the first clock transition.

SSC Timing

OTP Verification Mode 2 (for Memory Verification in OTP Protection Level 1)

Parameter	Symbol	Limit Values			Unit
		min.	typ	max.	
ALE pulse width	t_{AWD}	–	CLP	–	ns
ALE period	t_{ACY}	–	6 CLP	–	ns
Data valid after ALE	t_{DVA}	–	–	2 CLP	ns
Data stable after ALE	t_{DSA}	4 CLP	–	–	ns
P3.5 setup to ALE low	t_{AS}	–	t_{CL}	–	ns
Oscillator frequency	1/ CLP	4	–	6	MHz



ROM/OTP Verification Mode 2

5.5 OTP Memory Programming Mode Characteristics

V_{CC} = 5 V ± 10 %; V_{PP} = 11.5 V ± 5 %; T_A = 25 °C ± 10 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{PAW}	35	–	ns
PMSEL setup to ALE rising edge	t_{PMS}	10	–	
Address setup to ALE, $\overline{PROG}$, or $\overline{PRD}$ falling edge	t_{PAS}	10	–	ns
Address hold after ALE, $\overline{PROG}$, or $\overline{PRD}$ falling edge	t_{PAH}	10	–	ns
Address, data setup to $\overline{PROG}$ or $\overline{PRD}$	t_{PCS}	100	–	ns
Address, data hold after $\overline{PROG}$ or $\overline{PRD}$	t_{PCH}	0	–	ns
PMSEL setup to $\overline{PROG}$ or $\overline{PRD}$	t_{PMS}	10	–	ns
PMSEL hold after $\overline{PROG}$ or $\overline{PRD}$	t_{PMH}	10	–	ns
$\overline{PROG}$ pulse width	t_{PWW}	100	–	µs
$\overline{PRD}$ pulse width	t_{PRW}	100	–	ns
Address to valid data out	t_{PAD}	–	75	ns
$\overline{PRD}$ to valid data out	t_{PRD}	–	20	ns
Data hold after $\overline{PRD}$	t_{PDH}	0	–	ns
Data float after $\overline{PRD}$	t_{PDF}	–	20	ns
$\overline{PROG}$ high between two consecutive $\overline{PROG}$ low pulses	t_{PWH1}	1	–	µs
$\overline{PRD}$ high between two consecutive $\overline{PRD}$ low pulses	t_{PWH2}	100		ns
XTAL clock period	t_{CLKP}	TBD		ns

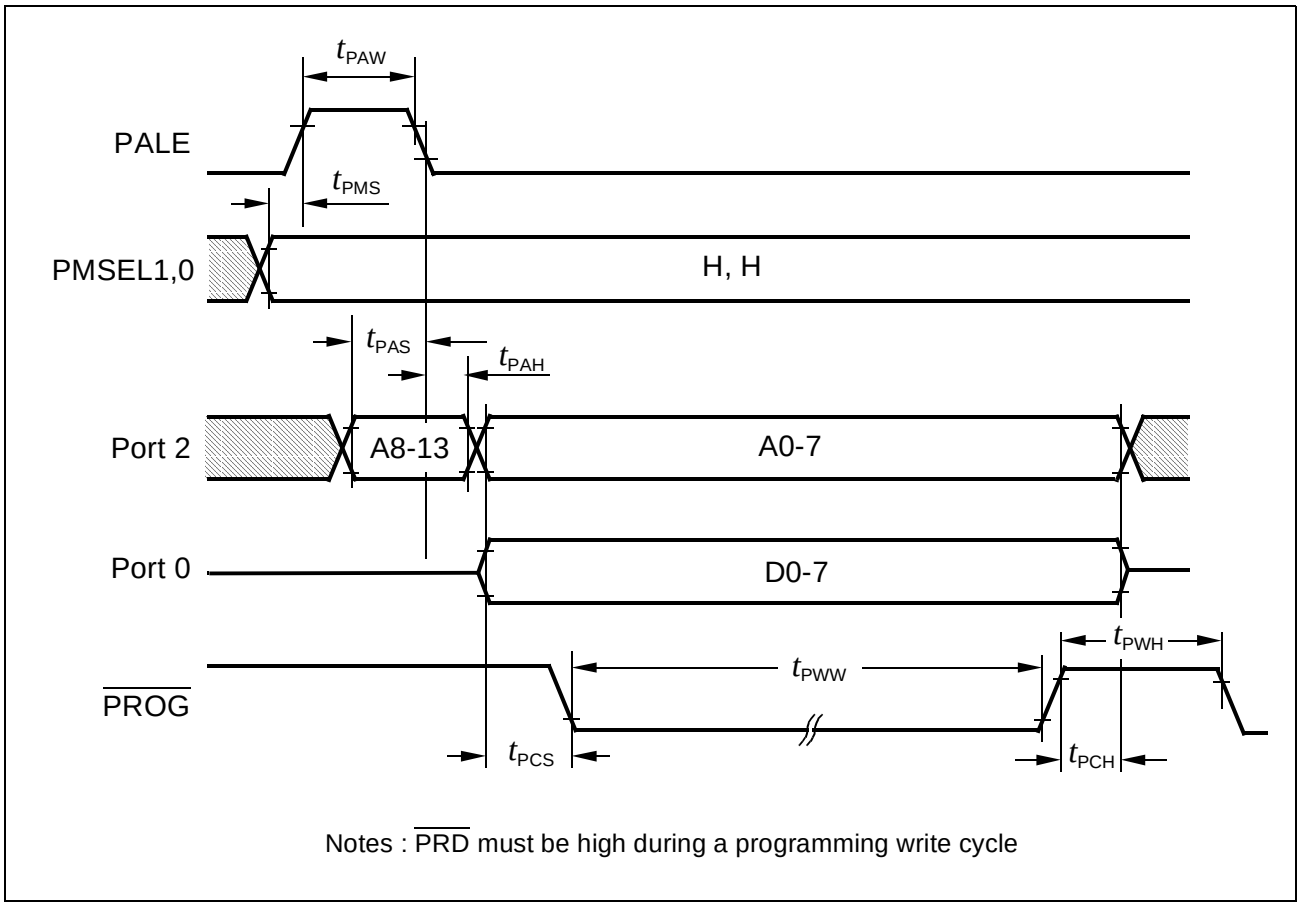


Figure 8
Programming Code Byte - Write Cycle Timing

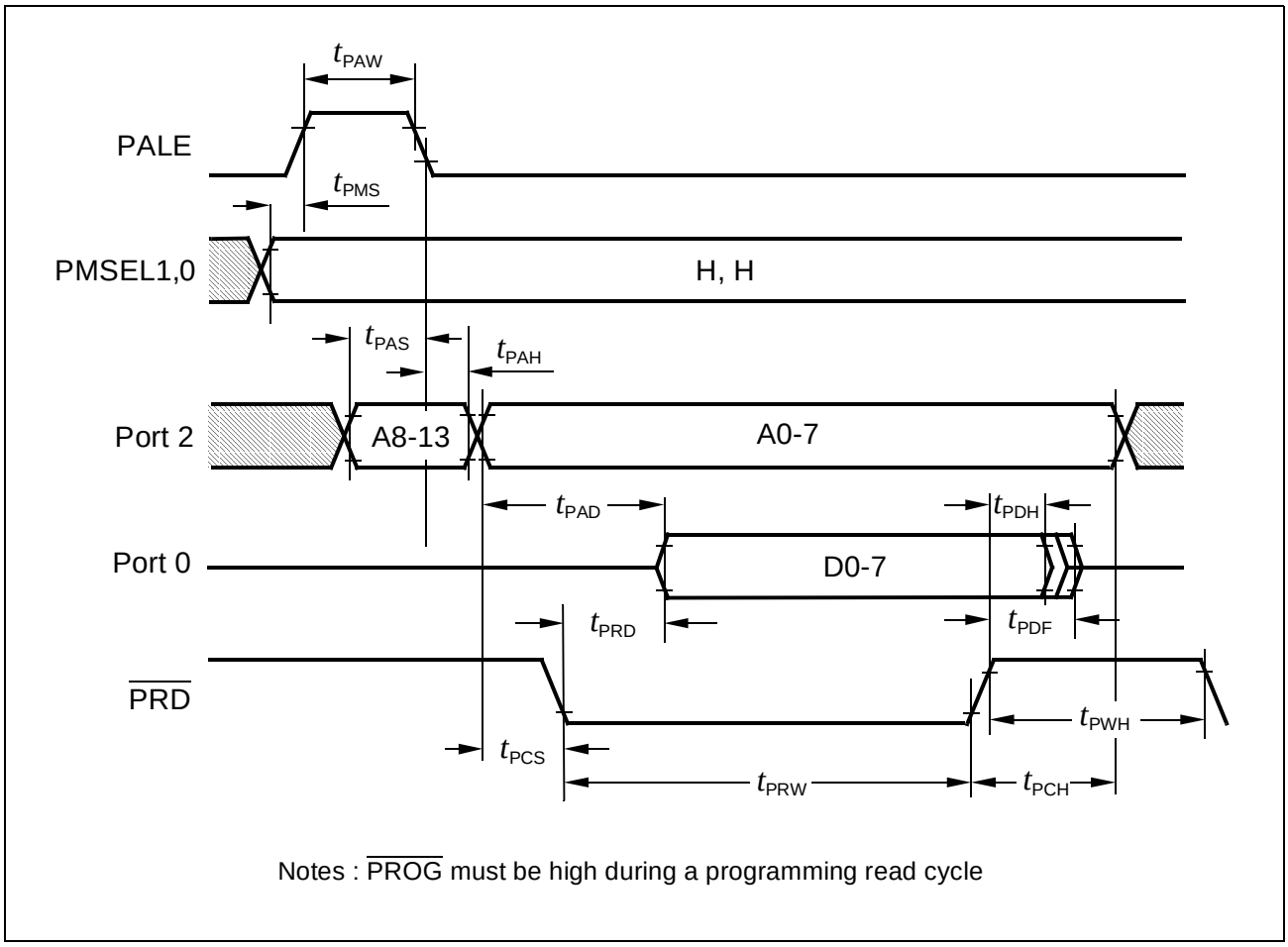
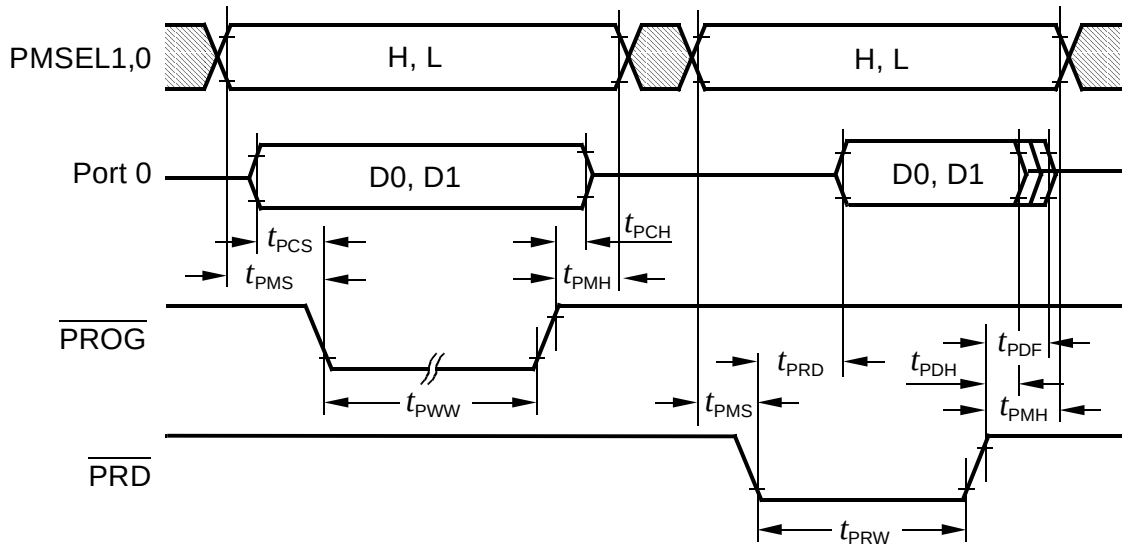
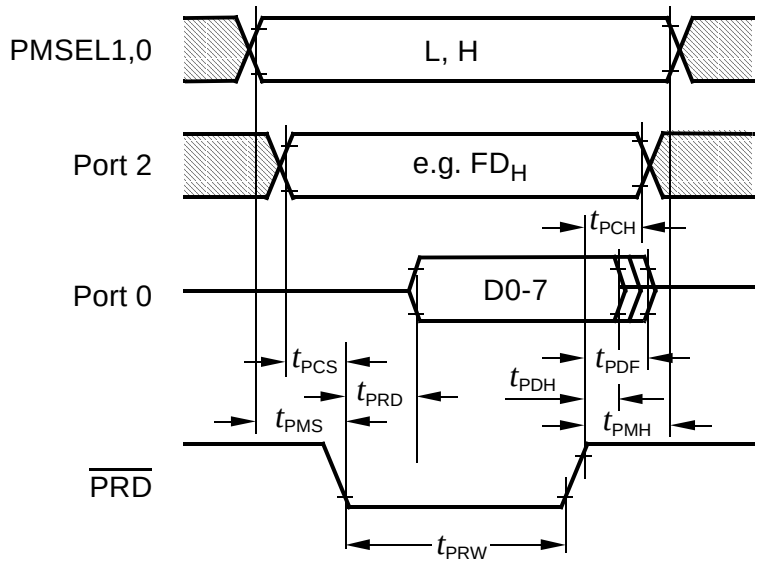


Figure 9
Verify Code Byte - Read Cycle Timing



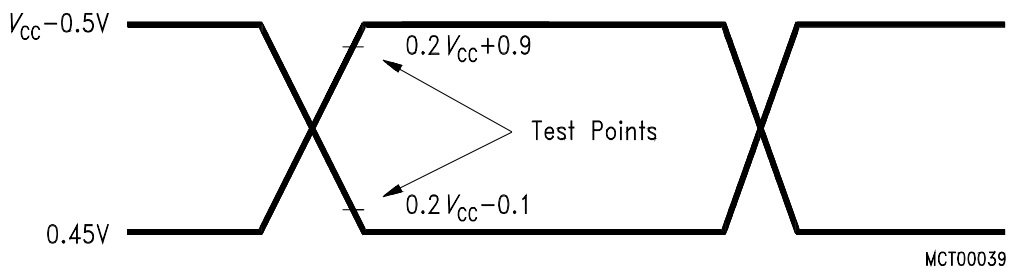
Note : PALE should be low during a lock bit read/write cycle

Figure 10
Lock Bit Access Timing



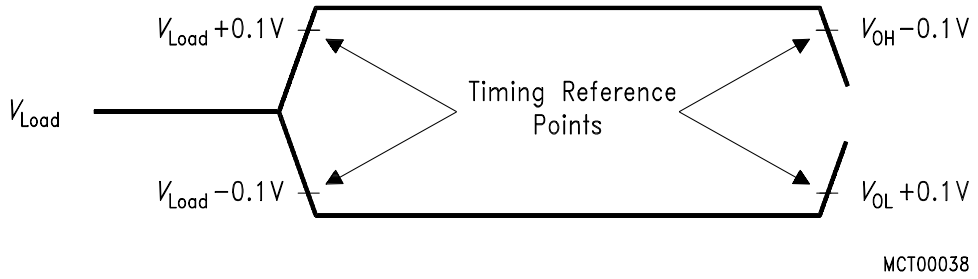
Note : PROG must be high during a programming read cycle

Figure 11
Version Byte - Read Timing



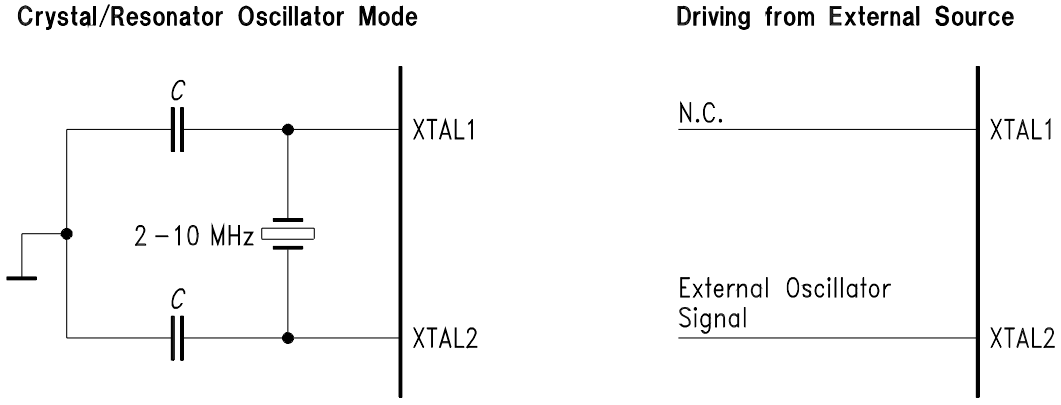
AC Inputs during testing are driven at V_{CC} - 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm$ 20 mA

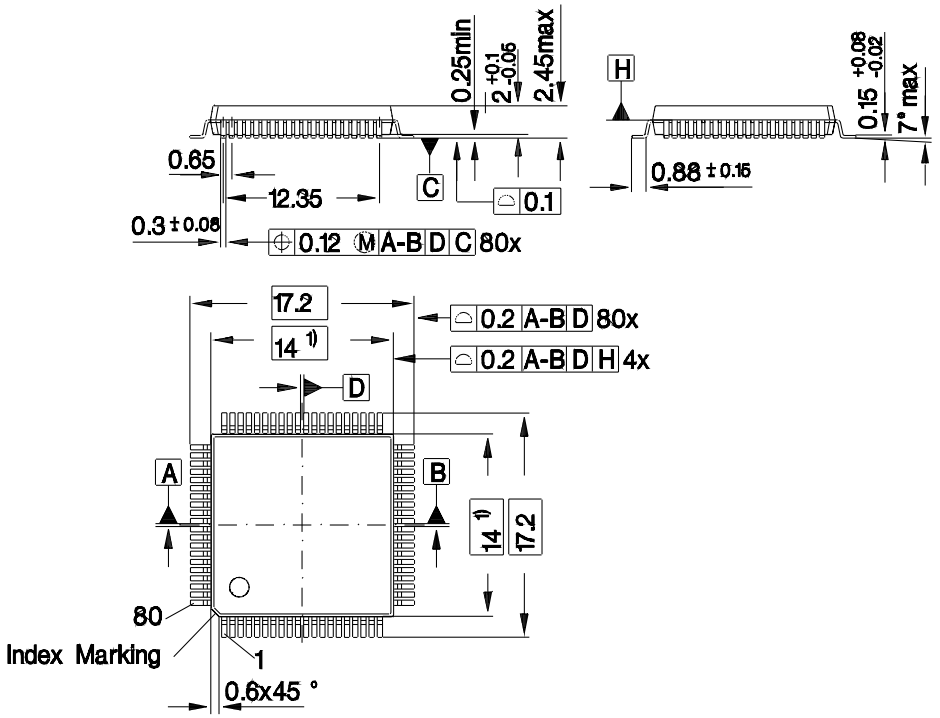
AC Testing : Float Waveforms



Recommended Oscillator Circuits for Crystal Oscillator

5.6 Package Information

Plastic Package, P-MQFP-80-1 (SMD)
(Plastic Metric Quad Flat Pack)



1) Does not include plastic or metal protrusion of 0.25 max. per side

SMD = Surface Mounted Device Dimensions in mm

P-MQFP-80-1 Package Outline

6 Addendum

Table 4
Cross Reference of Pins in Normal/Programming Mode

Pin Number	Pin in Normal Mode	Pin in Programming Mode
1	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$
15	PMSEL0	P3.0
16	PMSEL1	P3.1
17	$\overline{\text{PSEL}}$	P3.2
18	$\overline{\text{PRD}}$	P3.3
19	PALE	P3.4
36	XTAL2	XTAL2
37	XTAL1	XTAL1
38 - 45	A0/A8 - A7/A15	P2.0 - P2.7
47	$\overline{\text{PSEN}}$	$\overline{\text{PSEN}}$
48	$\overline{\text{PROG}}$	ALE
49	$\overline{\text{EA}}/V_{PP}$	$\overline{\text{EA}}$
52 - 59	D0 - D7	P0.0 - P0.7