MC100EP196

3.3V ECL Programmable Delay Chip with FTUNE

The MC100EP196 is a programmable delay chip (PDC) designed primarily for clock deskewing and timing adjustment. It provides programmably variable delay of a differential ECL input signal. It has similar architecture to the EP195 with the added feature of further tuneability in delay using the FTUNE pin. The FTUNE input takes an analog voltage from V_{CC} to V_{EE} to fine tune the output delay from 0 to 60 ps.

The delay section consists of a programmable matrix of gates and multiplexers as shown in the logic diagram, Figure 2. The delay increment of the EP196 has a digitally selectable resolution of about 10 ps and a range of up to 10 ns. The required delay is selected by the 10 programmable data select inputs D[0:9] which are latched on chip by a high signal on the latch enable (LEN) control. Delays are set by programming values of 0000000000 to 1111111111 on the D0 (LSB) through D9 (MSB) as shown in Table 1.

Because the EP196 is designed using a chain of multiplexers, it has a fixed minimum delay of 2.4 ns. An additional pin, D10, is provided for cascading multiple PDCs for increased programmable range. The cascade logic allows full control of multiple PDCs.

Select input pins, D0–D10, may be threshold controlled by combinations of interconnects between V_{EF} (pin 7) and V_{CF} (pin 8) for LVCMOS, ECL, or LVTTL level signals. LVTTL and LVCMOS operation is available in PECL mode only. For LVCMOS input levels, leave V_{CF} and V_{EF} open. For ECL operation, short V_{CF} and V_{EF} (pins 7 and 8). For LVTTL level operation, connect a 1.5 V supply reference to V_{CF} and leave open V_{EF} pin. The 1.5 V reference voltage to V_{CF} pin can be accomplished by placing a 2.2 kΩ resistor between V_{CF} and V_{EE} for 3.3 V power supply.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single–ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- Maximum Frequency > 1.2 GHz Typical
- PECL Mode Operating Range: V_{CC} = 3.0 V to 3.6 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = –3.0 V to –3.6 V
- Open Input Default State
- Safety Clamp on Inputs
- A Logic High on the $\overline{EN}$ Pin Will Force Q to Logic Low
- D[0:10] Can Accept Either ECL, LVCMOS, or LVTTL Inputs
- V_{BB} Output Reference Voltage

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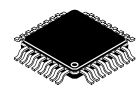
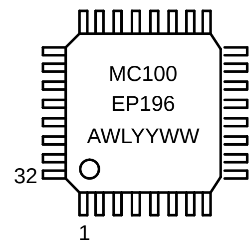
MARKING DIAGRAM*



LQFP–32
FA SUFFIX
CASE 873A

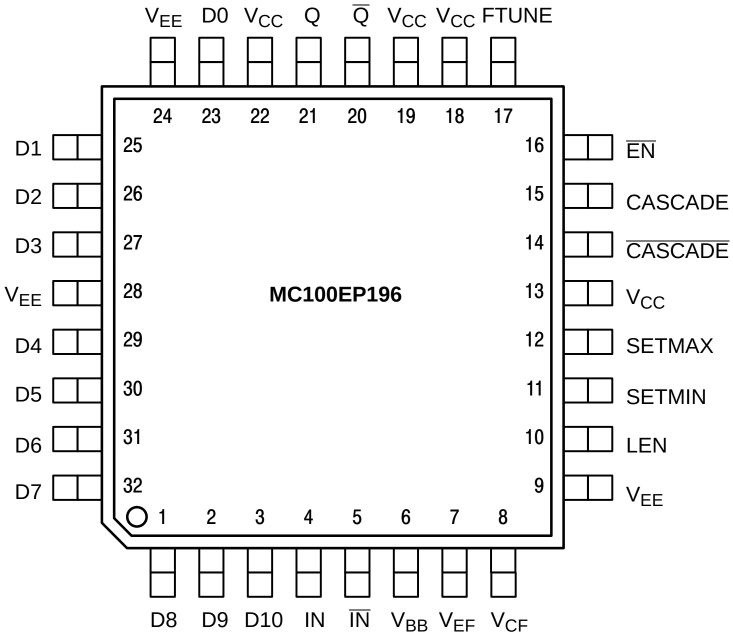


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, refer to Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100EP196FA	LQFP–32	250 Units/Tray
MC100EP196FAR2	LQFP–32	2000/Tape & Reel



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 32–Lead LQFP Pinout (Top View)

PIN DESCRIPTION

PIN	FUNCTION
IN*, $\overline{IN}$*	ECL Signal Input
$\overline{EN}$*	ECL Input Enable
D[0:10]*	LVCMOS, ECL, or LVTTL Select Inputs
Q, $\overline{Q}$	ECL Signal Output
LEN*	ECL Latch Enable Input
SETMIN*†	ECL Minimum Delay Set Input
SETMAX*	ECL Maximum Delay Set Input
CASCADE, $\overline{CASCADE}$	ECL Cascade Signal Output
V_{BB}	Output Reference Voltage
V_{CC}	Positive Supply
V_{EE}	Negative Supply
V_{CF}	LVCMOS, ECL, or LVTTL Input Select Input
V_{EF}	ECL Reference Mode Connection
FTUNE*	Fine Tuning Input

* Pins will default LOW (V_{EE}) when left open.
†SETMIN will override SETMAX if both pins are high.

TRUTH TABLE

$\overline{EN}$	L*	Q = IN
$\overline{EN}$	H	Q Logic Low
LEN	L*	Pass Through D[0:10]
LEN	H	Latch D[0:10]
SETMIN	L*	Normal Mode
SETMIN	H	Min Delay Path
SETMAX	L*	Normal Mode
SETMAX	H	Max Delay Path
V_{CF}	V_{EF} Pin**	ECL Mode
V_{CF}	No Connect	LVCMOS Mode
V_{CF}	1.5 V $\pm$100 mV	LVTTL Mode***

* Internal pulldown will provide logic low if pin left unconnected.
** Short V_{CF} (pin 8) and V_{EF} (pin 7).
*** For LVTTL Mode, if no external voltage can be provided, the reference voltage can be provided by connecting the appropriate resistor between V_{CF} and V_{EE} pins.

Power Supply	Resistor Value 5% (Tolerance)
3.3 V	2.2 kΩ

DATA INPUT OPERATING VOLTAGE TABLE				
POWER SUPPLY (V_{CC}, V_{EE})	DATA SELECT INPUTS (D [0:10])			
	LVCMOS	LVTTL	PECL	NECL
PECL	✓	✓	✓	N/A
NECL	N/A	N/A	N/A	✓

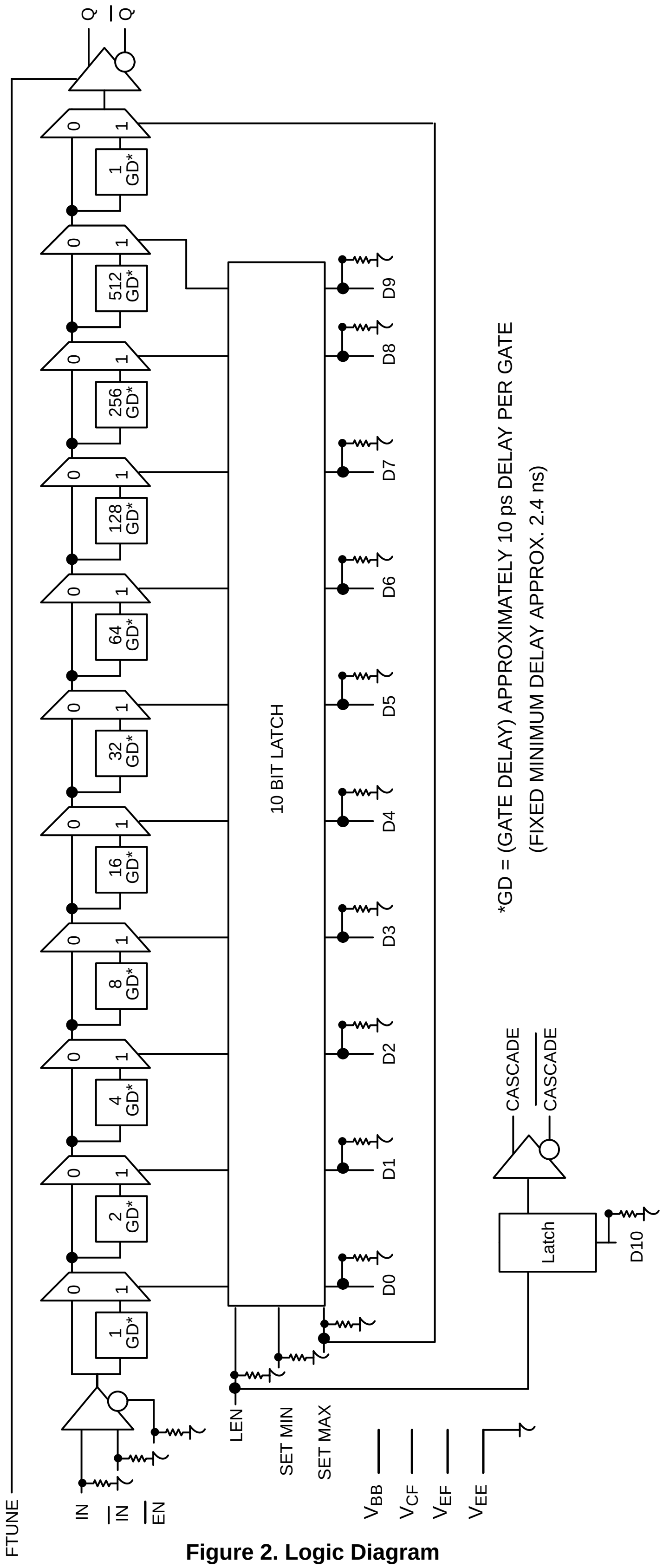


Figure 2. Logic Diagram

Table 1. Theoretical Delta Delay Values
(does not include fixed minimum delay)

D10	D(9:0) Value	Delay Value	Comment
	0000000000	0 ps	(SET MIN)
	0000000001	10 ps	
	0000000010	20 ps	
	0000000011	30 ps	
	0000000100	40 ps	
	0000000101	50 ps	
	0000000110	60 ps	
	0000000111	70 ps	
	0000001000	80 ps	
	0000010000	160 ps	
	0000100000	320 ps	
	0001000000	640 ps	
	0010000000	1280 ps	
	0100000000	2560 ps	
	1000000000	5120 ps	
	1111111111	10230 ps	
1	XXXXXXXXXX	10240 ps	(SET MAX)

Table 2. Typical FTUNE Delay Pin

Input Range	Output Range
V_{CC}–V_{EE} (V)	0 – 60 (ps)

ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		N/A
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 100 V > 2 kV
Moisture Sensitivity (Note 1)		Level 2
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in″
Transistor Count		1237 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient)	0 LFPM 500 LFPM	32 LQFP 32 LQFP	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	std bd	32 LQFP	12 to 17	°C/W
T_{sol}	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 3)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	100	125	160	110	130	170	110	135	175	mA
V_{OH}	Output HIGH Voltage (Note 4)	2155	2300	2405	2155	2300	2405	2155	2300	2405	mV
V_{OL}	Output LOW Voltage (Note 4)	1355	1520	1605	1355	1500	1605	1355	1485	1605	mV
V_{IH}	Input HIGH Voltage (Single–Ended) PECL LVCMOS LVTTL	 2075 2000 2000		 2420 3300 3300	 2075 2000 2000		 2420 3300 3300	 2075 2000 2000		 2420 3300 3300	mV
V_{IL}	Input LOW Voltage (Single–Ended) PECL LVCMOS LVTTL	 1355 0 0		 1675 800 800	 1355 0 0		 1675 800 800	 1355 0 0		 1675 800 800	mV
V_{BB}	Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{CF}	LVTTL Mode Input Detect Voltage @ IV_{CF} = 700 μA	1.4	1.5	1.6	1.4	1.5	1.6	1.4	1.5	1.6	V
V_{EF}	Reference Voltage for ECL Mode Connection	1900	1960	2050	1875	1953	2050	1850	1945	2050	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 5)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current (PECL) IN, $\overline{IN}$, $\overline{EN}$, LEN, SETMIN, SETMAX			150			150			150	μA
I_{IHH}	FTUNE Input High Current @ V_{CC}	50	87	150	50	84	150	50	82	150	μA
I_{IL}	Input LOW Current (PECL) IN, $\overline{IN}$, $\overline{EN}$, LEN, SETMIN, SETMAX	0.5			0.5			0.5			μA
I_{ILL}	FTUNE Input LOW Current @V_{EE}	–10	0	10	–10	0	10	–10	0	10	μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

3. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to –0.3 V.
4. All loading with 50 Ω to V_{CC}–2.0 volts.
5. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = –3.3 V (Note 6)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	100	125	160	110	130	170	110	135	175	mA
V_{OH}	Output HIGH Voltage (Note 7)	–1145	–1000	–895	–1145	–1000	–895	–1145	–1000	–895	mV
V_{OL}	Output LOW Voltage (Note 7)	–1945	–1780	–1695	–1945	–1800	–1695	–1945	–1815	–1695	mV
V_{IH}	Input HIGH Voltage (Single–Ended) NECL	–1225		–880	–1225		–880	–1225		–880	mV
V_{IL}	Input LOW Voltage (Single–Ended) NECL	–1945		–1625	–1945		–1625	–1945		–1625	mV
V_{BB}	Output Voltage Reference	–1525	–1425	–1325	–1525	–1425	–1325	–1525	–1425	–1325	mV
V_{EF}	Reference Voltage for ECL Mode Connection	–1400	–1340	–1250	–1425	–1347	–1250	–1450	–1355	–1250	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 8)	V_{EE}+2.0		0	V_{EE}+2.0		0	V_{EE}+2.0		0	V
I_{IH}	Input HIGH Current IN, $\overline{IN}$, $\overline{EN}$, LEN, SETMIN, SETMAX			150			150			150	μA
I_{IHH}	FTUNE Input High Current @ V_{CC}	50	87	150	50	84	150	50	82	150	μA
I_{IL}	Input LOW Current IN, $\overline{IN}$, $\overline{EN}$, LEN, SETMIN, SETMAX	0.5			0.5			0.5			μA
I_{ILL}	FTUNE Input LOW Current @ V_{EE}	–10	0	10	–10	0	10	–10	0	10	μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

6. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to –0.3 V.
7. All loading with 50 Ω to V_{CC}–2.0 volts.
8. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = –3.0 V to –3.6 V or V_{CC} = 3.0 V to 3.6 V; V_{EE} = 0 V (Note 9)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency		1.2			1.2			1.2		GHz
t_{PLH} t_{PHL}	Propagation Delay										ps
	IN to Q; D(0–9) = 0	1810	2210	2610	1960	2360	2760	2180	2580	2980	
	IN to Q; D(0–9) = 1023	9500	11496	13500	10000	12258	14000	10955	13454	15955	
	$\overline{EN}$ to Q; D(0–9) = 0	1780	2277	2780	1930	2430	2930	2150	2650	3150	
	D10 to CASCADE	350	450	550	380	477	580	420	520	620	
t_{RANGE}	Programmable Range										ps
	{D(0–9) = HI} – {D(0–9) = LO}	8600	9285	10000	9200	9897	10700	9900	10875	12000	
Δt	Step Delay (Note 10)										ps
	D0 High		7			11			13		
	D1 High		23			30			32		
	D2 High		39			48			53		
	D3 High		58			67			73		
	D4 High	90	137	185	100	149	200	90	154	225	
	D5 High	245	293	335	260	313	370	270	337	410	
	D6 High	530	590	650	560	629	710	600	681	770	
	D7 High	1060	1158	1265	1130	1237	1355	1200	1353	1520	
	D8 High	2160	2317	2490	2290	2472	2680	2450	2712	3015	
	D9 High	4335	4647	5010	4590	4955	5385	4935	5440	6015	
Mono	Monotonicity (Note 11)		9			10			11		ps
t_{SKEW}	Duty Cycle Skew (Note 12)										ps
	$\lvert t_{PHL}-t_{PLH} \rvert$		20			22			27		
t_s	Setup Time										ps
	D to LEN	150	–10		150	–70		150	–70		
	D to IN (Note 13)	100	–130		100	–150		100	–165		
	$\overline{EN}$ to IN (Note 14)	150	–105		150	–120		150	–140		
t_h	Hold Time										ps
	LEN to D	225	170		200	70		200	60		
	IN to $\overline{EN}$ (Note 15)	450	275		450	305		450	325		
t_R	Release Time										ps
	$\overline{EN}$ to IN (Note 16)	150	–105		150	–120		150	–140		
	SET MAX to LEN	400	70		400	110		400	160		
	SET MIN to LEN	300	165		350	180		350	205		
t_{jit}	Random Clock Jitter @ 1.2 GHz, SETMAX Delay		3			3			3		ps
V_{PP}	Input Voltage Swing (Differential)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Time										ps
	20–80% (Q)	85	110	130	95	120	145	110	135	160	
	20–80% (CASCADE)	100	150	200	110	160	210	125	175	225	

9. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}–2.0 V.
10. Specification limits represent the amount of delay added with the assertion of each individual delay control pin. The various combinations of asserted delay control inputs will typically realize D0 resolution steps across the specified programmable range.
11. The monotonicity indicates the increased delay value for each binary count increment on the control inputs D(0–9).
12. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output.
13. This setup time defines the amount of time prior to the input signal the delay tap of the device must be set.
14. This setup time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than V_{CC} – 1425 mV to that IN/$\overline{IN}$ transition.
15. This hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or positive going $\overline{IN}$ to prevent an output response greater than V_{CC} – 1425 mV to that IN/$\overline{IN}$ transition.
16. This release time is the minimum time that $\overline{EN}$ must be deasserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and transition times.

Using the FTUNE Analog Input

The analog FTUNE pin on the EP196 device is intended to add more delay in a tunable gate to enhance the 10 ps resolution capabilities of the fully digital EP196. The level of resolution obtained is dependent on the voltage applied to the FTUNE pin.

To provide this further level of resolution, the FTUNE pin must be capable of adjusting the additional delay finer than the 10 ps digital resolution (See Logic Diagram). This requirement is easily achieved because a 60 ps additional delay can be obtained over the entire FTUNE voltage range (See Figure 3). This extra analog range ensures that the FTUNE pin will be capable even under worst case conditions of covering a digital resolution. Typically, the analog input will be driven by an external DAC to provide a digital control with very fine analog output steps. The final resolution of the device will be dependent on the width of the DAC chosen.

To determine the voltage range necessary for the FTUNE input, Figure 3 should be used. There are numerous voltage ranges which can be used to cover a given delay range; users are given the flexibility to determine which one best fits their designs.

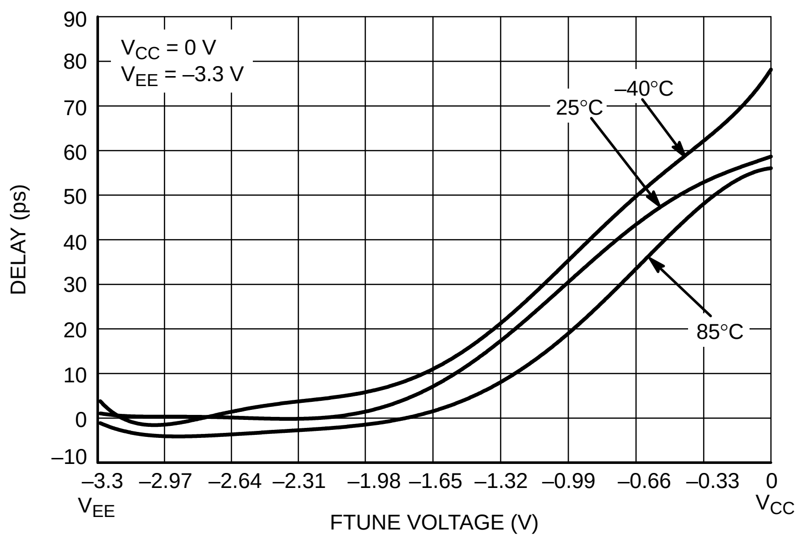


Figure 3. Typical EP196 Delay versus FTUNE Voltage

Cascading Multiple EP196s

To increase the programmable range of the EP196, internal cascade circuitry has been included. This circuitry allows for the cascading of multiple EP196s without the need for any external gating. Furthermore, this capability requires only one more address line per added E196. Obviously, cascading multiple programmable delay chips will result in a larger programmable range; however, this increase is at the expense of a longer minimum delay.

Figure 4 illustrates the interconnect scheme for cascading two EP196s. As can be seen, this scheme can easily be expanded for larger EP196 chains. The D10 input of the EP196 is the cascade control pin. With the interconnect scheme of Figure 4 when D10 is asserted, it signals the need for a larger programmable range than is achievable with a single device. The A11 address can be added to generate a cascade output for the next EP196. For a 2–device configuration, A11 is not required.

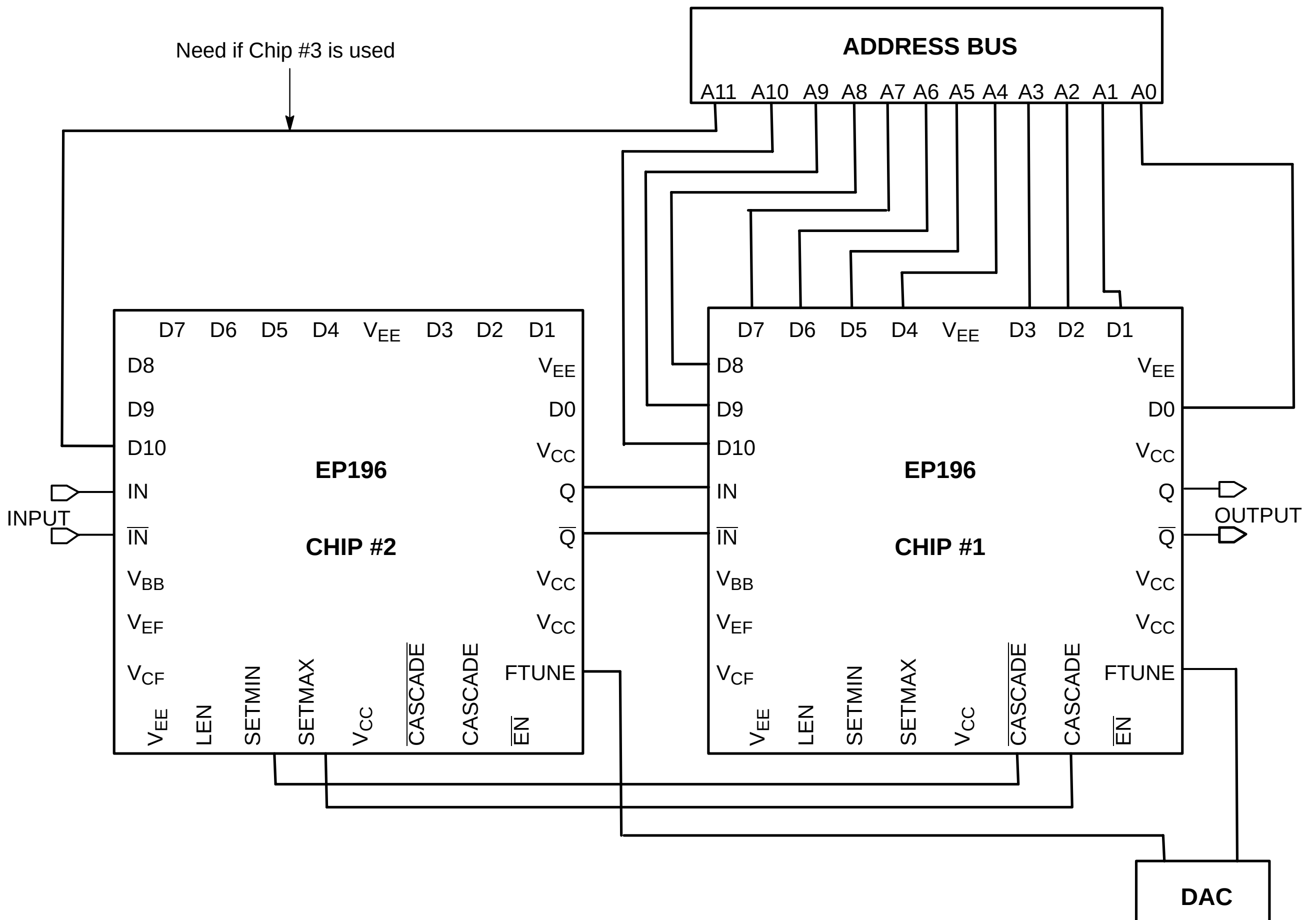


Figure 4. Cascading Interconnect Architecture

An expansion of the latch section of the block diagram is pictured in Figure 5. Use of this diagram will simplify the explanation of how the cascade circuitry works. When D10 of chip #1 in Figure 4 is low, the cascade output will also be low while the cascade bar output will be a logical high. In this condition, the SETMIN pin of chip #2 will be asserted and thus all of the latches of chip #2 will be reset and the device will be set at its minimum delay.

Chip #1, on the other hand, will have both SETMIN and SETMAX deasserted so that its delay will be controlled entirely by the address bus A0–A9. If the delay needed is greater than can be achieved with 1023 gate delays (1111111111 on the A0–A9 address bus), D10 will be asserted to signal the need to cascade the delay to the next EP196 device. When D10 is asserted, the SETMIN pin of chip #2 will be deasserted and the SETMAX pin asserted, resulting in the device delay to be the maximum delay. Figure 6 shows the delay time of two EP196 chips in cascade.

To expand this cascading scheme to more devices, one simply needs to connect the D10 pin from the next chip to the address bus and CASCADE outputs to the next chip in the same manner as pictured in Figure 4. The only addition to the logic is the increase of one line to the address bus for cascade control of the second programmable delay chip.

Furthermore, to fully utilize EP196, the FTUNE pin can be used for additional delay and for finer resolution than 10 ps. As shown in Figure 3, an analog voltage input from DAC can adjust the FTUNE pin with an extra 60 ps of delay for each chip.

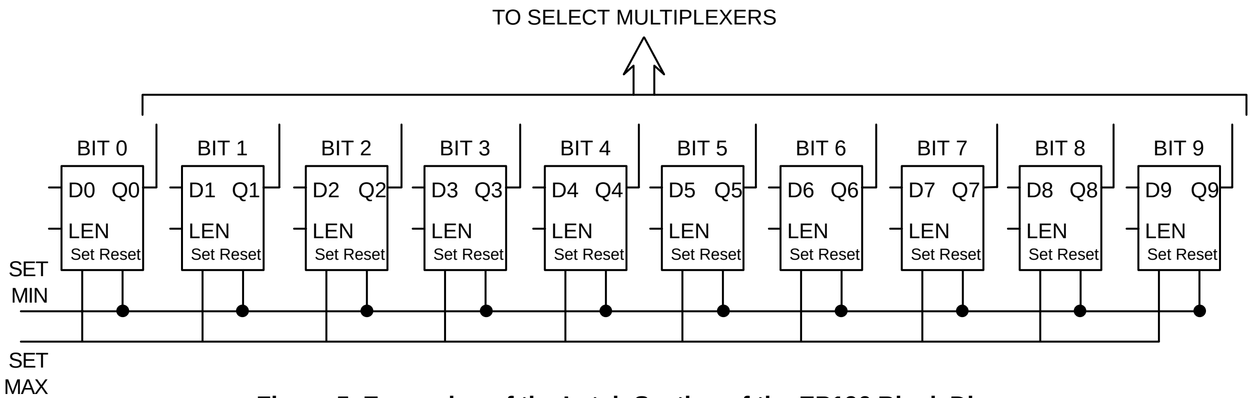


Figure 5. Expansion of the Latch Section of the EP196 Block Diagram

VARIABLE INPUT TO CHIP #1 AND *SETMIN* FOR CHIP #2												
INPUT FOR CHIP #1												**Total**
D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Delay Value	Delay Value
0	0	0	0	0	0	0	0	0	0	0	0 ps	4400 ps
0	0	0	0	0	0	0	0	0	0	1	10 ps	4410 ps
0	0	0	0	0	0	0	0	0	1	0	20 ps	4420 ps
0	0	0	0	0	0	0	0	0	1	1	30 ps	4430 ps
0	0	0	0	0	0	0	0	1	0	0	40 ps	4440 ps
0	0	0	0	0	0	0	0	1	0	1	50 ps	4450 ps
0	0	0	0	0	0	0	0	1	1	0	60 ps	4460 ps
0	0	0	0	0	0	0	0	1	1	1	70 ps	4470 ps
0	0	0	0	0	0	0	1	0	0	0	80 ps	4480 ps
0	0	0	0	0	0	1	0	0	0	0	160 ps	4560 ps
0	0	0	0	0	1	0	0	0	0	0	320 ps	4720 ps
0	0	0	0	1	0	0	0	0	0	0	640 ps	5040 ps
0	0	0	1	0	0	0	0	0	0	0	1280 ps	5680 ps
0	0	1	0	0	0	0	0	0	0	0	2560 ps	6960 ps
0	1	0	0	0	0	0	0	0	0	0	5120 ps	9520 ps
0	1	1	1	1	1	1	1	1	1	1	10230 ps	14630 ps

VARIABLE INPUT TO CHIP #1 AND *SETMAX* FOR CHIP #2												
INPUT FOR CHIP #1												**Total**
D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Delay Value	Delay Value
1	0	0	0	0	0	0	0	0	0	0	10240 ps	14640 ps
1	0	0	0	0	0	0	0	0	0	1	10250 ps	14650 ps
1	0	0	0	0	0	0	0	0	1	0	10260 ps	14660 ps
1	0	0	0	0	0	0	0	0	1	1	10270 ps	14670 ps
1	0	0	0	0	0	0	0	1	0	0	10280 ps	14680 ps
1	0	0	0	0	0	0	0	1	0	1	10290 ps	14690 ps
1	0	0	0	0	0	0	0	1	1	0	10300 ps	14700 ps
1	0	0	0	0	0	0	0	1	1	1	10310 ps	14710 ps
1	0	0	0	0	0	0	1	0	0	0	10320 ps	14720 ps
1	0	0	0	0	0	1	0	0	0	0	10400 ps	14800 ps
1	0	0	0	0	1	0	0	0	0	0	10560 ps	14960 ps
1	0	0	0	1	0	0	0	0	0	0	10880 ps	15280 ps
1	0	0	1	0	0	0	0	0	0	0	11520 ps	15920 ps
1	0	1	0	0	0	0	0	0	0	0	12800 ps	17200 ps
1	1	0	0	0	0	0	0	0	0	0	15360 ps	19760 ps
1	1	1	1	1	1	1	1	1	1	1	20470 ps	24870 ps

Figure 6. Cascaded Delay Value of Two EP196s

Multi–Channel Deskewing

The most practical application for EP196 is in multiple channel delay matching. Slight differences in impedance and cable length can create large timing skews within a high–speed system. To deskew multiple signal channels, each channel can be sent through each EP196 as shown in Figure 7. One signal channel can be used as reference and the other EP196s can be used to adjust the delay to eliminate the timing skews. Nearly any high–speed system can be fine tuned (as small as 10 ps) to reduce the skew to extremely tight tolerances using the available FTUNE pin.

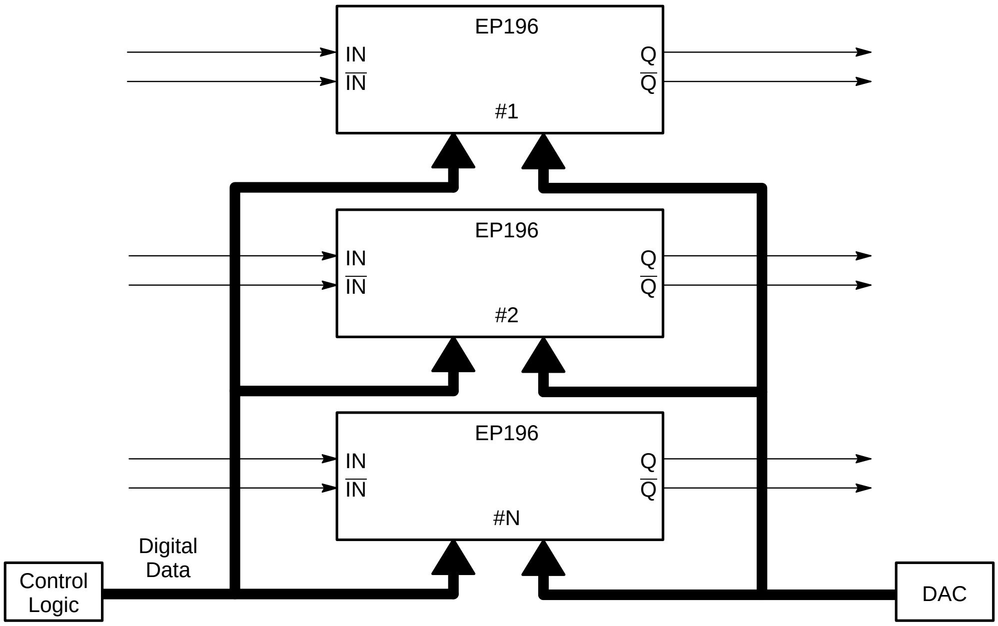


Figure 7. Multiple Channel Deskewing Diagram

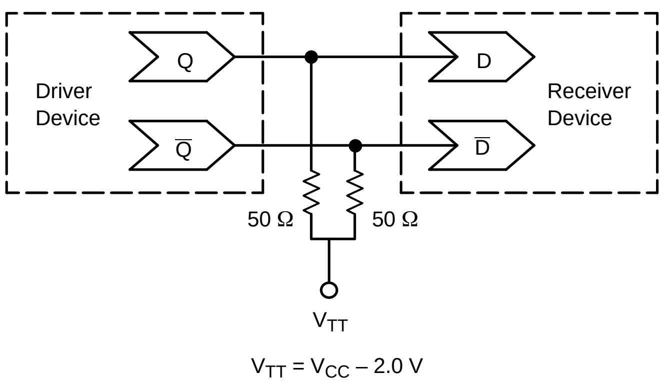


Figure 8. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels

AN1405 – ECL Clock Distribution Techniques

AN1406 – Designing with PECL (ECL at +5.0 V)

AN1504 – Metastability and the ECLinPS Family

AN1568 – Interfacing Between LVDS and ECL

AND8002 – Marking and Date Codes

AND8009 – ECLinPS Plus Spice I/O Model Kit

AND8020 – Termination of ECL Logic Devices

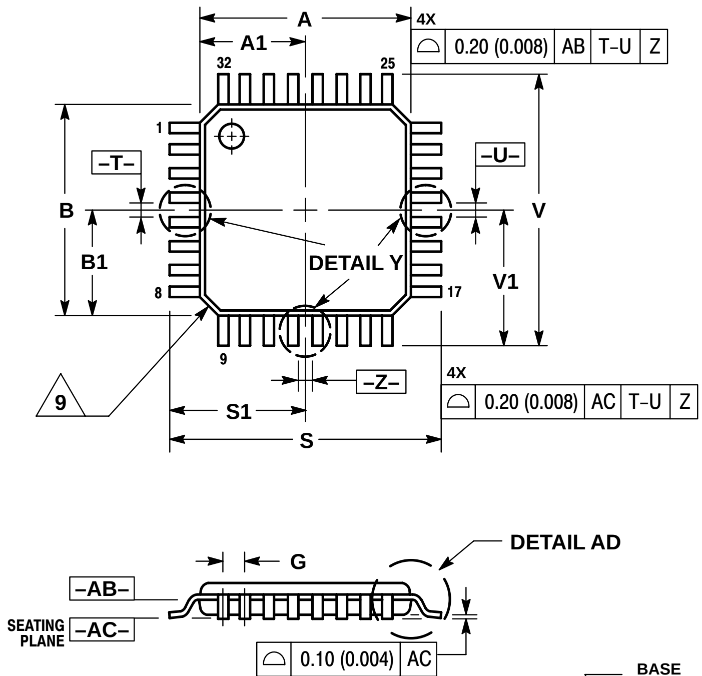
AND8066 – Interfacing with ECLinPS

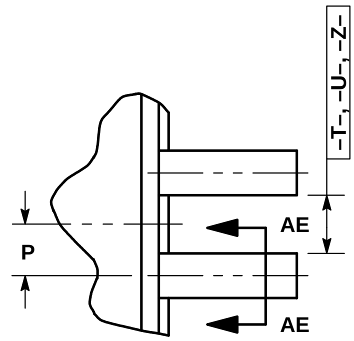
AND8072 – Thermal Analysis and Reliability of WIRE BONDED ECL

For an updated list of Application Notes, please see our website at http://onsemi.com.

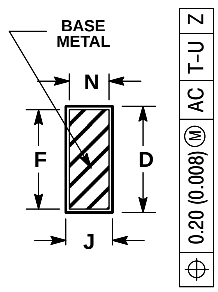
PACKAGE DIMENSIONS

LQFP
FA SUFFIX
32–LEAD PLASTIC PACKAGE
CASE 873A–02
ISSUE A

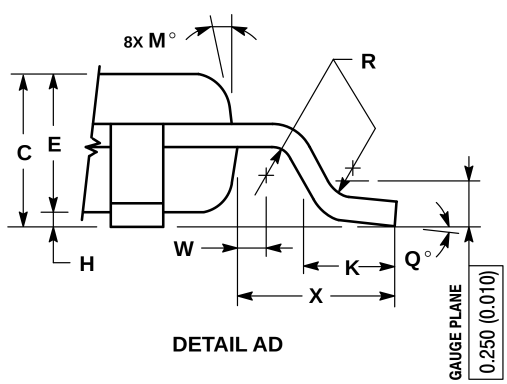




DETAIL Y



SECTION AE–AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

Notes

Notes

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