☐ MN101D06F , MN101D06G , MN101D06H VTR Servo

Type	MN101D06F	MN101D06G	MN101D06H
ROM (×8-bit)	96 K	128 K	160 K
RAM (×8-bit)	3 K	4 K	5 K
Package	QFP100-P-1818B *Lead-free		

Minimum Instruction Execution Time	With main clock operated	0.1397 μs (at 4.0 V to 5.5 V, 14.32 MHz)
	When sub-clock operated	71.5 μs (at 3.0 V to 5.5 V fixed to 14.32 MHz internal frequency division)
		61 μs (at 2.2 V to 5.5 V, 32.768 kHz)

Interrupts

• RESET • Runaway • External 0, 1, 2, 3, 4/key input (P50 to 54) • Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 4 • Timer 6 • Capstan FG • Control • HSW • Cylinder FG • Servo VSYNC • Synchronous output • OSD • XDS • Serial 0 • Serial 1 • Serial 2 • A/D (common with PWM 4 reference frequency) • OSDVSYNC

Timer Counter

Timer counter 0: 16-bit × 1
  (timer function, clock function [max. 2 s or max. 36 h at cascade-connecting with timer 6])
    Clock source ···················· 1/2, 1/4, 1/8, 1/16 of system clock frequency; overflow of timer counter 6;
                    1/512 of XI oscillation clock or OSC oscillation clock frequency
    Interrupt source ·············· overflow of timer counter 0

Timer counter 1: 16-bit × 1 (timer function, linear timer counter function)
    Clock source ···················· 1/2, 1/4, 1/8, 1/16 of system clock frequency; CTL signal
    Interrupt source ·············· overflow of timer counter 1

Timer counter 2: 16-bit × 1 (timer function, input capture (DCTL specified edge), duty judgment of DCTL signal)
    Clock source ···················· 1/2, 1/4, 1/8, 1/12, 1/16, 1/24 of system clock frequency
    Interrupt source ·············· overflow of timer counter 2; input of DCTL specified edge; underflow of timer 2
                    shift register 4-bit counter; coincidence of timer 2 shift register with timer 2 shift
                    register compare register

Timer counter 3: 16-bit × 1
  (timer function, detection of serial indexing, generation of remote control output carrier frequency)
    Clock source ···················· 1/2, 1/4, 1/8, 1/16 of system clock frequency; XI oscillation clock
    Interrupt source ·············· overflow of timer counter 3

Timer counter 4: 16-bit × 1 (timer function, event count [P15 input], generation of serial transmission clock)
    Clock source ···················· 1/8, 1/16 of system clock frequency; external clock input
    Interrupt source ·············· overflow of timer counter 4; coincidence of timer counter 4 with OCR4

Timer counter 5: 19-bit × 1 (watchdog, stable oscillation waiting function)
    Clock source ···················· system clock
    Watchdog interrupt source ·· $1/2^{16}$, $1/2^{19}$ of timer counter 5 frequency
    Clear by stable oscillation ·· after 256 counts by timer counter 5 (2^{18} counts of OSC oscillation clock)

Timer counter 6: 16-bit × 1 (clock function [max. 2 s])
    Clock source ···················· 1/512 of OSC oscillation clock frequency; XI oscillation clock;
                    1/4, 1/8, 1/64, 1/128 of system clock frequency
    Interrupt source ·············· $1/2^{13}$, $1/2^{14}$, $1/2^{15}$ overflow of timer counter 6

Timer counter 7: 8-bit × 1 (timer function, event count [P53 input])
    Clock source ···················· 1/4, 1/8, 1/16, 1/32 of system clock frequency; external clock input
    Interrupt source ·············· overflow of timer counter 7

Serial Interface

Serial 0: 8-bit × 1 (synchronous type/start-stop synchronous type) (transfer direction of MSB/LSB selectable)
    Synchronous type clock source · 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency;
                    2-division timer 4 output; $\overline{SBT0}$ pin input
    Clock for UART ·············· 8-division of above clock; 2-division timer 4 output; $\overline{SBT0}$ pin input

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■ **Serial Interface (Continue)**	Serial 1: 8-bit × 1

(synchronous type/remote control transmission/simple remote control receive) (transfer direction of MSB/LSB selectable, start condition function)

Clock source ···················· 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency;
2-division timer 4 output; $\overline{SBT1}$ pin input

Remote control clock ······ 2-division timer 4 output

Serial 2: 8-bit × 1 (I²C) (master transmission/reception, slave transmission/reception)
Clock source ···················· 1/144 to 1/252 of system clock; SCK pin input

■ **OSD**

OSD mode:Accommodation with menu or super impose display

Applicable broadcasting system :	NTSC, PAL, PAL-M, PAL-N
Screen configuration	: 24 characters × 2n rows (n = 1 to 6)
Character type	: max. 512 character types (variable)
Character size	: 12 × 18 dots (Vertical direction: 1 dot for 2H at × 1 setting.)
Enlarged characters	: each × 2, × 3 or × 4 settings in horizontal and vertical
Character interpolation	: none
Line background color	: 8-hue settable (settable in the row unit at menu display)
Line background intensity	: 8 gradations settable in the row unit
Screen background color	: 8-hue settable (at output of composite video signal)
Character color	: white
Character intensity	: 8 gradations settable in the row unit
Frame function	: 1-dot frame in 4 or 8 directions
Frame intensity	: 4 gradations settable in the row unit
Box shade function	: settable in the character unit (at output of composite video signal with 129 or more characters (character types))
Blinking	: none (covered by software)
Inverted character	: settable in the character unit
Halftone	: settable in the row unit in 2 intensity gradations (at output of external synchronous composite video signal)

CCD mode: Supports Closed Caption in the U.S.A.

Screen configuration	: 32 characters × 16 rows
Character type	: max. 128 character types (variable)
Character size	: 12 × 26 dots (Vertical direction: 1 dot for 1H, including 8 dots in the underlined area)
Enlarged characters	: none
Character interpolation	: none
Line background color	: 8-hue settable
Line background intensity	: 8 gradations settable in the screen unit (at output of composite video signal)
Screen background color	: 8-hue settable (at output of composite video signal)
Character color	: 8 colors (at RGB output)
	: White (at output of composite video signal)
Character intensity	: 8 gradations settable in the screen unit
Frame function	: none
Box shade function	: none
Inverted character	: none
Halftone	: settable in the row unit in 2 intensity gradations (at output of external synchronous composite video signal)
Others	: Underline, italic, blinking function and scroll
Input	: composite video signal input (output level: 1 V[p-p] / 2 V[p-p])
Clamp method	: sync chip clamp, clamp level in 4 levels
Output	: composite video output
	: digital output (6 pins)
Measure against image fluctuation	: built-in AFC circuit
Dot clock	: 1/2 of OSC oscillation clock (automatic phase adjustment)

See the next page for electrical characteristics, pin assignment and support tool.

■ **XDS**			Built-in U.S. closed caption data slicer (optional 2 line data can be extracted.)
■ **ROM Correction**			Correcting address designation: up to 3 addresses possible Correction method: correction program being saved in internal RAM
■ **I/O Pins**	**I/O**	75	• Common use: 75 ports 0, 1, 2, 4, 5, 6, 7, A, B (by bit)
	Input	2	• Common use: 2
■ **A/D Inputs**			8-bit × 13-ch. (without S/H)
■ **PWM**			13-bit × 2-ch. (at repetition cycle 572 μs, 14.32 MHz), 10-bit × 2-ch. (at repetition cycle 71.5 μs, 14.32 MHz), 8-bit × 1-ch. (at repetition cycle 35.7 μs, 14.32 MHz)
■ **ICR**			18-bit × 6-ch.
■ **OCR**			16-bit × 7-ch. , 8-bit × 1-ch.
■ **Special Ports**			Buzzer output; 3-state output (PTO) VLP pin; synchronous output: 7; 3-state synchronous output: 4; remote control receive; CTL amp; built-in FG amp; output of 1/2 OSC oscillation clock (2 V[p-p]); output of 1/4 OSC oscillation clock (1 V[p-p])
■ **Notes**			VISS/VASS detection function

■ **Electrical Characteristics**

Supply current

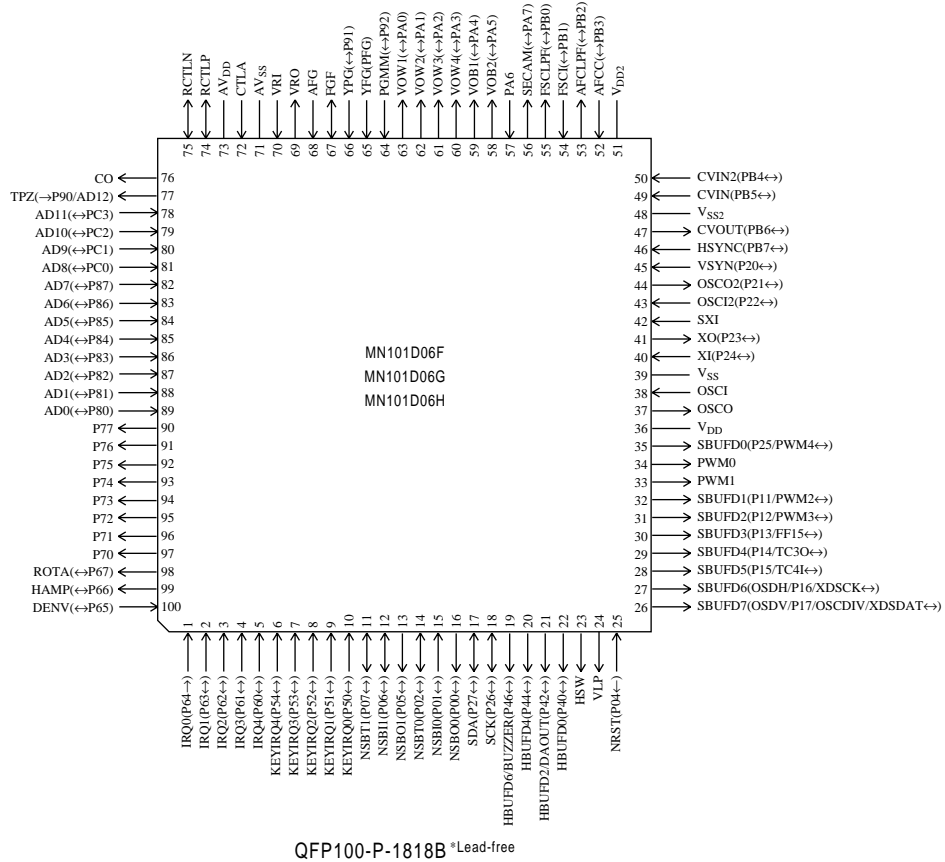| Parameter	Symbol	Condition	Limit min	Limit typ	Limit max	Unit
Operating supply current	IDD1	14.32 MHz operation without load, VDD = 5 V		60	100	mA
	IDD2	1/1024 of 14.32 MHz operation without load, VDD = 3.0 V		2	5	mA
	IDD3	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		50	100	μA
Supply current at STOP	IDSP	Stop of oscillation without load, VDD = 5 V			20	μA
Supply current at HALT	IDHT0	14.32 MHz oscillation without load, VDD = 5 V		5	15	mA
	IDHT1	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		5	20	μA

(Ta = 25°C ± 2°C , VSS = 0 V)

A/D Converter Performance

Parameter	Symbol	Condition	Limit min	Limit typ	Limit max	Unit
Conversion relative error	ΔNLAD				± 3	LSB
A/D Conversion Time	tAD	fosc = 14.32 MHz		8		μs
Analog Input Voltage					5	V

(Ta = 25°C ± 2°C , VDD = 5.0 V , VSS = 0 V)

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■ **Pin Assignment**

Top pins (left to right, 75–51):
RCTLN (75), RCTLP (74), AV_DD (73), CTLA (72), AV_SS (71), VRI (70), VRO (69), AFG (68), FGF (67), YPG(↔P91) (66), YFG(PFG) (65), PGMM(↔P92) (64), VOWl(↔PA0) (63), VOW2(↔PA1) (62), VOW3(↔PA2) (61), VOW4(↔PA3) (60), VOB1(↔PA4) (59), VOB2(↔PA5) (58), PA6 (57), SECAM(↔PA7) (56), FSCLPF(↔PB0) (55), FSCI(↔PB1) (54), AFCLPF(↔PB2) (53), AFCC(↔PB3) (52), V_DD2 (51)

Left pins (top to bottom, 76–100):
CO (76)
TPZ(→P90/AD12) (77)
AD11(↔PC3) (78)
AD10(↔PC2) (79)
AD9(↔PC1) (80)
AD8(↔PC0) (81)
AD7(↔P87) (82)
AD6(↔P86) (83)
AD5(↔P85) (84)
AD4(↔P84) (85)
AD3(↔P83) (86)
AD2(↔P82) (87)
AD1(↔P81) (88)
AD0(↔P80) (89)
P77 (90)
P76 (91)
P75 (92)
P74 (93)
P73 (94)
P72 (95)
P71 (96)
P70 (97)
ROTA(↔P67) (98)
HAMP(↔P66) (99)
DENV(↔P65) (100)

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Right pins (top to bottom, 50–26):
CVIN2(PB4↔) (50)
CVIN(PB5↔) (49)
V_SS2 (48)
CVOUT(PB6↔) (47)
HSYNC(PB7↔) (46)
VSYN(P20↔) (45)
OSCO2(P21↔) (44)
OSCI2(P22↔) (43)
SXI (42)
XO(P23↔) (41)
XI(P24↔) (40)
V_SS (39)
OSCI (38)
OSCO (37)
V_DD (36)
SBUFD0(P25/PWM4↔) (35)
PWM0 (34)
PWM1 (33)
SBUFD1(P11/PWM2↔) (32)
SBUFD2(P12/PWM3↔) (31)
SBUFD3(P13/FF15↔) (30)
SBUFD4(P14/TC3O↔) (29)
SBUFD5(P15/TC4I↔) (28)
SBUFD6(OSDH/P16/XDSCK↔) (27)
SBUFD7(OSDV/P17/OSCDIV/XDSDAT↔) (26)

Bottom pins (left to right, 1–25):
IRQ0(P64↔) (1), IRQ1(P63↔) (2), IRQ2(P62↔) (3), IRQ3(P61↔) (4), IRQ4(P60↔) (5), KEYIRQ4(P54↔) (6), KEYIRQ3(P53↔) (7), KEYIRQ2(P52↔) (8), KEYIRQ1(P51↔) (9), KEYIRQ0(P50↔) (10), NSBTI(P07↔) (11), NSBI1(P06↔) (12), NSBO1(P05↔) (13), NSBT0(P02↔) (14), NSBI0(P01↔) (15), NSBO0(P00↔) (16), SDA(P27↔) (17), SCK(P26↔) (18), HBUFD6BUZZER(P46↔) (19), HBUFD4(P44↔) (20), HBUFD2/DAOUT(P42↔) (21), HBUFD0(P40↔) (22), HSW (23), VLP (24), NRST(P04↔) (25)

QFP100-P-1818B *Lead-free

Support Tool

■ **In-circuit Emulator**	PX-ICE101C / D + PX-PRB101D06-QFP100-P-1818B-M	
■ **Flash Memory Built-in Type**	Type	MN101DF06K [ES (Engineering Sample) available]
	ROM (× 8-bit)	224 K
	RAM (× 8-bit)	6 K
	Minimum instruction execution time	0.1397 µs (at 4.0 V to 5.5 V, 14.32 MHz)
		71.5 µs (at 3.0 V to 5.5 V, fixed to 14.32 MHz internal division)
	Package	QFP100-P-1818B *Lead-free

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