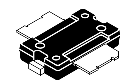
The RF MOSFET Line
RF Power Field Effect Transistor
N-Channel Enhancement-Mode Lateral MOSFET

MRF5S9070NR1

Designed for broadband commercial and industrial applications with frequencies up to 1.0 GHz. The high gain and broadband performance of this device make it ideal for large-signal, common-source amplifier applications in 26 volt base station equipment.

- Typical Single-Carrier N-CDMA Performance @ 880 MHz, V_{DD} = 26 Volts, I_{DQ} = 600 mA, P_{out} = 14 Watts Avg., IS-95 CDMA (Pilot, Sync, Paging, Traffic Codes 8 Through 13)
  Power Gain — 17.8 dB
  Drain Efficiency — 30%
  ACPR @ 750 kHz Offset — -47 dBc @ 30 kHz Bandwidth
- Integrated ESD Protection
- Lead-Free Terminations, 200°C Capable Plastic Package
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 880 MHz, 70 Watts CW Output Power
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R1 Suffix = 500 Units per 24 mm, 13 inch Reel.

880 MHz, 70 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFET



CASE 1265-08, STYLE 1
TO-270-2
PLASTIC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	68	Vdc
Gate-Source Voltage	V_{GS}	- 0.5, +15	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	224 1.28	W W/°C
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value (1)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 70 W CW Case Temperature 80°C, 14 W CW	$R_{\theta JC}$	 0.86 0.99	°C/W

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	A (Minimum)
Charge Device Model	4 (Minimum)

(1) Refer to AN1955/D, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.motorola.com/semiconductors/rf. Select Documentation/Application Notes - AN1955.

NOTE - **CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 68 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 200 μA)	$V_{GS(th)}$	2	2.7	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 600 mAdc)	$V_{GS(Q)}$	—	3.7	—	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.0 Adc)	$V_{DS(on)}$	—	0.18	0.22	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 4 Adc)	g_{fs}	—	4.7	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{iss}	—	126	—	pF
Output Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	34	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	1.37	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) V_{DD} = 26 Vdc, P_{out} = 14 W Avg. N-CDMA, I_{DQ} = 600 mA, f = 880 MHz, Single-Carrier N-CDMA, 1.2288 MHz Channel Bandwidth Carrier, Peak/Avg. Ratio = 9.8 dB @ 0.01% Probability on CCDF					
Power Gain	G_{ps}	17	17.8	—	dB
Drain Efficiency	η_D	29	30	—	%
Adjacent Channel Power Ratio (±750 kHz Offset, 30 kHz Bandwidth)	ACPR	—	-47	-45	dBc
Input Return Loss	IRL	—	-19	-9	dB
TYPICAL GSM CW PERFORMANCE (In Motorola GSM Test Fixture Optimized for 921-960 MHz, 50 ohm system) V_{DD} = 26 Vdc, P_{out} = 60 W, I_{DQ} = 400 mA, f = 921-960 MHz					
Power Gain	G_{ps}	—	16.4	—	dB
Drain Efficiency	η_D	—	62	—	%
Input Return Loss	IRL	—	-12	—	dB
P_{out} @ 1 dB Compression Point (f = 940 MHz)	P1dB	—	68	—	W
TYPICAL GSM EDGE PERFORMANCE (In Motorola GSM EDGE Test Fixture Optimized for 921-960 MHz, 50 ohm system) V_{DD} = 26 Vdc, P_{out} = 25 W Avg., I_{DQ} = 400 mA, f = 921-960 MHz, GSM EDGE Signal					
Power Gain	G_{ps}	—	17	—	dB
Drain Efficiency	η_D	—	44	—	%
Error Vector Magnitude	EVM	—	1.5	—	%
Spectral Regrowth at 400 kHz Offset	SR1	—	-62	—	dBc
Spectral Regrowth at 600 kHz Offset	SR2	—	-78	—	dBc

(continued)

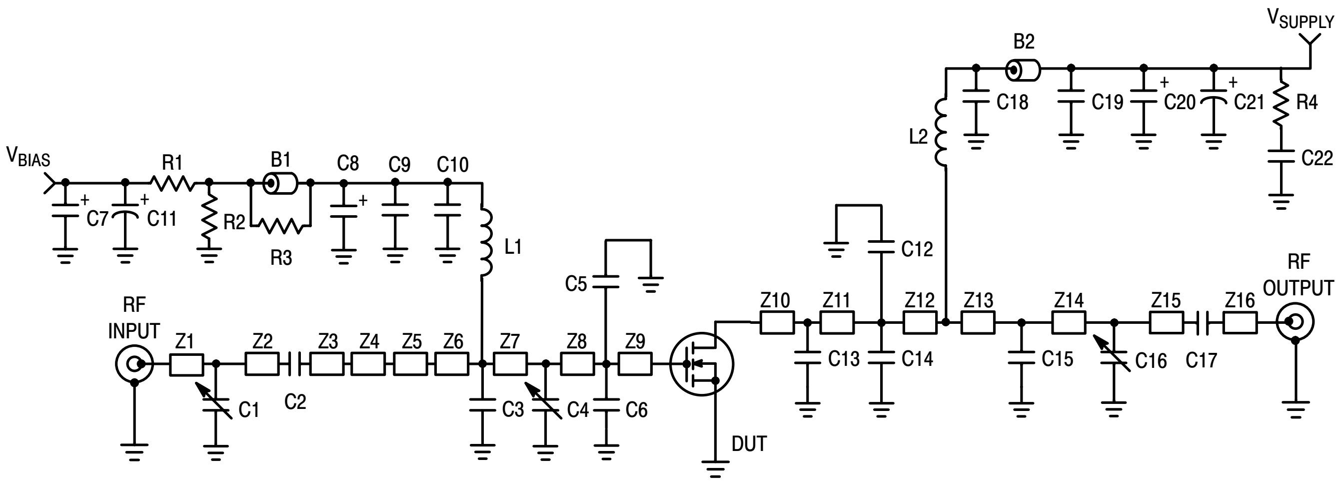
ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

TYPICAL GSM CW PERFORMANCE (In Motorola GSM Test Fixture Optimized for 865-895 MHz, 50 ohm system) V_{DD} = 26 Vdc, P_{out} = 60 W, I_{DQ} = 400 mA, f = 865-895 MHz

Power Gain	G_{ps}	—	16.4	—	dB
Drain Efficiency	η_D	—	59	—	%
Input Return Loss	IRL	—	-15	—	dB
P_{out} @ 1 dB Compression Point (f = 880 MHz)	P1dB	—	71	—	W

TYPICAL GSM EDGE PERFORMANCE (In Motorola GSM EDGE Test Fixture Optimized for 865-895 MHz, 50 ohm system) V_{DD} = 26 Vdc, P_{out} = 25 W Avg., I_{DQ} = 400 mA, f = 865-895 MHz, GSM EDGE Signal

Power Gain	G_{ps}	—	17	—	dB
Drain Efficiency	η_D	—	41	—	%
Error Vector Magnitude	EVM	—	1.35	—	%
Spectral Regrowth at 400 kHz Offset	SR1	—	-66	—	dBc
Spectral Regrowth at 600 kHz Offset	SR2	—	-81	—	dBc



Z1	0.140″ x 0.060″ Microstrip	Z10	0.245″ x 0.270″ Microstrip
Z2	0.141″ x 0.060″ Microstrip	Z11	0.110″ x 0.270″ Microstrip
Z3	0.280″ x 0.060″ Microstrip	Z12	0.055″ x 0.270″ Microstrip
Z4	0.500″ x 0.100″ Microstrip	Z13	0.512″ x 0.060″ Microstrip
Z5	0.530″ x 0.270″ Microstrip	Z14	0.106″ x 0.060″ Microstrip
Z6	0.155″ x 0.270″ x 0.530″ Taper	Z15	0.930″ x 0.060″ Microstrip
Z7	0.376″ x 0.530″ Microstrip	Z16	0.365″ x 0.060″ Microstrip
Z8	0.116″ x 0.530″ Microstrip	PCB	Taconic RF-35, 0.030″, ε_r = 3.5
Z9	0.055″ x 0.530″ Microstrip		

Figure 1. MRF5S9070NR1 Test Circuit Schematic

Table 1. MRF5S9070NR1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1	Small Ferrite Bead, Surface Mount	2743019447	Fair-Rite
B2	Large Ferrite Bead, Surface Mount	2743021447	Fair-Rite
C1	0.6-6.0 pF Variable Capacitor, Gigatrim	272715L	Johanson
C2	16 pF Chip Capacitor, B Case	100B160JP500X	ATC
C3	7.5 pF Chip Capacitor, B Case	100B7R5JP500X	ATC
C4, C16	0.8-8.0 pF Variable Capacitor, Gigatrim	272915L	Johanson
C5, C6	15 pF Chip Capacitors, B Case	100B150JP500X	ATC
C7, C8, C20	10 μF, 35 V Tantalum Capacitors	T491D106K035AS	Kemet
C9, C19, C22	0.58 μF Chip Capacitors	700A561MP150X	ATC
C10, C18	18 pF Chip Capacitors, B Case	100B180JP500X	ATC
C11	100 μF, 50 V Electrolytic Capacitor	515D107M050BB6A	Vishay-Dale
C12	0.7 pF Chip Capacitor, B Case	100B0R7BP500X	ATC
C13, C14	13 pF Chip Capacitors, B Case	100B130JP500X	ATC
C15	3.9 pF Chip Capacitor, B Case	100B3R9JP500X	ATC
C17	22 pF Chip Capacitor, B Case	100B180JP500X	ATC
C21	470 μF, 63 V Electrolytic Capacitor	SME63VB471M12X25LL	United Chemi-Con
L1, L2	12.5 nH Surface Mount Inductors	A04T-5	Coilcraft
R1	1 kΩ Chip Resistor	CRCW12061001F100	Vishay-Dale
R2	560 kΩ Chip Resistor	CRCW12065603F100	Vishay-Dale
R3	12 Ω Chip Resistor	CRCW120612R0F100	Vishay-Dale
R4	27 Ω Chip Resistor	CRCW120627R0F100	Vishay-Dale

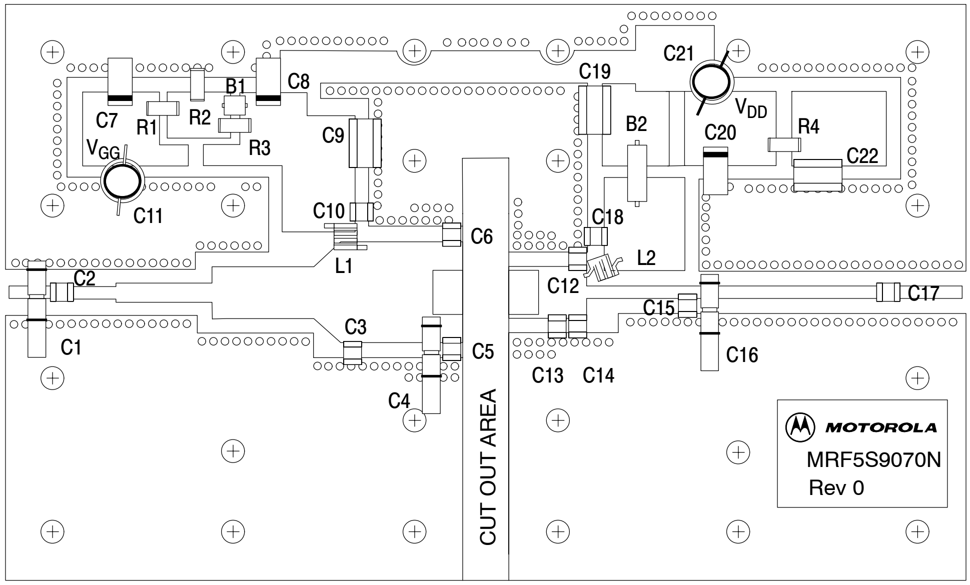


Figure 2. MRF5S9070NR1 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

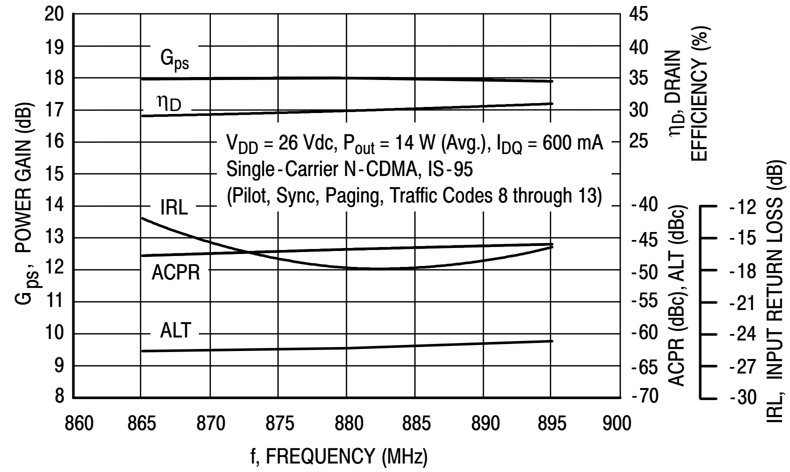


Figure 3. Class AB Broadband Performance

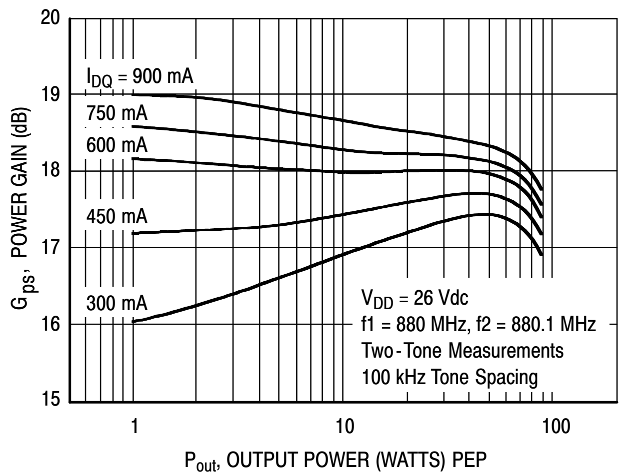


Figure 4. Two-Tone Power Gain versus Output Power

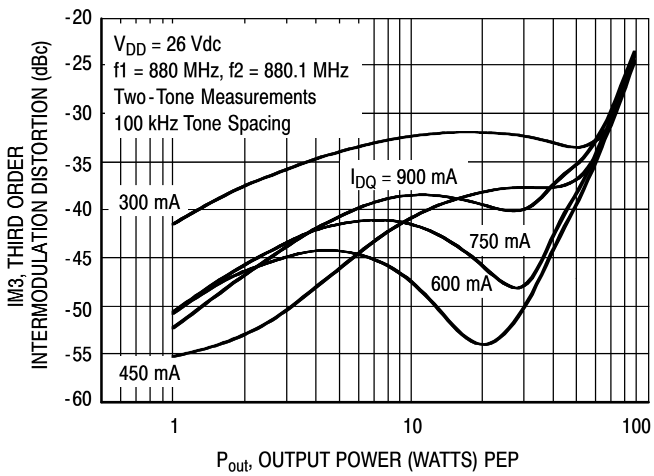


Figure 5. Third Order Intermodulation Distortion versus Output Power

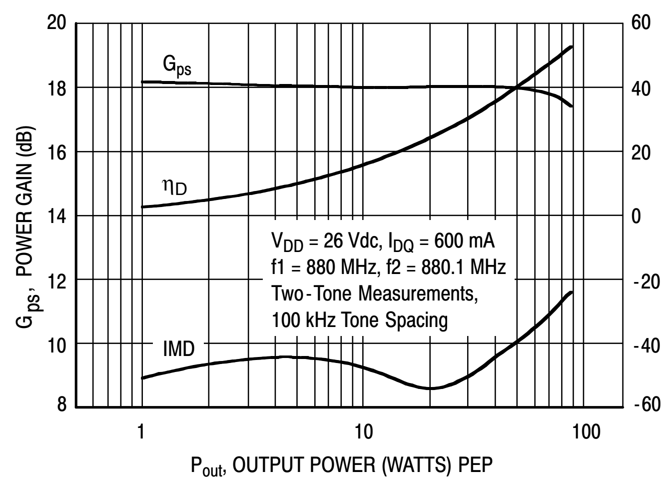


Figure 6. Power Gain, Drain Efficiency and IMD versus Output Power

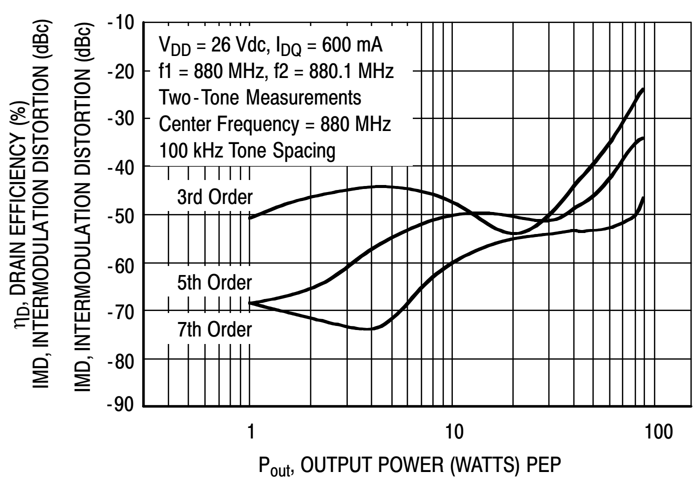


Figure 7. Intermodulation Distortion Products versus Output Power

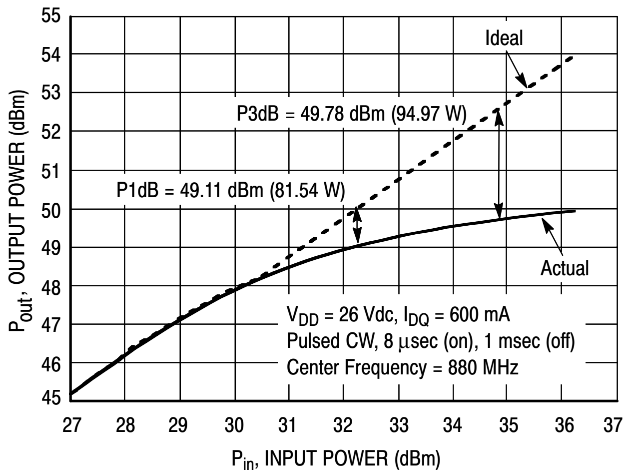


Figure 8. Pulse CW Output Power versus Input Power

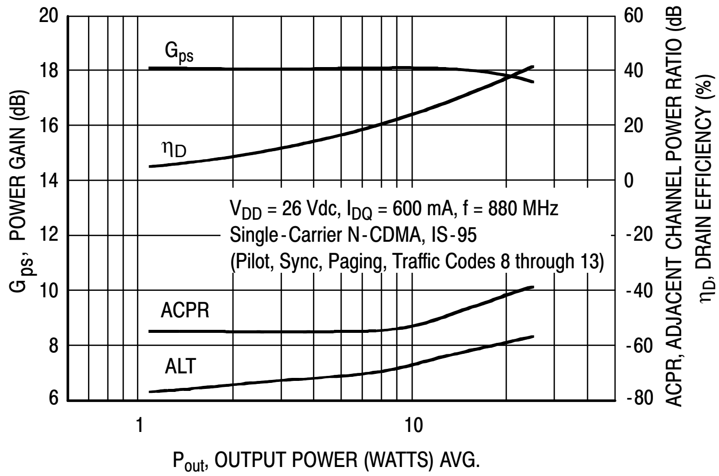


Figure 9. N-CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

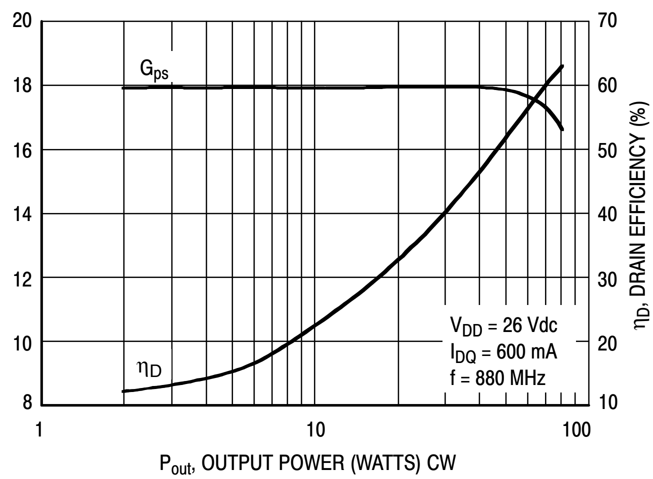
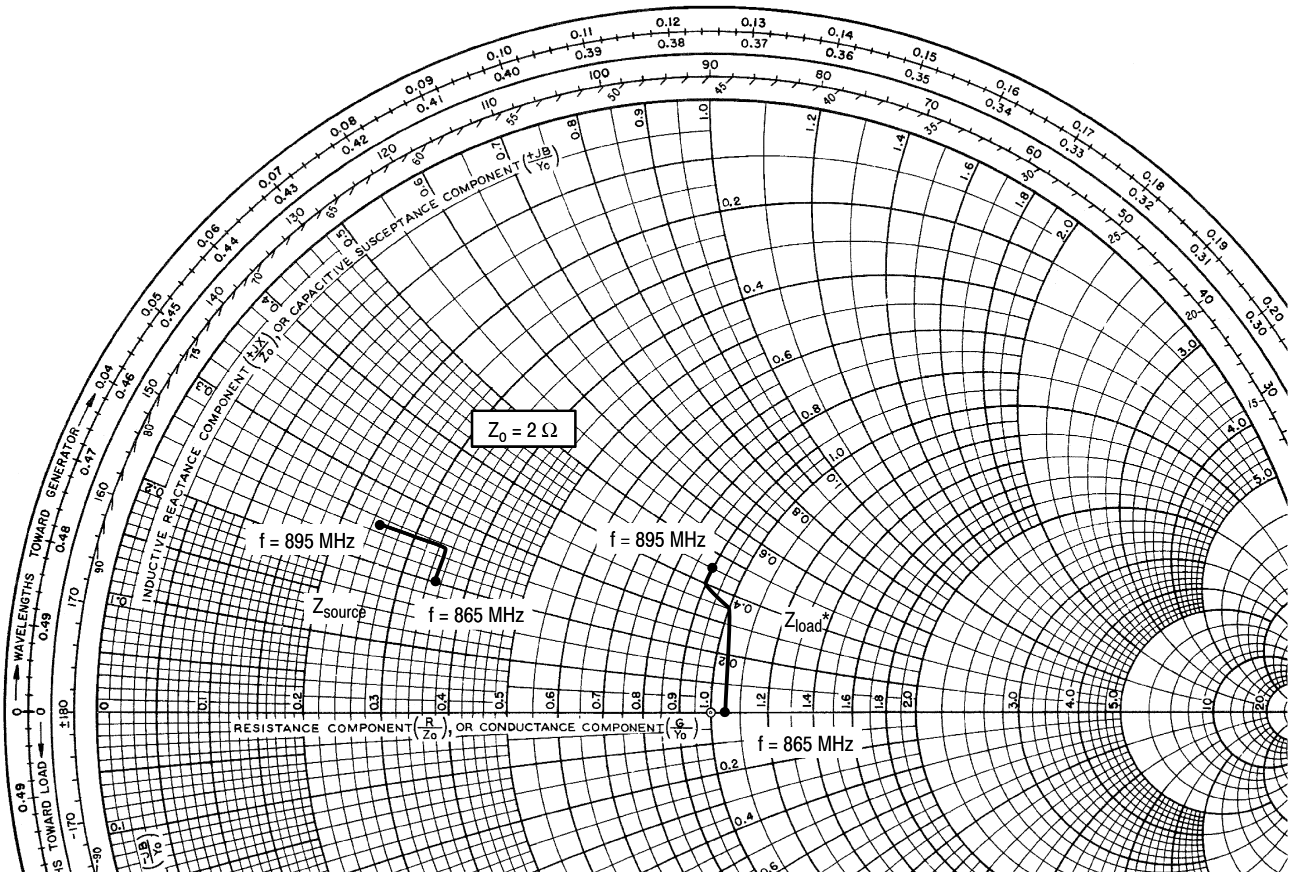


Figure 10. Power Gain and Drain Efficiency versus CW Output Power



V_{DD} = 26 Vdc, I_{DQ} = 600 mA, P_{out} = 14 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
865	0.7 + j0.4	2.1 + j0.6
875	0.7 + j0.5	2.0 + j0.7
885	0.6 + j0.5	1.8 + j0.8
895	0.5 + j0.5	1.8 + j0.9

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

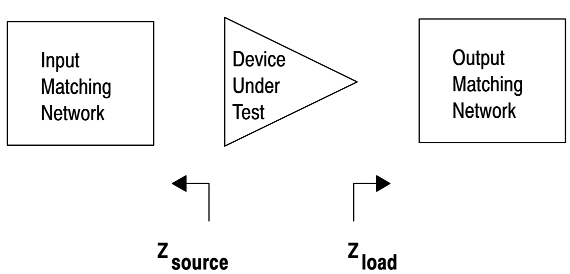
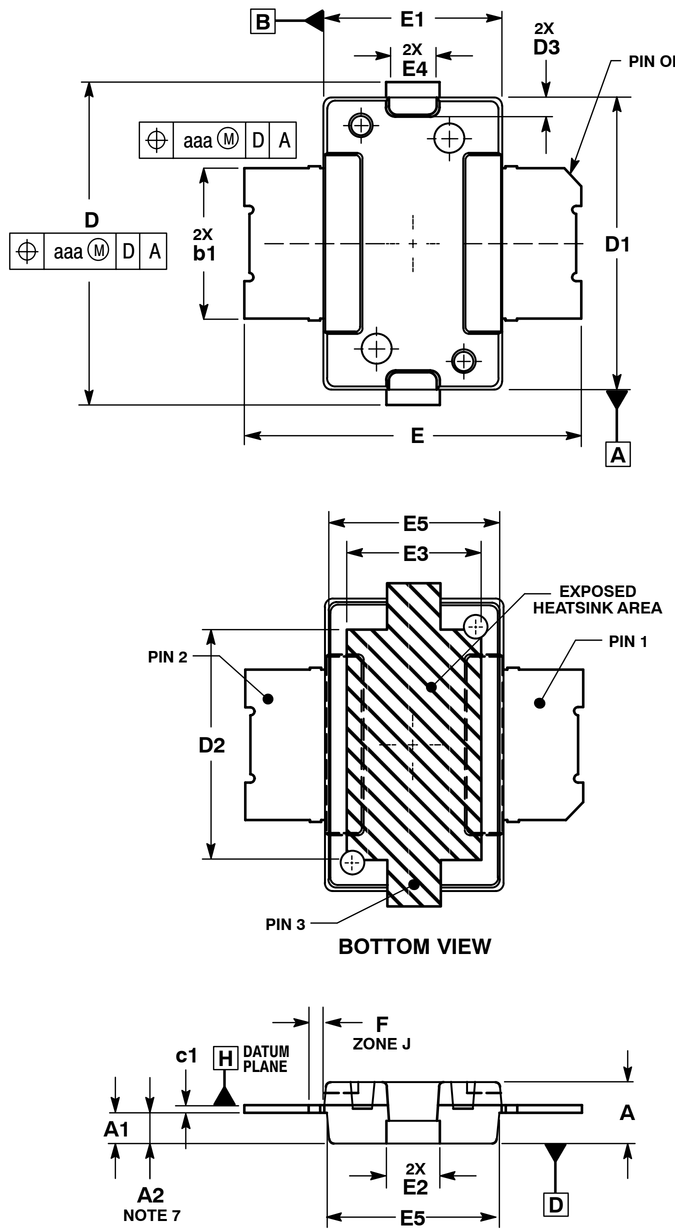


Figure 11. Series Equivalent Source and Load Impedance

NOTES

NOTES

PACKAGE DIMENSIONS



NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS “D1” AND “E1” DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS “D1” AND “E1” DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b1 DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE “J” ONLY.
8. DIMENSIONS “D” AND “E2” DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .003 PER SIDE. DIMENSIONS “D” AND “E2” DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -D-.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.078	.082	1.98	2.08
A1	.039	.043	0.99	1.09
A2	.040	.042	1.02	1.07
D	.416	.424	10.57	10.77
D1	.378	.382	9.60	9.70
D2	.290	.320	7.37	8.13
D3	.016	.024	0.41	0.61
E	.436	.444	11.07	11.28
E1	.238	.242	6.04	6.15
E2	.066	.074	1.68	1.88
E3	.150	.180	3.81	4.57
E4	.058	.066	1.47	1.68
E5	.231	.235	5.87	5.97
F	.025 BSC		0.64 BSC	
b1	.193	.199	4.90	5.06
c1	.007	.011	0.18	0.28
aaa	.004		0.10	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 1265-08
ISSUE G
TO-270-2
PLASTIC

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