MT92210

Carrier Class VoIP Processor

Advance Datasheet

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Introduction

The MT92210 is an assembly and disassembly engine that can convert up to 1023 full-duplex TDM voice channels to IP packets and back, according to the H.225 standard. The device communicates via an H.1x0 TDM bus on the WAN Access side, carrying voice in plain PCM format, ADPCM or HDLC-encapsulated mini-packets.

On the Packet Switch Fabric side, the MT92210 can carry IP packets over Ethernet, ATM (using AAL5 cells) or Packet over SONET. A 16 bit Intel/Motorola CPU interface is used to access and configure the device. Finally, up to 12 SRAMs and 2 SDRAMs can be used as external memory configuration and storage space.

The MT92210 offers significant savings in systems cost and system simplicity through reduced component count and simplified software.

Features

General

- Up to 1023 Full-duplex PCM or ADPCM Voice Channels over IP/UDP/RTP connections
- Up to 4096 HDLC channels carrying UDP payload converted to IP/UDP connections
- Simultaneous support of PCM, ADPCM and HDLC Connections
- 16-bit Intel/Motorola CPU Interface
- Fully H.1x0 compliant TDM interface
- Network Interface A: UTOPIA Level 1/2, POS-PHY Level 2 or MII
- Network Interface B: UTOPIA Level 1
- Two to eight 18 bit data bus ZBT SSRAMs, each ranging in size from 128K to 1M bytes
- One to four 36 bit data bus ZBT SSRAMs, each ranging in size from 128K to 1M bytes
- Two 16 bit data bus SDRAMs, each ranging in size from 8M to 16M bytes

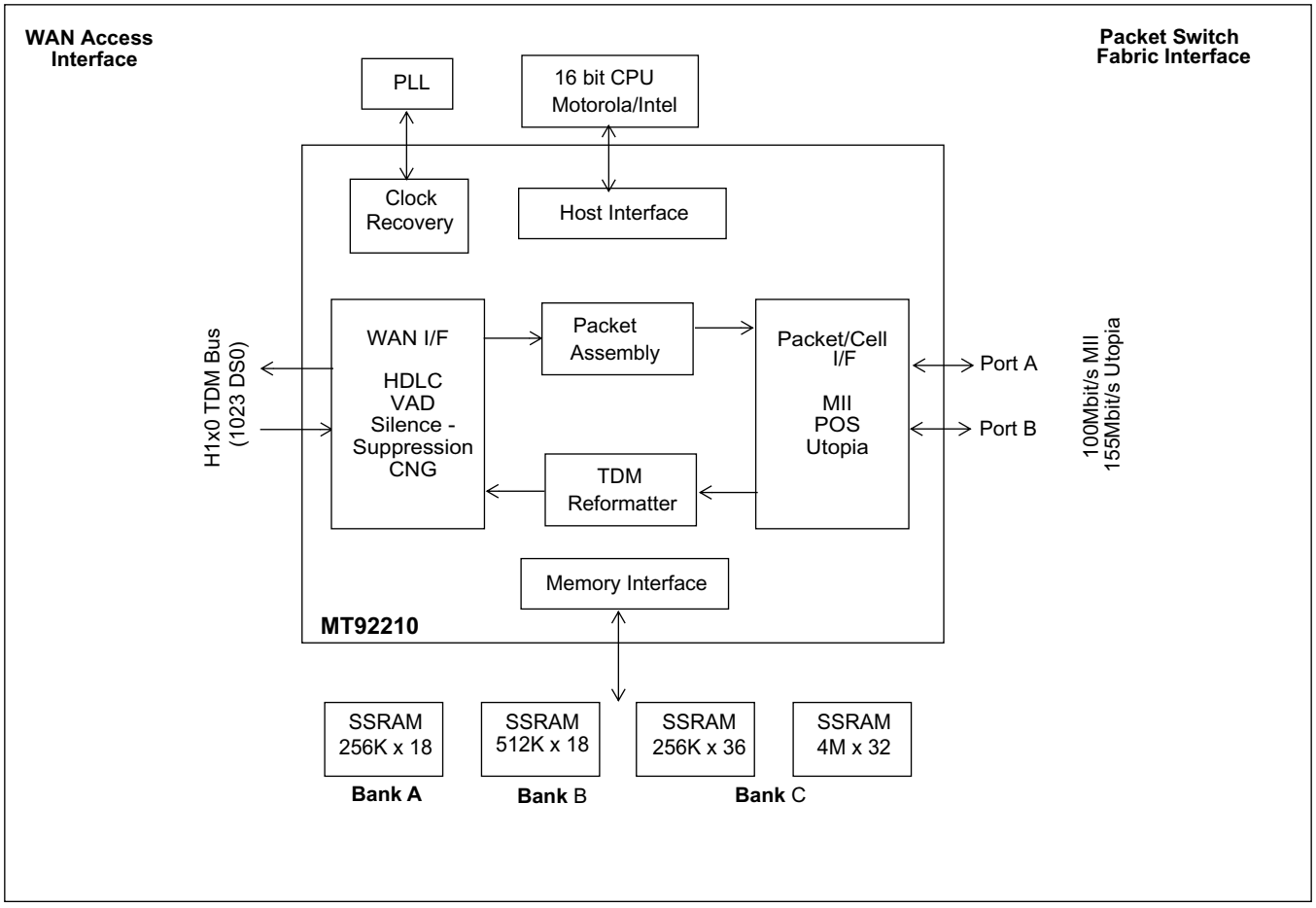

Figure 1 - MT92210 VOIP Processor

Data Formats

- Simultaneous Support of IP versions 4 and 6
- Support for RTP, UDP and IP to support H.225
- IP packets can be sent over 3 different types of physical links (Ethernet, Utopia, Packet over SONET)
- RTP packaging is optional per connection
- IP over AAL5 can be performed using Classical IP over ATM with SNAP/LLC headers or Ethernet LAN Emulation (LANE)
- Support of MPLS & MPOA on reception
- Quality of service can de determined using Ethernet user priority or IP Type Of Service (TOS)

SAR Functions

- Up to 4096 connections using HDCC mini-packets
- Up to 1023 PCM/ADPCM channels
- HDLC packets containing UDP payload converted to IP/UDP datagrams
- Packets sizes up to 1500 bytes
- Jitter Absorption Buffer size up to 8192 bytes allows absorption of ±512 ms of PDV
- Injection of CPU-generated RTP packets
- Reception of CPU-destined RTP packets in buffers of up to 64K bytes
- Packet loss & miss-insertion compensation for PCM and ADPCM packets
- Network jitter monitoring allows support of RTCP for PCM, ADPCM, HDLC and CPU connections

Network Functions

- Off-the-shelf AAL5 SAR can be used to terminate data connections on a PCI bus
- Look-up can be performed on a priority basis: for example, a packet can be looked-up using only IP and UDP headers, then the look-up result can request a second lookup using IP, UDP and RTP headers
- IP, UDP and RTP header verification performed
- Payload type & Marker bit routing allows different compression formats as well as signaling packets to be transported on the same connection

Silence Suppression and Padding

- Proprietary Adaptive Silence Suppression
- Supported in both PCM and ADPCM formats
- Built-in detection of energy level
- Padding with matched energy "comfort noise"
- 32 large "comfort noise" buffers (16Kb to 64Kb)
- Suppression indication can be generated by chip or fed externally to synchronize with off-chip compression codecs

H.1x0 Interface

- Fully H.110/H.100 compatible
- H.1x0 Master and Slave capability
- Support of message channel
- Low Latency Loop-back, H.1x0 to H.1x0, of 128 channels (delay <= 375 us)
- Redundant Adaptive Clock Recovery Circuit
- Support of 2/4/8 MHz bus speed in groups of 4 streams (8 separate groups)
- Generation of H.1x0 compatibility signals

TDM data formats

- Support of plain PCM in u-law and A-law
- Translation between u-law and A-law on a per connection basis
- Support of ADPCM at 40, 32, 24 or 16 kbps
- Support of HDLC encapsulated mini-packets with asynchronous timing
- Support of HDLC streams ranging from 1 to 1023 time slots
- Support of HDLC packets up to 1500 bytes in length

Link Interface

- Ethernet: support of MII interface
- ATM: twin UTOPIA interfaces allow secondary data SAR to be daisy-chained with device for data connections
- Packet over SONET: support of 16-bit POS-PHY bus allowing interoperation with PHYs at speeds up to 155 Mbps
- Secondary UTOPIA port can be used in all modes, allowing the same data support architecture to be used independently of the link layer with minimal changes
- Transmission of voice to secondary port allows H.1x0/PCM bridging when coupled with AAL5 SAR
- Chip's pin-out allows designs that support Ethernet, ATM and Packet over SONET with only software configuration deciding on the link layer used

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