FAIRCHILD SEMICONDUCTOR™

April 2000
Revised February 2002

# NC7WZ132
# TinyLogic™ UHS Dual 2-Input NAND Gate with Schmitt Trigger Inputs

## General Description

The NC7WZ132 is a dual 2-Input NAND Gate from Fairchild's Ultra High Speed Series of TinyLogic™. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a broad $V_{CC}$ operating range. The device is specified to operate over the 1.65V to 5.5V $V_{CC}$ operating range. The inputs and output are high impedance when $V_{CC}$ is 0V. Inputs tolerate voltages up to 7V independent of $V_{CC}$ operating voltage. Schmitt trigger inputs achieve typically 1V hysteresis between the positive-going and negative-going input threshold voltage at 5V $V_{CC}$.

## Features

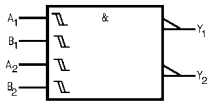
- Space saving US8 surface mount package
- Ultra High Speed; $t_{PD}$ 3.1 ns typ into 50 pF at 5V $V_{CC}$
- High Output Drive; ±24 mA at 3V $V_{CC}$
- Broad $V_{CC}$ Operating Range; 1.65V–5.5V
- Matches the performance of LCX when operated at 3.3V $V_{CC}$
- Power down high impedance inputs/output
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented
- Schmitt trigger inputs are tolerant of slow changing input signals

## Ordering Code:

| Order Number | Package Number | Product Code Top Mark | Package Description | Supplied As |
|---|---|---|---|---|
| NC7WZ132K8X | MAB08A | WZD2 | 8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide | 3k Units on Tape and Reel |

## Logic Symbol

**IEEE/IEC**




## Pin Descriptions

| Pin Names | Description |
|---|---|
| $A_n$, $B_n$ | Inputs |
| $Y_n$ | Output |

## Function Table

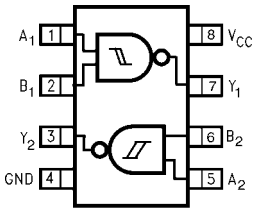
$$Y = \overline{AB}$$

| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

H = HIGH Logic Level L = LOW Logic Level

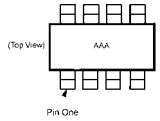
TinyLogic™ is a trademark of Fairchild Semiconductor Corporation.

## Connection Diagrams




**(Top View)**

**Pin One Orientation Diagram**




AAA represents Product Code Top Mark - see ordering code

**Note:** Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

## Absolute Maximum Ratings (Note 1)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +7V |
| DC Input Voltage ($V_{IN}$) | −0.5V to +7V |
| DC Output Voltage ($V_{OUT}$) | −0.5V to +7V |
| DC Input Diode Current ($I_{IK}$) | |
| @$V_{IN}$ < −0.5V | −50 mA |
| DC Output Diode Current ($I_{OK}$) | |
| @$V_{OUT}$ < −0.5V | −50 mA |
| DC Output Current ($I_{OUT}$) | ± 50 mA |
| DC $V_{CC}$/GND Current ($I_{CC}$/$I_{GND}$) | ± 100 mA |
| Storage Temperature ($T_{STG}$) | −65°C to +150°C |
| Junction Temperature under Bias ($T_J$) | 150°C |
| Junction Lead Temperature ($T_L$); | |
| (Soldering, 10 seconds) | 260°C |
| Power Dissipation ($P_D$) @ +85°C | 250 mW |

## Recommended Operating Conditions (Note 2)

| | |
|---|---|
| Supply Voltage Operating ($V_{CC}$) | 1.65V to 5.5V |
| Supply Voltage Data Retention ($V_{CC}$) | 1.5V to 5.5V |
| Input Voltage ($V_{IN}$) | 0V to 5.5V |
| Output Voltage ($V_{OUT}$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | −40°C to +85°C |
| Thermal Resistance ($\theta_{JA}$) | 250°C/W |

**Note 1:** Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

**Note 2:** Unused inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ | $T_A$ = +25°C | | | $T_A$ = −40°C to +85°C | | Units | Conditions | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | (V) | Min | Typ | Max | Min | Max | | | |
| $V_P$ | Positive Threshold | 1.65 | 0.6 | 0.99 | 1.4 | 0.6 | 1.4 | | | |
| | Voltage | 2.3 | 1.0 | 1.39 | 1.8 | 1.0 | 1.8 | | | |
| | | 3.0 | 1.3 | 1.77 | 2.2 | 1.3 | 2.2 | V | | |
| | | 4.5 | 1.9 | 2.49 | 3.1 | 1.9 | 3.1 | | | |
| | | 5.5 | 2.2 | 2.96 | 3.6 | 2.2 | 3.6 | | | |
| $V_N$ | Negative Threshold | 1.65 | 0.2 | 0.53 | 0.9 | 0.2 | 0.9 | | | |
| | Voltage | 2.3 | 0.4 | 0.78 | 1.15 | 0.4 | 1.15 | | | |
| | | 3.0 | 0.6 | 1.02 | 1.5 | 0.6 | 1.5 | V | | |
| | | 4.5 | 1.0 | 1.48 | 2.0 | 1.0 | 2.0 | | | |
| | | 5.5 | 1.2 | 1.76 | 2.3 | 1.2 | 2.3 | | | |
| $V_H$ | Hysteresis Voltage | 1.65 | 0.15 | 0.46 | 0.9 | 0.15 | 0.9 | | | |
| | | 2.3 | 0.25 | 0.61 | 1.1 | 0.25 | 1.1 | | | |
| | | 3.0 | 0.4 | 0.75 | 1.2 | 0.4 | 1.2 | V | | |
| | | 4.5 | 0.6 | 1.01 | 1.5 | 0.6 | 1.5 | | | |
| | | 5.5 | 0.7 | 1.20 | 1.7 | 0.7 | 1.7 | | | |
| $V_{OH}$ | HIGH Level Output | 1.65 | 1.55 | 1.65 | | 1.55 | | | | |
| | Voltage | 2.3 | 2.2 | 2.3 | | 2.2 | | | | |
| | | 3.0 | 2.9 | 3.0 | | 2.9 | | V | $V_{IN}$ = $V_{IL}$ | $I_{OH}$ = −100 µA |
| | | 4.5 | 4.4 | 4.5 | | 4.4 | | | | |
| | | 1.65 | 1.29 | 1.52 | | 1.29 | | | | $I_{OH}$ = −4 mA |
| | | 2.3 | 1.9 | 2.15 | | 1.9 | | | | $I_{OH}$ = −8 mA |
| | | 3.0 | 2.4 | 2.80 | | 2.4 | | V | | $I_{OH}$ = −16 mA |
| | | 3.0 | 2.3 | 3.68 | | 2.3 | | | | $I_{OH}$ = −24 mA |
| | | 4.5 | 3.8 | 4.20 | | 3.8 | | | | $I_{OH}$ = −32 mA |
| $V_{OL}$ | LOW Level Output | 1.65 | | 0.0 | 0.10 | | 0.10 | | | |
| | Voltage | 2.3 | | 0.0 | 0.10 | | 0.10 | | | |
| | | 3.0 | | 0.0 | 0.10 | | 0.10 | V | $V_{IN}$ = $V_{IH}$ | $I_{OL}$ = 100 µA |
| | | 4.5 | | 0.0 | 0.10 | | 0.10 | | | |
| | | 1.65 | | 0.08 | 0.24 | | 0.24 | | | $I_{OL}$ = 4 mA |
| | | 2.3 | | 0.10 | 0.3 | | 0.3 | | | $I_{OL}$ = 8 mA |
| | | 3.0 | | 0.15 | 0.4 | | 0.4 | V | | $I_{OL}$ = 16 mA |
| | | 3.0 | | 0.22 | 0.55 | | 0.55 | | | $I_{OL}$ = 24 mA |
| | | 4.5 | | 0.22 | 0.55 | | 0.55 | | | $I_{OL}$ = 32 mA |
| $I_{IN}$ | Input Leakage Current | 0-5.5 | | | ±0.1 | | ±1 | µA | $V_{IN}$ = 5.5V, GND | |
| $I_{OFF}$ | Power Off Leakage Current | 0.0 | | | 1 | | 10 | µA | $V_{IN}$ or $V_{OUT}$ = 5.5V | |

## DC Electrical Characteristics (Continued)

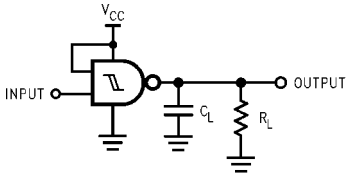
| Symbol | Parameter | $V_{CC}$ (V) | $T_A = +25°C$ | | | $T_A = -40°C$ to $+85°C$ | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | | |
| $I_{CC}$ | Quiescent Supply Current | 1.65 to 5.5 | | | 1 | | 10 | μA | $V_{IN}$ = 5.5V, GND |

## AC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | $T_A = +25°C$ | | | $T_A = -40°C$ to $+85°C$ | | Units | Conditions | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay | 1.8 ± 0.15 | 3.0 | 7.1 | 13.0 | 3.0 | 13.5 | ns | $C_L$ = 15 pF, $R_L$ = 1 MΩ | Figures 1, 3 |
| | | 2.5 ± 0.2 | 2.0 | 4.5 | 7.5 | 2.0 | 8.0 | | | |
| | | 3.3 ± 0.3 | 1.2 | 3.4 | 5.0 | 1.2 | 5.5 | | | |
| | | 5.0 ± 0.5 | 0.8 | 2.6 | 3.8 | 0.8 | 4.2 | | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay | 3.3 ± 0.3 | 1.8 | 4.0 | 5.8 | 1.8 | 6.3 | ns | $C_L$ = 50 pF, $R_L$ = 500Ω | Figures 1, 3 |
| | | 5.0 ± 0.5 | 1.2 | 3.1 | 4.5 | 1.2 | 4.9 | | | |
| $C_{IN}$ | Input Capacitance | 0 | | 2.5 | | | | pF | | |
| $C_{PD}$ | Power Dissipation Capacitance | 3.3 | | 15 | | | | pF | (Note 3) | Figure 2 |
| | | 5.0 | | 18 | | | | | | |

**Note 3:** $C_{PD}$ is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption ($I_{CCD}$) at no output loading and operating at 50% duty cycle. (See Figure 2.) $C_{PD}$ is related to $I_{CCD}$ dynamic operating current by the expression: $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC}static)$.

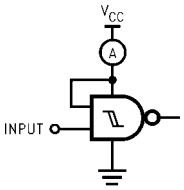
## AC Loading and Waveforms




$C_L$ includes load and stray capacitance

Input PRR = 1.0 MHz; $t_w$ = 500 ns

**FIGURE 1. AC Test Circuit**




Input = AC Waveform; $t_r = t_f$ = 1.8 ns;

PRR = 10 MHz; Duty Cycle = 50%

**FIGURE 2. $I_{CCD}$ Test Circuit**

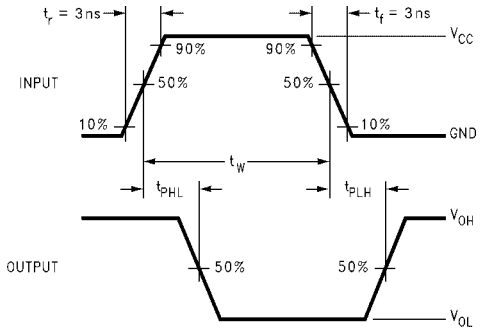


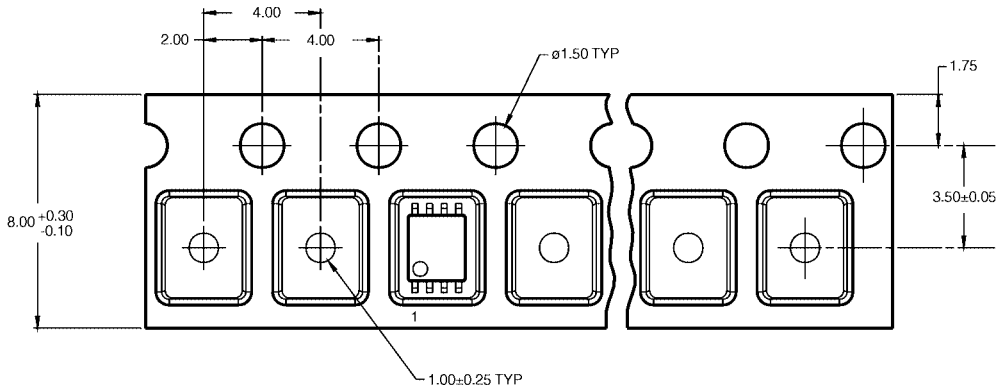

**FIGURE 3. AC Waveforms**

## Tape and Reel Specification

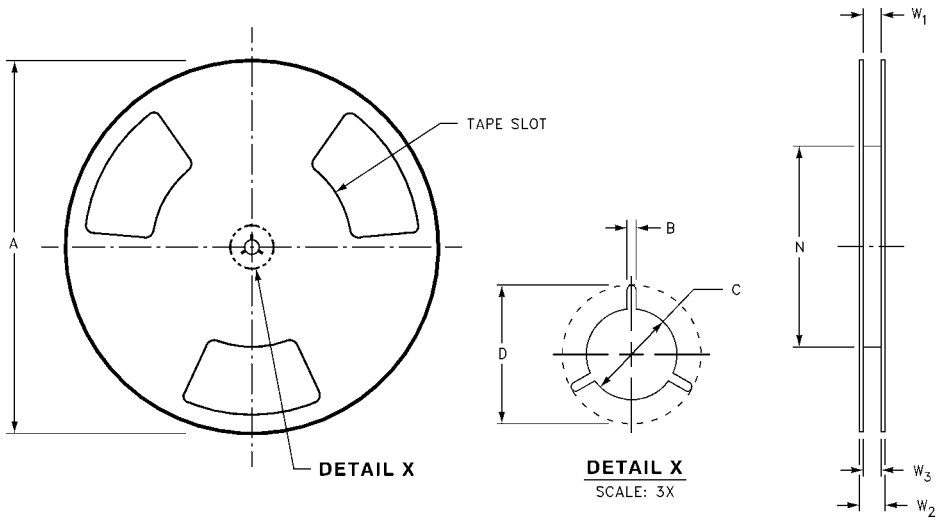
**Tape Format**

| Package Designator | Tape Section | Number Cavities | Cavity Status | Cover Tape Status |
|---|---|---|---|---|
| K8X | Leader (Start End) | 125 (typ) | Empty | Sealed |
| | Carrier | 3000 | Filled | Sealed |
| | Trailer (Hub End) | 75 (typ) | Empty | Sealed |

**TAPE DIMENSIONS** inches (millimeters)

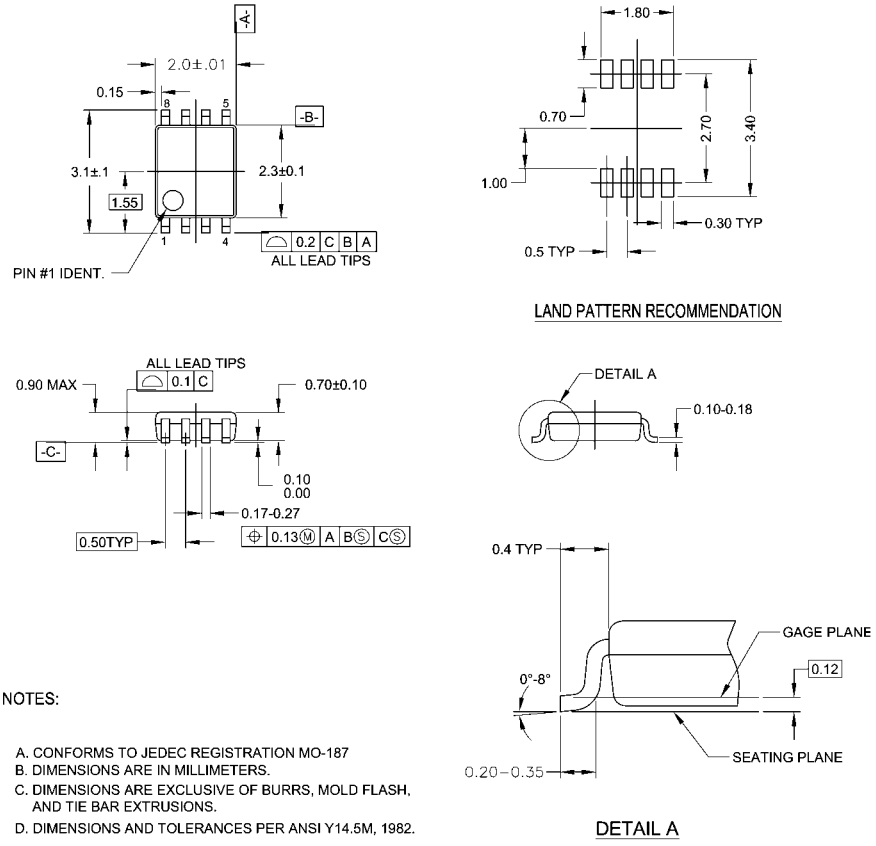



**REEL DIMENSIONS** inches (millimeters)




| Tape Size | A | B | C | D | N | W1 | W2 | W3 |
|---|---|---|---|---|---|---|---|---|
| 8 mm | 7.0 (177.8) | 0.059 (1.50) | 0.512 (13.00) | 0.795 (20.20) | 2.165 (55.00) | 0.331 + 0.059/–0.000 (8.40 + 1.50/–0.00) | 0.567 (14.40) | W1 + 0.078/–0.039 (W1 + 2.00/–1.00) |

## Physical Dimensions inches (millimeters) unless otherwise noted




NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-187
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVC

**8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide**
**Package Number MAB08A**



**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**www.fairchildsemi.com**