# DATA SHEET

## NE5537
## Sample-and-hold amplifier

Product data
Supersedes data of 1994 Aug 31
File under Integrated Circuits, IC11 Handbook

2001 Aug 03

Philips
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# Sample-and-hold amplifier NE5537

## DESCRIPTION

The NE5537 monolithic sample-and-hold amplifier combines the best features of ion-implanted JFETs with bipolar devices to obtain high accuracy, fast acquisition time, and low droop rate. This device is pin-compatible with the LF198, and features superior performance in droop rate and output drive capability. The circuit shown in Figure 5 contains two operational amplifiers which function as a unity gain amplifier in the sample mode. The first amplifier has bipolar input transistors which give the system a low offset voltage. The second amplifier has JFET input transistors to achieve low leakage current from the hold capacitor. A unique circuit design for leakage current cancellation using current mirrors gives the NE5537 a low droop rate at higher temperature. The output stage has the capability to drive a 2 kΩ load. The logic input is compatible with TTL, PMOS or CMOS logic. The differential logic threshold is 1.4 V with the sample mode occurring when the logic input is high. It is available in 8-pin plastic DIP and 14-pin SO packages.

## FEATURES

- Operates from ±5 V to ±18 V supplies
- Hold leakage current 6 pA @ $T_j$ = 25 °C
- Less than 4 μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5 mV typical hold step at $C_H$ = 0.01 μF
- Low input offset: 1 MV (typical)
- 0.002% gain accuracy with $R_L$ = 2 kΩ
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

## PIN CONFIGURATIONS

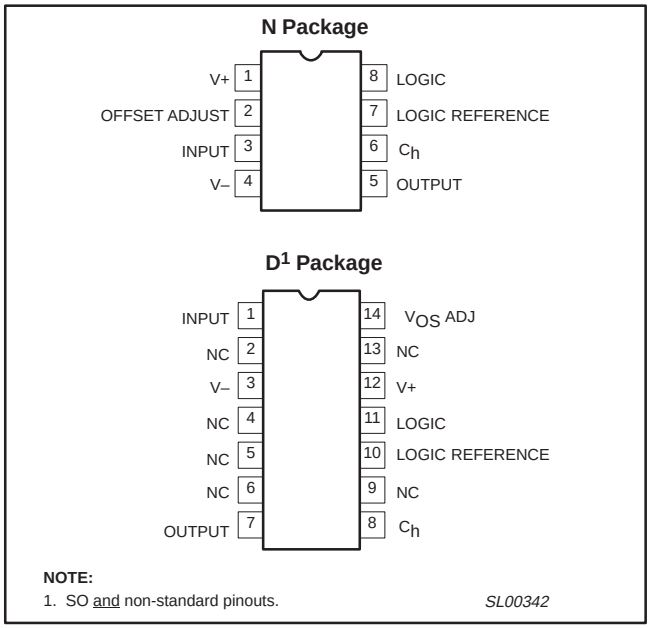



**Figure 1. Pin Configuration**

## BLOCK DIAGRAM

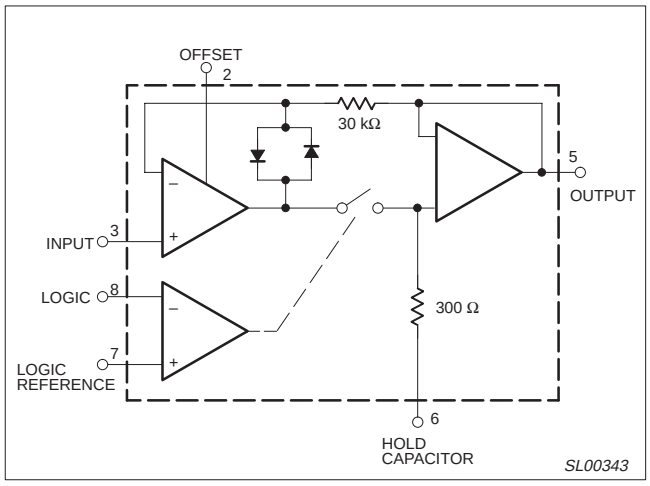



**Figure 2. Block Diagram**

## ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE | DWG # |
|---|---|---|---|
| 8-Pin Plastic Dual In-Line Package (DIP) | 0 °C to +70 °C | NE5537N | SOT97-1 |
| 14-Pin Plastic Small Outline (SO) Package | 0 °C to +70 °C | NE5537D | SOT108-1 |

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_S$ | Voltage supply | ±18 | V |
| $P_D$ | Maximum power dissipation; $T_{amb}$ = 25 °C (still-air)[1]<br>N package<br>D package | <br>1160<br>1090 | <br>mW<br>mW |
| $V_{IN}$ | Input voltage | Equal to supply voltage | |
| | Logic to logic reference differential voltage[2] | +7, –30 | V |
| | Output short circuit duration | Indefinite | |
| | Hold capacitor short circuit duration | 10 | s |
| $T_{amb}$ | Operating ambient temperature range | 0 to +70 | °C |
| $T_{stg}$ | Storage temperature range | –65 to +150 | °C |
| $T_{sld}$ | Lead soldering temperature (10 sec max) | 230 | °C |

**NOTES:**
1. Derate above 25°C at the following rates:
   N package at 9.3 mW/°C
   D package at 8.3 mW/°C
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2 V below the positive supply and 3 V above the negative supply.

## DC ELECTRICAL CHARACTERISTICS[1]

| SYMBOL | PARAMETER | TEST CONDITIONS | Limits | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{OS}$ | Input offset voltage[4] | $T_j$ = 25 °C<br>Full temperature range | | 2 | 7<br>10 | mV<br>mV |
| $I_{BIAS}$ | Input bias current[4] | $T_j$ = 25 °C<br>Full temperature range | | 10 | 50<br>100 | nA<br>nA |
| | Input impedance | $T_j$ = 25 °C | | $10^{10}$ | | Ω |
| | Gain error | $T_j$ = 25 °C<br>–10 V ≤ $V_{IN}$ ≤ 10 V; $R_L$ = 2 kΩ<br>–11.5 V ≤ $V_{IN}$ ≤ 11.5 V; $R_L$ = 10 kΩ<br>Full temperature range | | 0.004 | 0.01<br><br><br>0.02 | %<br><br><br>% |
| | Feedthrough attenuation ratio at 1kHz | $T_j$ = 25 °C, $C_H$ = 0.01 µF | 80 | 90 | | dB |
| | Output impedance | $T_j$ = 25 °C; "HOLD" mode<br>Full temperature range | | 0.5 | 4<br>6 | Ω |
| | "HOLD" Step[2] | $T_j$ = 25 °C; $C_H$ = 0.01 µF; $V_{OUT}$= 0 V | | 1.0 | 2.5 | mV |
| $I_{CC}$ | Supply current[4] | $T_j$ = 25 °C | | 4.5 | 7.5 | mA |
| | Logic and logic reference input current | $T_j$ = 25 °C | | 2 | 10 | µA |
| | Leakage current into hold capacitor[4] | $T_j$ = 25 °C "hold" mode[3] | | 6 | 100 | pA |
| | Acquisition time to 0.1% | $V_{OUT}$ = 10 V;<br>$C_H$ = 1000 pF<br>$C_H$ = 0.01 µF | | 4<br><br>20 | | µs<br><br>µs |
| | Hold capacitor charging current | $V_{IN}$–$V_{OUT}$ = 2 V | | 5 | | mA |
| SVRR | Supply voltage rejection ratio | $V_{OUT}$ = 0 V | 80 | 110 | | dB |
| | Differential logic threshold | $T_j$ = 25 °C | 0.8 | 1.4 | 2.4 | V |

**NOTES:**
1. Unless otherwise specified, the following conditions apply: Unit is in "sample" mode. $V_S$ = ±15 V, $T_j$ = 25 °C, –11.5V ≤ $V_{IN}$ ≤ 11.5 V, $C_H$ = 0.01 µF, and $R_L$ = 2 kΩ. Logic reference voltage = 0 V and logic voltage = 2.5 V.
2. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5 mV step with a 5 V logic swing and a 0.01 F hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
3. Leakage current is measured at a junction temperature of 25 °C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25 °C value for each 11 °C increase in chip temperature. Leakage is guaranteed over full input signal range.
4. These parameters guaranteed over a supply voltage range of ±5 V to ±18 V.

## TYPICAL PERFORMANCE CHARACTERISTICS

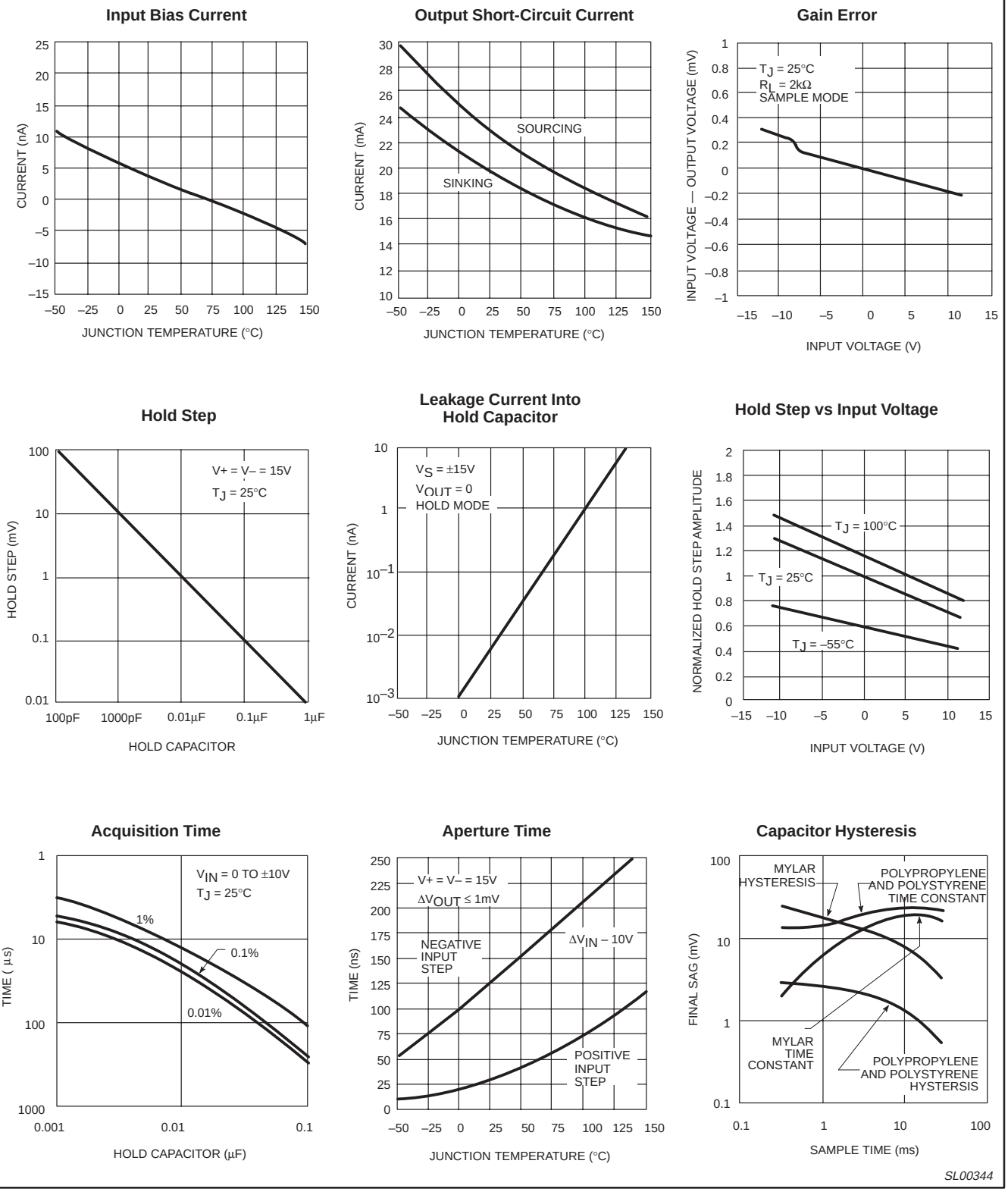



**Figure 3. Typical Performance Characteristics**

## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

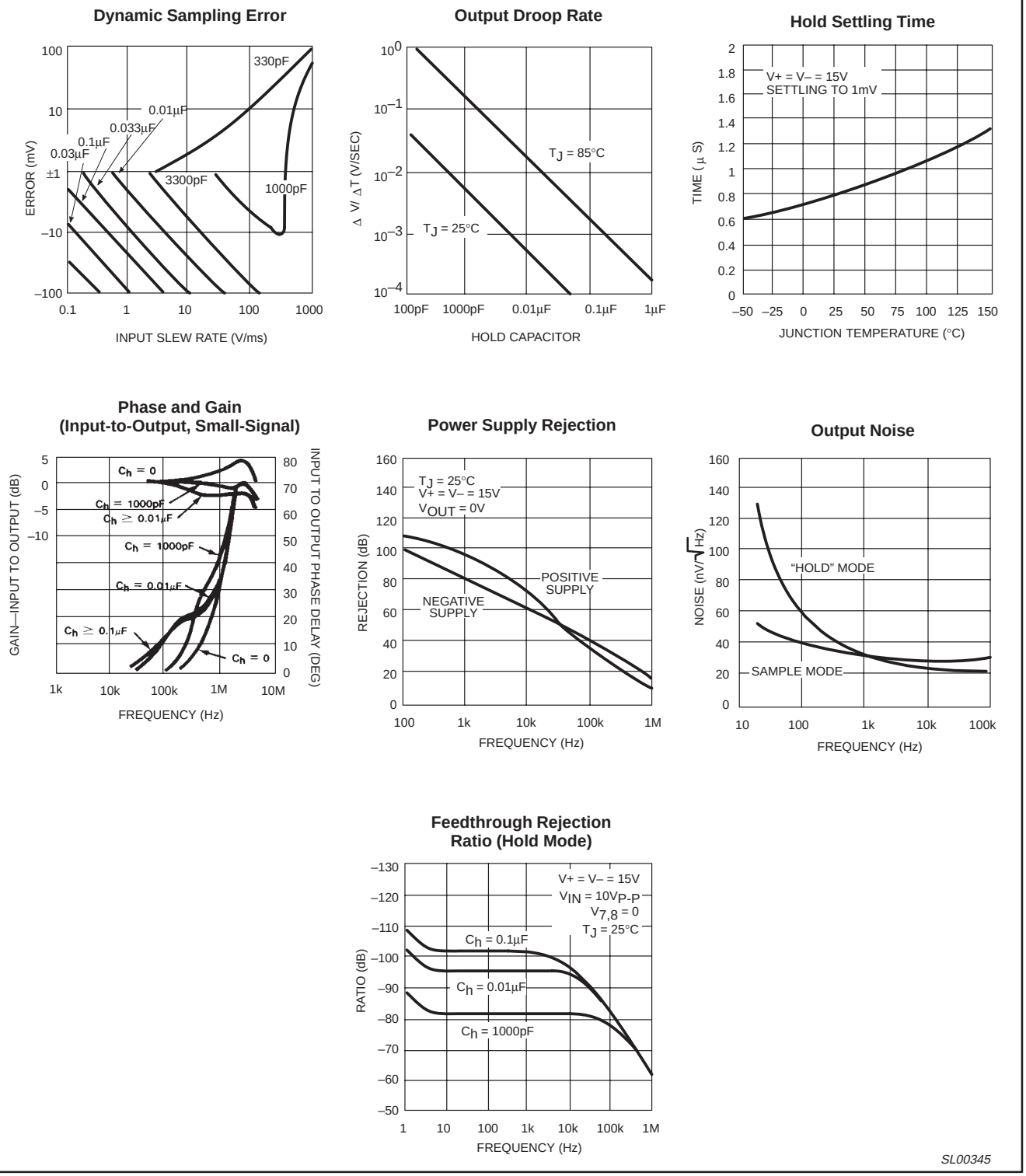



**Figure 4. Typical Performance Characteristics (cont.)**

## SAMPLE-AND-HOLD

For many years designers have used the sample-and-hold (or track-and-hold) to operate on analog information in a time frame which is expedient.

By sampling a segment of the information and holding it until the proper timing for converting to some form of control signal or readout, the designer maintains certain freedom in performing predetermined manipulative functions. Therefore, the sample-and-hold can be defined as a "selective analog memory cell".

The memory is volatile and will also decay with time.

When using the sample-and-hold method for evaluating signal information, the designer is given the added feature of eliminating outside noise elements. With the analog-to-digital converter products available today, the "DC memory" of the sample-and-hold can be easily converted to digital format and further incorporated into microprocessor-based systems.

Parametric evaluation of the sample-and-hold will be discussed in the following paragraphs.

## DEFINITION OF TERMS

**Acquisition Time —** The time required to acquire a new analog input voltage with an output step of 10 V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

**Aperture Delay Time —** The time elapsed from the hold command to the opening of the switch.

**Aperture Jitter —** Also called "aperture uncertainty time", it is the time variation or uncertainty with which the switch opens, or the time variation in aperture delay.

**Aperture Time —** The delay required between "HOLD" command and an input analog transition, so that the transition does not affect the held output.

**Bandwidth —** The frequency at which the gain is down 3 dB from its DC value. It's measured in sample (track) mode with a small-signal sine wave that doesn't exceed the slew rate limit.

**Dynamic Sampling Error —** The error introduced into the hold output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

**Effective Aperture Delay —** The time difference between the hold command and the time at which the input signal is at the held voltage.

**Figure of Merit —** The ratio of the available charging current during sample mode to the leakage current during hold mode.

**Gain Error —** The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

**Hold Mode Droop —** The output voltage change per unit of time while in hold. Commonly specified in V/s, μV/μs or other convenient units.

**Hold Mode Feedthrough —** The percentage of an input sinusoidal signal that is measured at the output of a sample-hold when it's in hold mode.

**Hold Settling Time —** The time required for the output to settle within 1mV of final value after the "HOLD" logic command.

**Hold Step —** The voltage step at the output of the sample-and-hold when switching from sample mode to hold mode with a steady (DC) analog input voltage. Logic swing is 5 V.

**Sample-to-Hold Offset Error —** The difference in output voltage between the time the switch starts to open, and the time when the output has settled completely. It is caused by charge being transferred to the hold capacitor switch as it opens.

**Slew Rate —** The fastest rate at which the sample-and-hold output can change (specified in V/μs).

**Threshold Level —** That level which causes the switch control to change state.

## BASIC BLOCK DIAGRAM

The basic circuit concept of the sample-and-hold circuit incorporates the use of two (2) operational amplifiers and a switch control mechanism (which determines sample, hold or track conditions).

The block diagram of the NE5537 is a closed loop, non-inverting unity gain sample-and-hold system. The input buffer amplifier supplies the current necessary to charge the hold capacitor, while the output buffer amplifier closes the loop so that the output voltage is identical to the input voltage (with consideration for input offset voltage, offset current, and temperature variations which are common to all sample-and-hold circuits, be they monolithic, hybrid or modular).

When the sampling switch is open (in the hold mode), the clamping diodes close the loop around the input amplifier to keep it from being overdriven into saturation.

The switch control is driven by external logic levels via a timing sequence remote from the sample-and-hold device (See Figure 5). The switch control has a floating reference (Pin 7), referred to as the logic reference which makes the sample-and-hold device compatible to several types of external logic signals (TTL, PMOS, and CMOS). The switching device operates at a threshold level of 1.4 V.

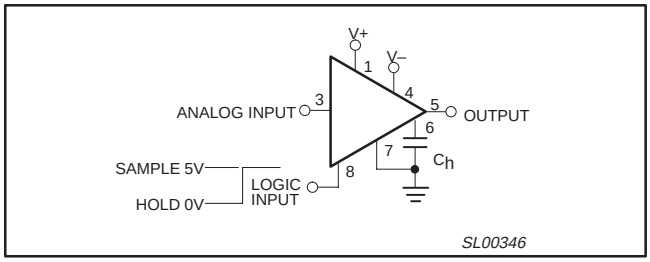



**Figure 5. Typical Connection**

The switch mechanism is on (sampling an information stream) when the logic level is high (Pin 8 is 1.4 V higher than Pin 7) and presents a load of 5 μA to the input logic signal. The analog sampled signal is amplified, stored (in the external holding capacitor), and buffered. At the end of the sampling period, the internal switch mechanism turns

off (switch opens) and the "stored analog memory" information on the external capacitor (Pin 6) is loaded down by an operational amplifier connected in the unity gain non-inverting configuration. This input impedance of this amplifier is effectively:

$$R = R_{IN} (A_{OL}) / (1 + 1/A)$$

where

R = Effective input impedance
$R_{IN}$ = Open-loop input impedance
$A_{OL}$ = Open-loop gain
A = AC loop gain

Therefore, the higher the open-loop gain of the second operational amplifier, the larger the effective loading on the capacitor. The larger the load, the lower the "leakage" current and the better the droop characteristics.

In actuality, the amplifiers are designed with special leakage current cancellation circuits along with FET input devices. The leakage current cancellation circuits give better high temperature operation. (Remember that the FET amplifiers double in required bias current for every 10 degree increase in junction temperature.)

Sampling time for the NE5537 is less than 10µs (measured to 0.1% of input signal). Leakage current is 6 pA at a rate output load of 2 kΩ.

## BASIC APPLICATIONS

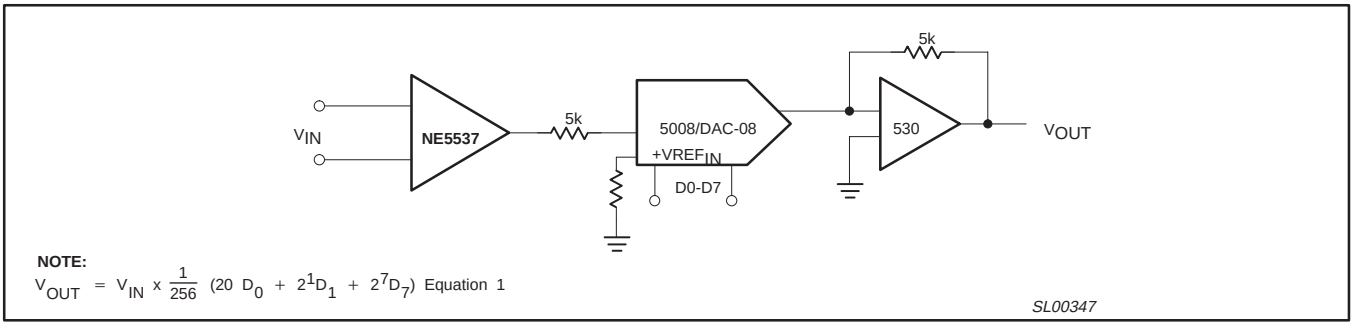
### Multiplying DAC

As depicted in the block diagram of Figure 6, the sample-and-hold circuit is used to supply a "variable" reference to the digital-to-analog converter. As the input reference varies, the output will change in accordance with Equation 1, shown in Figure 6.

Varying the input signal reference level can aid the system in performing both compression and expansion operations. The multiplying DACs used are the Philips Semiconductors NE/SE5008; however, if the rate of change of the reference variation is kept slow enough, a microprocessor-compatible DAC can be incorporated, such as the NE5018 or the NE5020.

## DATA ACQUISITION SYSTEMS

As mentioned earlier, the designer may wish to operate on several different segments of an "analog" signal; however, he is limited by the fact that only one analog-to-digital converter channel is available to him. Figure 7 shows the means by which a multiplexing system may be accomplished.




**NOTE:**

$$V_{OUT} = V_{IN} \times \frac{1}{256} (20\ D_0 + 2^1 D_1 + 2^7 D_7) \quad \text{Equation 1}$$

**Figure 6. Multiplying DAC Application**

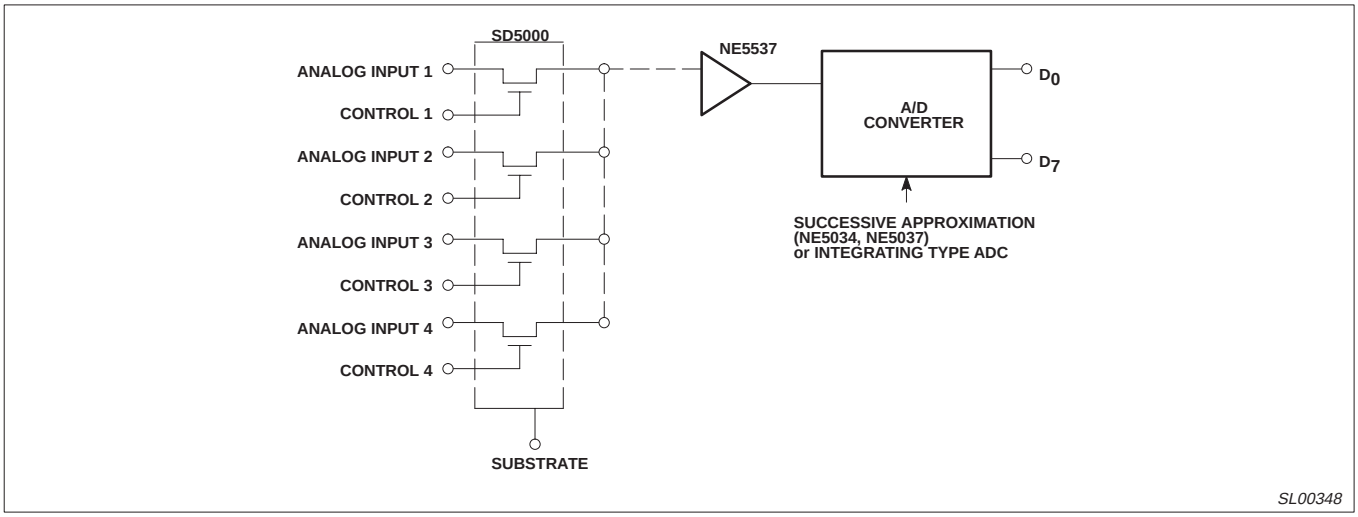



**Figure 7. Analog Data Multiplexing**

## APPLICATION HINTS

### Hold Capacitor

A significant source of error in an accurate sample-and-hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may “sag back” up to 0.2% after a quick change in voltage. A long “soak” time is required before the circuit can be put back in the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and teflon. Other types such as mica and polycarbonate are not nearly as good. Ceramic is unusable with >1% hysteresis. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85 °C to 100 °C. The hysteresis relaxation time constant in polystyrene, for instance, is 10–50 ms. If A-to-D conversion can be made within 1 ms, hysteresis error will be reduced by a factor of ten.

## DC ZEROING

DC zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1 kΩ potentiometer which has one end tied to V+ and the other end tied through a resistor to ground. The resistor should be selected to give 0.6mA through the 1 kΩ potentiometer.

### Sampling Dynamic Signals

Sampling errors due to moving (changing) input signals are of significant concern to designers employing sample-and-hold circuits. There exist finite phase delays through the sample-and-hold circuit causing an input-output phase of differential for moving signals. In addition, the series protection resistor (300 Ω to Pin 6 of the NE5537) will add an RC time constant, over and above the slew rate limitation of the input buffer/current drive amplifier. This means that at the moment the “HOLD” command arrives, the hold capacitor voltage may be somewhat different from the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 $V_{P-P}$ at 10 kHz. Maximum dV/dt is 0.6 V/μs. With no analog phase delay and 100 ns logic delay, one could expect up to (0.1 μs) (0.6 V/μs) = 60 mV error if the “HOLD” signal arrived near maximum dV/dt of the input. A positive-going input would give a ±60 mV error. Now assume a 1 MHz (3 dB) bandwidth for the overall analog loop. This generates a phase delay of 160 ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16 μs) (0.6 V/μs) = –96 mV (analog) for a total of –36 mV. To add to the confusion, analog delay is proportional to hold capacitor value, while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

A curve labeled “Aperture Time” has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the “HOLD” command. This curve is based on a 1 mV error fed into the output.

A second curve, “Hold Settling Time,” indicates the time required for the output to settle to 1 mV after the “HOLD” command.

### Digital Feedthrough

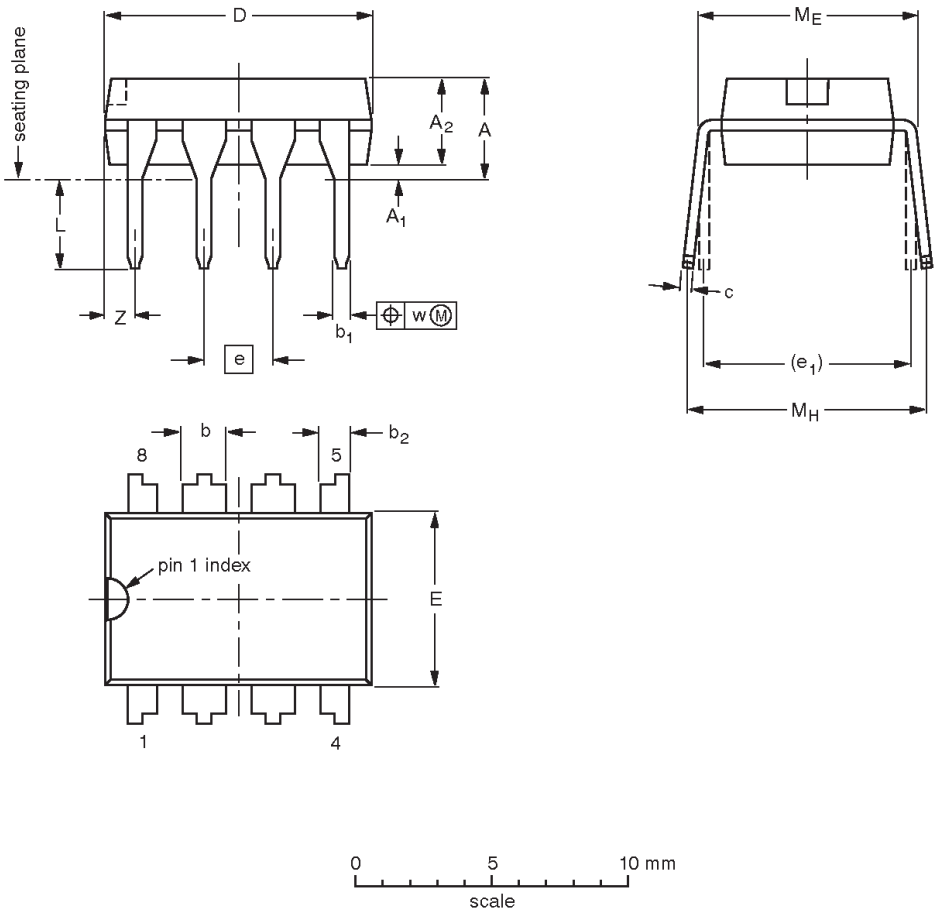
Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5 V will also help.

Logic signals also couple to the hold capacitor. This hold capacitor should be guarded by a PC card trace connected to the sample-and-hold output. This will also minimize board leakage.

## SPECIAL NOTES

1. Not all definitions herein defined are measured parametrically for the NE5537, but are legitimate terms used in sample-and-hold systems.
2. Reference should be made to *Design Engineering*, Volumes 23 (Nov. 8, 1978), 25 (Dec. 6, 1978) and 26 (Dec. 20, 1978) for articles written by Eugene Zuch of Datel Systems, Inc., for a further discussion of sample-and-hold circuits.
3. Reference also made to National Semiconductor Corporation’s *Special Functions Data Book* (1976).

**DIP8: plastic dual in-line package; 8 leads (300 mil)** **SOT97-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

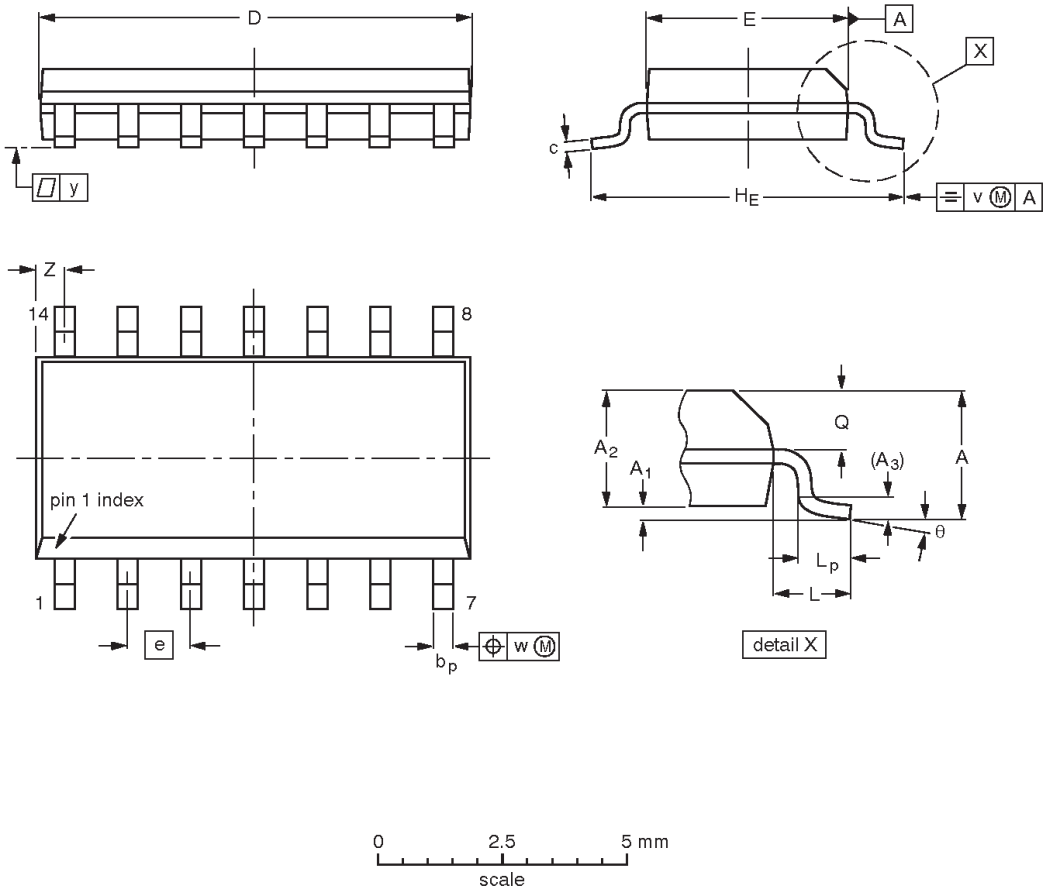
| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | $b_2$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.2 | 0.51 | 3.2 | 1.73<br>1.14 | 0.53<br>0.38 | 1.07<br>0.89 | 0.36<br>0.23 | 9.8<br>9.2 | 6.48<br>6.20 | 2.54 | 7.62 | 3.60<br>3.05 | 8.25<br>7.80 | 10.0<br>8.3 | 0.254 | 1.15 |
| inches | 0.17 | 0.020 | 0.13 | 0.068<br>0.045 | 0.021<br>0.015 | 0.042<br>0.035 | 0.014<br>0.009 | 0.39<br>0.36 | 0.26<br>0.24 | 0.10 | 0.30 | 0.14<br>0.12 | 0.32<br>0.31 | 0.39<br>0.33 | 0.01 | 0.045 |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT97-1 | 050G01 | MO-001 | SC-504-8 | | | ~~95-02-04~~<br>99-12-27 |

**SO14: plastic small outline package; 14 leads; body width 3.9 mm** **SOT108-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 8.75<br>8.55 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.35<br>0.34 | 0.16<br>0.15 | 0.050 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT108-1 | 076E06 | MS-012 | | | | ~~97-05-22~~<br>99-12-27 |

**NOTES**

## Data sheet status

| Data sheet status[1] | Product status[2] | Definitions |
|---|---|---|
| Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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**Limiting values definition —** Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 12-01

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