

QUARTZ CRYSTAL OSCILLATOR

■ GENERAL DESCRIPTION

The NJU6339 series is a C-MOS quartz crystal oscillator which consists of an oscillation amplifier, 3-stage divider and 3-state output buffer.

This series are classed into three groups A to D, H to L and Q to T according to their oscillation frequency range mentioned in the line-up table.

The oscillation amplifier incorporates feed-back resistance and oscillation capacitors(Cg, Cd), therefore, it requires no external component except quartz crystal.

The 3-stage divider generates f_0 , $f_0/2$, $f_0/4$ and $f_0/8$ and only one frequency selected by internal circuits is output.

The 3-state output buffer is C-MOS compatible and capable of 10 LSTTL driving.

The difference between NJU6339 and NJU6332 series is pin configuration only.

■ FEATURES

- Operating Voltage. -- 4.0~6.0V
- Maximum Oscillation Frequency (See Line-Up Table)
- Low Operating Current
- High Fan-out -- LSTTL 10
- 3-state Output Buffer
- Selected Frequency Output (mask option)
Only one frequency out of f_0 , $f_0/2$, $f_0/4$ and $f_0/8$ output
- Oscillation Capacitors Cg and Cd on-chip
- Oscillation and/or Output Stand-by Function
- Package Outline -- CHIP / EMP 8
- C-MOS Technology

■ LINE-UP TABLE

Type No.	Recommended Osc. Freq.	Output Freq.	Cg, Cd
NJU6339A 6339B 6339C 6339D	From 20 to 35MHz	f_0 $f_0/2$ $f_0/4$ $f_0/8$	28pF
NJU6339H 6339J 6339K 6339L	From 30 to 50MHz	f_0 $f_0/2$ $f_0/4$ $f_0/8$	20pF
NJU6339Q 6339R 6339S 6339T	From 45 to 75MHz	f_0 $f_0/2$ $f_0/4$ $f_0/8$	17pF

■ PACKAGE OUTLINE

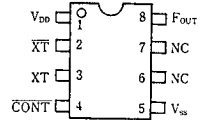
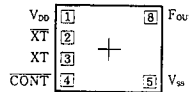


NJU6339XC



NJU6339XE

■ PIN CONFIGURATION/PAD LOCATION



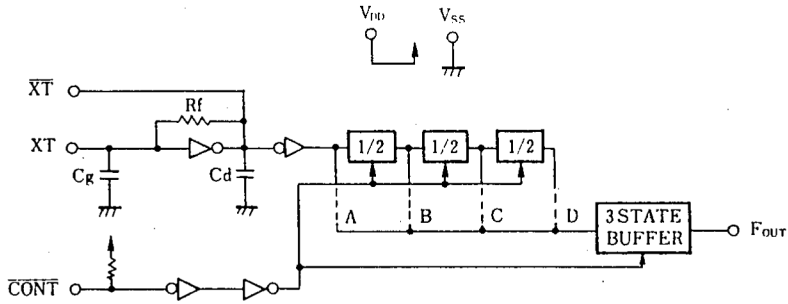
■ COORDINATES

Unit: μm

No.	PAD	X	Y
1	V_{DD}	-408	248
2	XT	-408	81
3	XT	-408	-86
4	CONT	-408	-248
5	V_{SS}	464	-248
8	FOUT	464	248

Chip Size : 1.29 X 0.8mm
 Chip Center : X=0 μm , Y=0 μm
 Chip Thickness : 400 $\mu\text{m} \pm 30\mu\text{m}$
 (Note) No. 6 and 7 terminals are only for package type information. There are no PAD on the chip.

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

NO.	SYMBOL	F U N C T I O N						
1	V_{DD}	+ 5V						
2	\overline{XT}	Quartz Crystal Connecting Terminals						
3	XT							
4	\overline{CONT}	3-State Output Control and Divider Reset						
		<table border="1"> <thead> <tr> <th>CONT</th> <th>F_{OUT}</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>Output either one frequency from f_o, $f_o/2$, $f_o/4$ and $f_o/8$</td> </tr> <tr> <td>L</td> <td>Output High Impedance and Divider Reset</td> </tr> </tbody> </table>	CONT	F_{OUT}	H	Output either one frequency from f_o , $f_o/2$, $f_o/4$ and $f_o/8$	L	Output High Impedance and Divider Reset
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5	V_{SS}	GND						
8	F_{OUT}	Output either one frequency from f_o , $f_o/2$, $f_o/4$ and $f_o/8$						

(Note) Reference the Line-Up Table

■ ABSOLUTE MAXIMUM RATINGS

 ($T_a=25^\circ\text{C}$)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.5 ~ +7.0	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_O	-0.5 ~ $V_{DD}+0.5$	V
Input Current	I_{IN}	± 10	mA
Output Current	I_O	± 25	mA
Power Dissipation	P_D	200 (EMP)	mW
Operating Temperature Range	T_{OPR}	-40 ~ + 85	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 ~ +125	$^\circ\text{C}$

 (Note) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the circuit.

■ ELECTRICAL CHARACTERISTICS

 ($T_a=25^{\circ}\text{C}$, $V_{DD}=5\text{V}$)

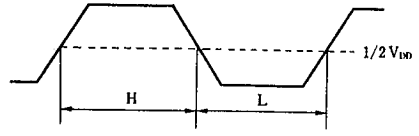
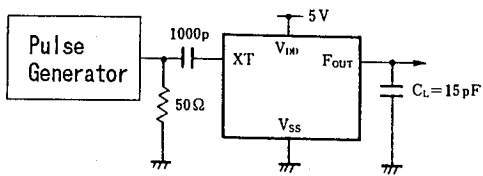
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V_{DD}		4		6	V
Operating Current	I_{DD1}	A,B,C,D, $f_{osc}=24\text{MHz}$, No Load			15	mA
	I_{DD2}	H,J,K,L, $f_{osc}=48\text{MHz}$, No Load			20	
	I_{DD3}	Q,R,S,T, $f_{osc}=48\text{MHz}$, No Load			25	
Stand-by Current	I_{st}	$\overline{\text{CONT}}, X_T=V_{SS}$, No Load (Note)			1	μA
Input Voltage	V_{IH}		3.5		5.0	V
	V_{IL}		0		1.5	
Output Current	I_{OH}	$V_{DD}=5\text{V}$, $V_{OH}=4.5\text{V}$	4			mA
	I_{OL}	$V_{DD}=5\text{V}$, $V_{OL}=0.5\text{V}$	4			
Input Current	I_{IN}	$\overline{\text{CONT}}$ Terminal, $\overline{\text{CONT}}=V_{SS}$	125	250	500	μA
3-St Off-leakage Current	I_{OZ}	$\overline{\text{CONT}}=V_{SS}$, $F_{OUT}=V_{SS}$ and V_{DD}			± 0.1	μA
Internal Capacitor	C_g, C_d	A,B,C,D Version, $f_{osc}=24\text{MHz}$		28		pF
		H,J,K,L Version, $f_{osc}=48\text{MHz}$		20		
		Q,R,S,T Version, $f_{osc}=48\text{MHz}$		17		
Maximum Oscillation Frequency	f_{MAX}	A,B,C,D Version	35			MHz
		H,J,K,L Version	50			
		Q,R,S,T Version	75			
Output Signal Symmetry	SYM	$C_L=15\text{pF}$, $R_L=390\Omega$, at $1/2V_{DD}$	45	50	55	%
Output Signal Rise Time	t_r	$C_L=15\text{pF}$, 10~90%			6	ns
Output Signal Fall Time	t_f	$C_L=15\text{pF}$, 90~10%			4	ns

 Note) Excluding input current on $\overline{\text{CONT}}$ terminal.

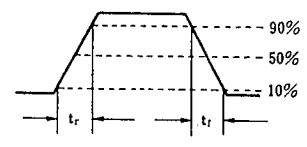
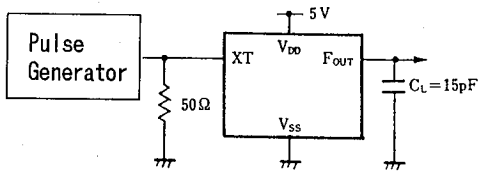
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■ MEASUREMENT CIRCUITS

(1) Output Signal Symmetry ($C_L=15\text{pF}$)



(2) Output Signal Rise / Fall Time ($C_L=15\text{pF}$)



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NJU6339 Series

MEMO

[CAUTION]

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