

MNCLC522A-X REV 0A0

Original Creation Date: 06/24/98
Last Update Date: 04/05/99
Last Major Revision Date: 1/27/99

WIDEBAND VARIABLE-GAIN AMPLIFIER

General Description

The CLC522 variable gain amplifier (VGA) is a dc-coupled, two-quadrant multiplier with differential voltage inputs and a single-ended voltage output. Two input buffers and an output operational amplifier are integrated with the multiplier core to make the CLC522 a complete VGA system that does not require external buffering.

The CLC522 provides the flexibility of externally setting the maximum gain with only two external resistors. Greater than 40dB gain control is easily achieved through a single high impedance voltage input. The CLC522 provides a linear (in Volts per Volt) relationship between the amplifier's gain and the gain-control input voltage.

The CLC522's maximum gain may be set anywhere over a nominal range of 2V/V to 100V/V. The gain control input then provides attenuation from the maximum setting. For example, set for a maximum gain of 100V/V, the CLC522 will provide a 100V/V to 1V/V gain control range by sweeping the gain control input voltage from +1 to -0.98V.

Set a maximum gain of 10V/V, the CLC522 provides a 165MHz signal channel bandwidth and a 165MHz gain control bandwidth. Gain non-linearity over a 40dB gain range is 0.5% and gain accuracy at $A_{vmax} = 10V/V$ is typically $\pm 0.3\%$.

Industry Part Number

CLC522A

NS Part Numbers

CLC522AE-QML**
CLC522AJ-QML*

Prime Die

UB1579B

Controlling Document

5962-9451701MCA*, M2A**

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp Description

Temp (°C)

1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 330MHz signal bandwidth: $A_{vmax} = 2$
- 165MHz gain-control bandwidth
- 0.3 degrees to 60MHz linear phase deviation
- 0.04% (-68dB) signal-channel non-linearity
- >40dB gain-adjustment range
- Differential or single-end voltage inputs
- Single-ended voltage output

Applications

- Variable attenuators
- Pulse amplitude equalizers
- HF modulators
- Automatic gain control & leveling loops
- Video production switching
- Differential line receivers
- Voltage controlled filters

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage (Vs)	±7V dc
Output Current (Iout)	95mA
Common Mode Input Voltage (Vcm)	Vs
Differential Input Voltage (Vid)	±10V
Power Dissipation (Pd) (Note 2)	810mW
Lead Temperature (soldering, 10 seconds)	+300 C
Junction Temperature (Tj)	+175 C
Storage Temperature Range	-65 C to +150 C
Thermal Resistance	
Junction-to-Ambient (ThetaJA)	
Ceramic DIP (Still Air)	84 C/W
(500 LFPM)	44 C/W
LCC (Still Air)	85 C/W
(500 LFPM)	61 C/W
Junction-to-Case (ThetaJC)	
Ceramic DIP	13 C/W
LCC	21 C/W
Package Weight (typical)	
Ceramic DIP	TBD
LCC	470 mg
ESD Tolerance (Note 3)	
ESD Rating	500 V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{dmax} = (T_{jmax} - TA) / \Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100pF discharged through 1.5K Ohms.

Recommended Operating Conditions

Supply Voltage (Vs)	$\pm 5\text{V}$ dc
Gain Range (Av)	$\pm 2\text{V/V}$ to $\pm 100\text{V/V}$
Ambient Operating Temperature Range (Ta)	-55 C to +125 C

Electrical Characteristics

DC PARAMETERS: Static and DC Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $V_s = \pm 5V$ dc, gain setting voltage (V_g) = +1.1V, $A_v = 10V/V$, load resistance (R_l) = 100 Ohms, feedback resistance (R_f) = 1 KOhms, and gain setting resistance (R_g) = 182 Ohms $-55\text{ C} \leq T_a \leq +125\text{ C}$ (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Iib	Input Bias Current				-21	+21	uA	1, 2
					-45	+45	uA	3
Iio	Input Offset Current				-2.0	+2.0	uA	1, 2
					-4.0	+4.0	uA	3
Voo	Output Offset Voltage	$R_s = 50\text{ Ohms}$			-85	+85	mV	1
					-120	+120	mV	2
					-90	+90	mV	3
Dib	Average Input Bias Current Drift		1		-125	+125	nA/C	2
			1		-275	+275	nA/C	3
DVoo	Average Output Offset Voltage Drift	$T_a = +125\text{ C}, -55\text{ C}$	1		-300	+300	uV/C	2
			1		-400	+400	uV/C	3
DIio	Average Input Offset Current Drift	$T_a = +125\text{ C}, -55\text{ C}$	1		-20	+20	nA/C	2
			1		-40	+40	nA/C	3
Icc	Supply Current	No Load			-61	+61	mA	1, 2
					-63	+63	mA	3
PSS	Power Supply Sensitivity	$+V_s = +4.5V$ to $+5.0V$, $-V_s = -4.5V$ to $-5.0V$, output referred				-28	dB	1, 2, 3
Ig	Gain Control Input Bias Current				-38	+38	uA	1, 2
					-82	+82	uA	3
DIg	Gain Control Input Bias Current Temperature Coefficient	$T_a = +125\text{ C}, -55\text{ C}$	1			+210	nA/C	2
			1			+600	nA/C	3
CMRR	Common Mode Rejection Ratio	$V_{cm} = \pm 1V$, input referenced	1		59		dB	1, 2, 3
SGNL	Integral Signal Nonlinearity	$V_{out} = 4\text{ Vpp}$				0.1	%	1, 2, 3
GCNL	Gain Control Nonlinearity	$V_{out} = 4\text{ Vpp}$				2.0	%	1
						2.5	%	2
						3.0	%	3
GACCU	Gain Error	$A_v = 10V/V$			-0.5	+0.5	dB	1, 2
					-1.0	+0.5	dB	3

Electrical Characteristics

AC PARAMETERS: Frequency Response Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC:

AC: $V_s = \pm 5V$ dc, gain setting voltage (V_g) = +1.1V, $A_v = 10V/V$, load resistance (R_L) = 100 Ohms, feedback resistance (R_f) = 1 KOhms, and gain setting resistance (R_g) = 182 Ohms $-55^\circ C \leq T_a \leq +125^\circ C$ (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
SSBW	Small Signal Bandwidth	$V_{out} < 0.5 V_{pp}$			120		MHz	4
			2		110		MHz	5
			2		120		MHz	6
LSBW	Large Signal Bandwidth	$V_{out} < 5.0 V_{pp}$	1		100		MHz	4, 6
			1		90		MHz	5
GFPH	Gain Flatness Peaking High	0.1MHz to 200MHz, $V_{out} \leq 0.5 V_{pp}$				0.5	dB	4
			2			0.7	dB	5, 6
GFRH	Gain Flatness Rolloff High	0.1MHz to 60MHz, $V_{out} \leq 0.5 V_{pp}$				1.0	dB	4
			2			1.0	dB	5
			2			1.3	dB	6
GFPL	Gain Flatness Peaking Low	0.1MHz to 30MHz, $V_{out} \leq 0.5 V_{pp}$				0.1	dB	4
			2			0.1	dB	5, 6
GFRL	Gain Flatness Rolloff Low	0.1MHz to 30MHz, $V_{out} \leq 0.5 V_{pp}$				0.25	dB	4
			2			0.25	dB	5
			2			0.4	dB	6
LPD	Linear Phase Deviation	0.1MHz to 60MHz, $V_{out} \leq 0.5 V_{pp}$	1			1.0	Deg	4
			1			1.2	Deg	5, 6
GCBW	Gain Control Bandwidth	$V_{out}, V_g \leq 0.5 V_{pp}$	1		120		MHz	4, 6
			1		110		MHz	5
FDTH	Feedthrough	30MHz, $V_g < -1.1V$			-37		dB	4
			2		-37		dB	5, 6

Electrical Characteristics

AC PARAMETERS: Distortion and Noise Tests.

(The following conditions apply to all the following parameters, unless otherwise specified.)

AC: $V_s = \pm 5V$ dc, gain setting voltage (V_g) = +1.1V, $A_v = 10V/V$, load resistance (R_l) = 100 Ohms, feedback resistance (R_f) = 1 KOhms, and gain setting resistance (R_g) = 182 Ohms -55 C $\leq T_a \leq +125$ C (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
HD2	2nd Harmonic Distortion	2 VPP at 20MHz				-44	dBc	4
			2			-44	dBc	5, 6
HD3	3rd Harmonic Distortion	2 VPP at 20MHz				-58	dBc	4
			2			-54	dBc	5
			2			-58	dBc	6
OSNF	Output Noise Floor	1MHz to 200MHz	1			-130	dBm 1Hz	4, 6
			1			-129	dBm 1Hz	5
OSN	Output Spot Noise	1 MHz to 200MHz	1			62	nV/Sq RtHz	4, 6
			1			68	nV/Sq RtHz	5

AC PARAMETERS: Timing Domain Response Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)

AC: $V_s = \pm 5V$ dc, gain setting voltage (V_g) = +1.1V, $A_v = 10V/V$, load resistance (R_l) = 100 Ohms, feedback resistance (R_f) = 1 KOhms, and gain setting resistance (R_g) = 182 Ohms -55 C $\leq T_a \leq +125$ C (Note 3)

SR	Slew Rate	Measured $\pm 1V$ with 4V Step, $A_v = +10$	1		1400		V/uS	9, 10, 11
Trs	Rise and Fall Time	0.5V Step	1			2.9	nS	9, 11
			1			3.2	nS	10
Trl	Rise and Fall Time	5.0V Step	1			5.0	nS	9, 10, 11
TS	Settling Time	2V step at 0.1% of the final value	1			18	nS	9, 10, 11
OS	Overshoot	0.5V Step	1			15	%	9, 10, 11

Electrical Characteristics

AC/DC PARAMETERS: Miscellaneous Performance Tests.

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $V_s = \pm 5V$ dc, gain setting voltage (V_g) = +1.1V, $A_v = 10V/V$, load resistance (R_l) = 100 Ohms, feedback resistance (R_f) = 1 KOhms, and gain setting resistance (R_g) = 182 Ohms -55 C $\leq T_a \leq$ +125 C (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
It	Buffer Tail Current		1		1.37		mA	1, 3
			1		1.15		mA	2
CMIR	Vin Common Mode Voltage Range		1		-1.2	+1.2	V	1, 2
			1		-1.4	+1.4	V	3
Vgosh	Vg Input Voltage	$A_v = 10V/V$	1		930	1050	mV	1, 2, 3
Vgosl	Vg Input Voltage	$A_v = 0V/V$	1		-1055	-895	mV	1, 2, 3
Vout	Output Voltage Range	No Load	1		-3.7	+3.7	V	1, 2
			1		-3.5	+3.5	V	3
Iout	Output Current		1		-47	+47	mA	1, 2
			1		-25	+25	mA	3
Rin	Vin Signal Input Resistance		1		650		KOhms	4, 5
			1		175		KOhms	6
Cin	Vin Signal Input Capacitance		1			2	pF	4, 5, 6
Ring	Vg Control Input resistance		1		38		KOhms	4, 5
			1		15		KOhms	6
Cing	Vg Control Input Capacitance		1			2.0	pF	4, 5, 6
Ro	Output Impedance	DC	1			0.2	Ohms	4, 5
			1			0.6	Ohms	6

Note 1: If not tested, shall be guaranteed to the limits specified in table I

Note 2: Group A testing only.

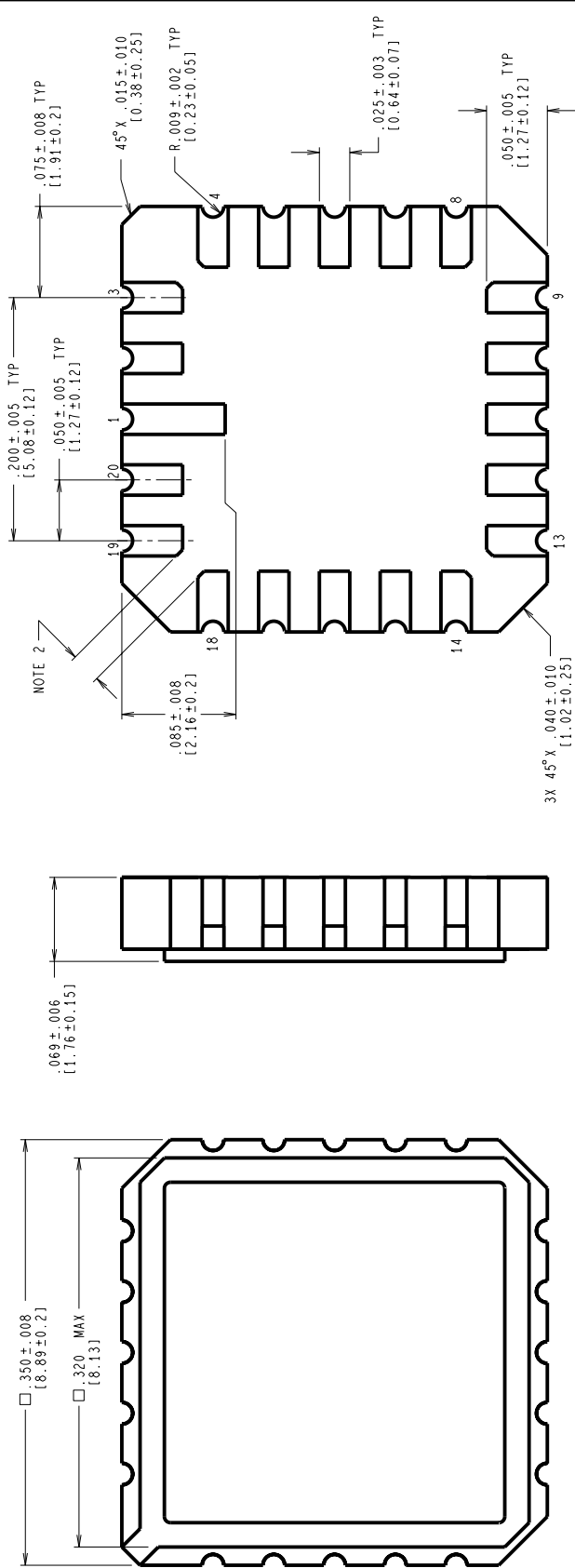
Note 3: The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
07079HRA2	CERDIP (J), 14 LEAD (B/I CKT)
07092HRA2	(new)
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000423A	CERDIP (J), 14 LEAD (PINOUT)
P000449A	(new)

See attached graphics following this page.

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
E	REVISE AND REDRAW	10005	02/10/94 DEG/



CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

a. 50 MICRONS/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICRONS/1.27-8.89 MICROMETERS NICKEL.

b. SOLDER DIP.
SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

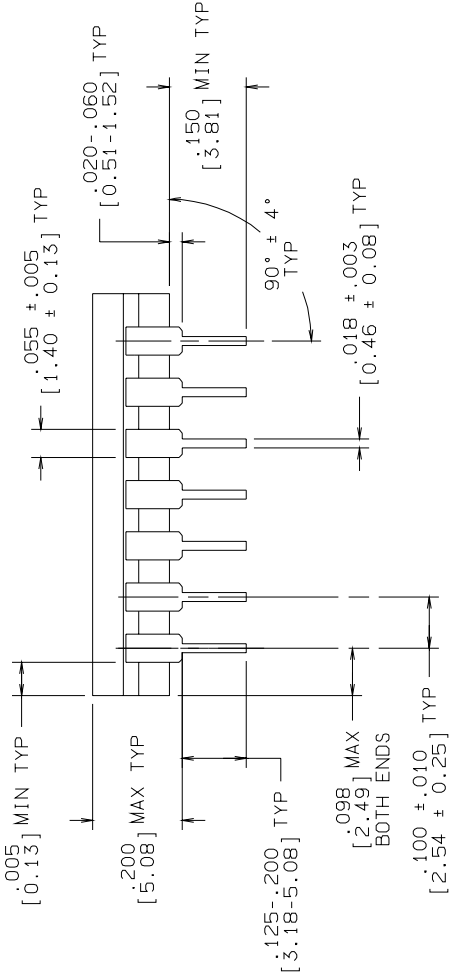
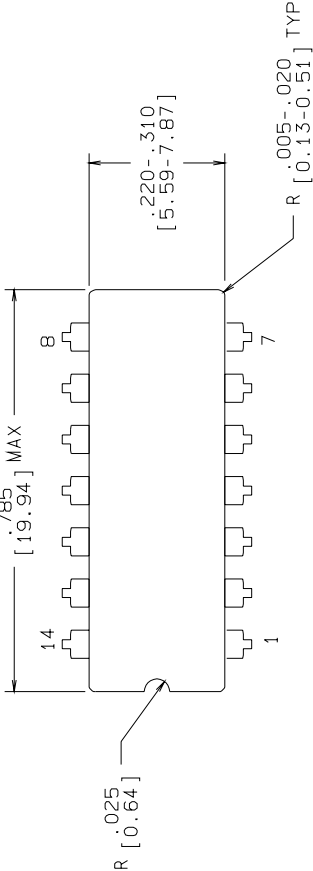
2. CORNER PADS MAY HAVE A 45° X $.020$ IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015 IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO CONFIGURATION CONTROL

APPROVALS		DATE	NATIONAL SEMICONDUCTOR CORPORATION	
DESIGN	Design Grady	02/10/94	2000 Semiconductor Drive, Santa Clara, CA 95052-8090	
ESTG. CHK.			LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL	
ENGR. CHK.				
APPROVAL				
PROJECTION		SCALE		REV
1 INCH = 1 INCH		N/A C		E
		DO NOT SCALE DRAWING		SHEET 1 of 1

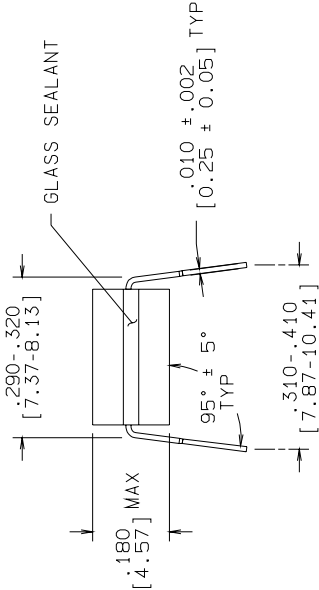
R E V I S I O N S				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/



CONTROLLING DIMENSION: INCH

NOTES: UNLESS OTHERWISE SPECIFIED

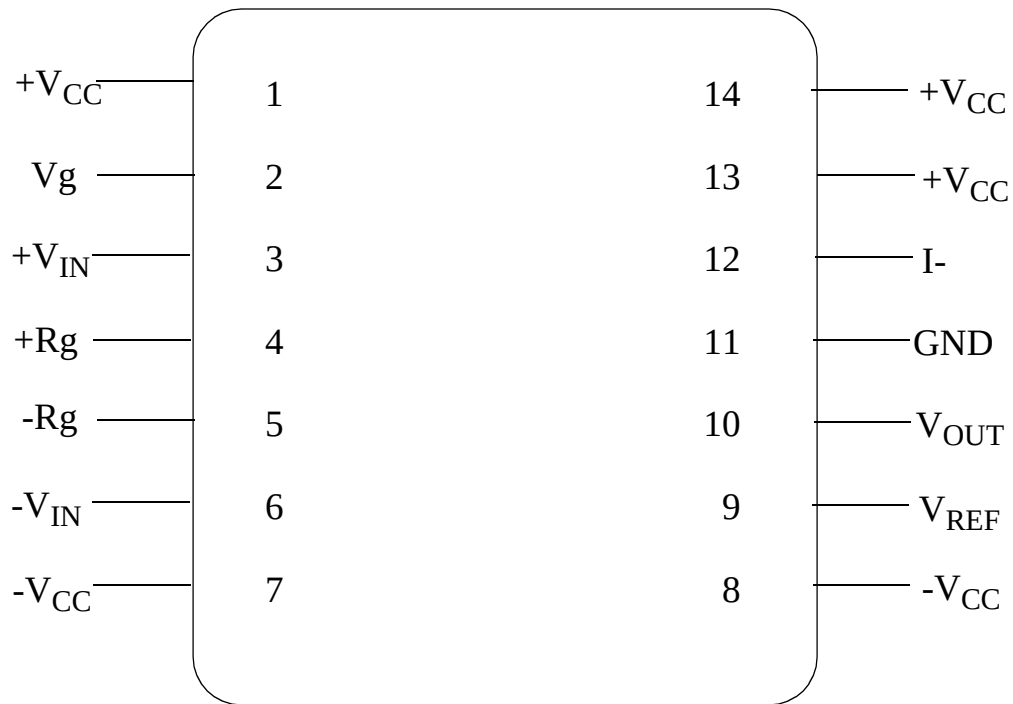
1. LEAD FINISH TO BE 200 MICROMETERS / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.



MIL/AERO MIL-M-38510
CONFIGURATION CONTROL CONFIGURATION CONTROL

APPROVALS	DATE	NATIONAL SEMICONDUCTOR CORPORATION		
DRAWN LEQUANG	09/15/93	2900 Semiconductor Drive, Santa Clara, CA 95052-8090		
DFTG. CHK.				
ENGR. CHK.				
APPROVAL				
PROJECTION		SCALE	SIZE	DRAWING NUMBER
		N/A	B	MKT-J14A
		DO NOT SCALE	DRAWING	SHEET 1 OF 1
				REV H

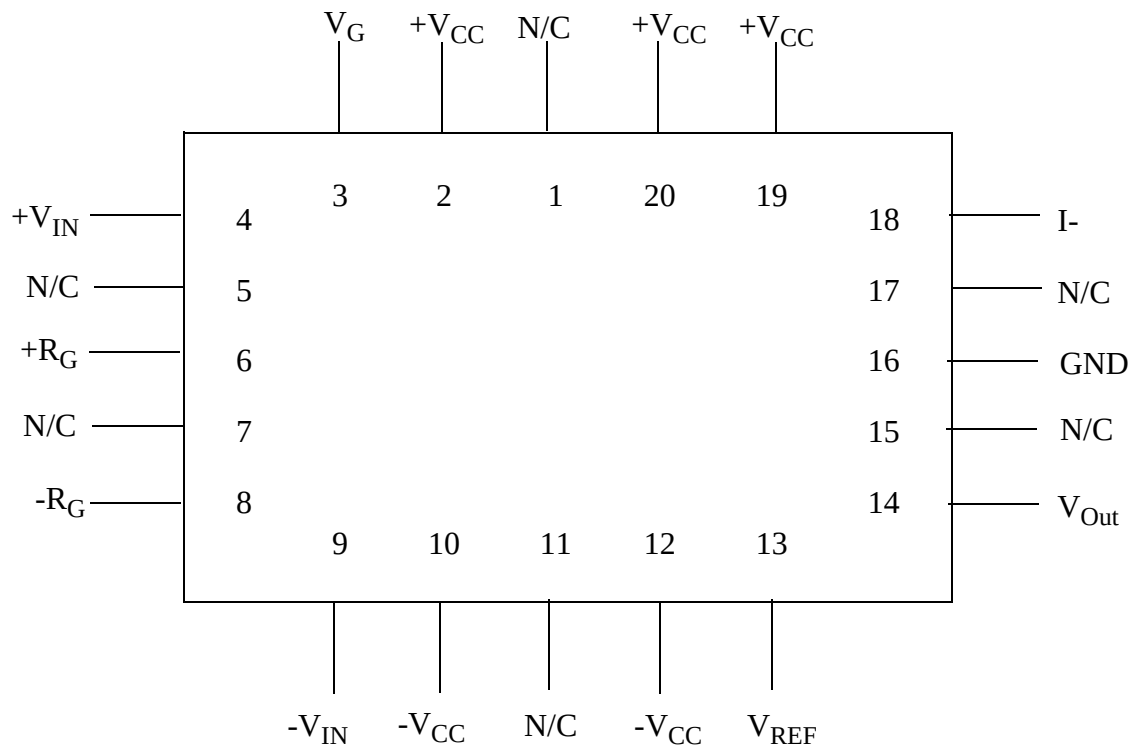
CERDIP (J) ,
14 LEAD,



CLC522J
 14 - LEAD DIP
 CONNECTION DIAGRAM
 TOP VIEW
 P000423A



National Semiconductor™
 MIL/AEROSPACE OPERATIONS
 2900 SEMICONDUCTOR DRIVE
 SANTA CLARA, CA 95050



CLC522E
 20 - LEAD LCC
 CONNECTION DIAGRAM
 TOP VIEW
 P000449A



National Semiconductor™
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 2900 SEMICONDUCTOR DRIVE
 SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003338	04/05/99	Shaw Mead	Initial MDS Release