National Semiconductor

MILITARY DATA SHEET

MNDS3884A-X REV 0B0

Original Creation Date: 10/18/94
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Last Major Revision Date: 10/18/94

BTL HANDSHAKE TRANSCEIVER

General Description

The DS3884A is one in a series of transceivers designed specifically for the implementation of high performance Futurebus+ and proprietary bus interfaces. The DS3884A is a BTL 6-bit Handshake Transceiver designed to conform to IEEE 1194.1 (Backplane Transceiver Logic-BTL) as specified in the IEEE 896.2 Futurebus+ specification. Utilization of the DS3884A simplifies the implementation of all handshake signals which require Wired-OR glitch filtering. Three of the six bits have an additional parallel Wired-OR filtered receive output giving a total of nine receiver outputs.

In Wired-OR applications, the glitch generated as drivers are released from the bus, is dependent upon the backplane and parasitic wiring components causing the characteristics of the glitch to vary in pulse width and amplitude. To accommodate this variation the DS3884A features two pins defined as PS1 and PS2 which allow selection of Four Different Filter Settings to optimize glitch filtering for a given situation. The REXT pin is issued in conjunction with the filtering circuitry and requires a 15K Ohm resistor to ground.

The DS3884A driver output configuration is an NPN open collector which allows Wired-OR connection on the bus. Each driver output incorporates a Schottky diode in series with its collector to isolate the transistor output capacitance from the bus thus reducing the bus loading in the inactive state. The driver also has high sink current capability.

Backplane Transceiver Logic (BTL) is a signaling standard that was invented and first introduced by National Semiconductor, then developed by the IEEE to enhance the performance of backplane buses. BTL compatible transceivers feature low output capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. The BTL standard eliminates settling time delays that severely limit TTL bus performance, and thus provide significantly higher bus transfer rates. The backplane bus is intended to be operated with termination resistors (selected to match the bus impedance) connected to 2.1V at both ends. The low voltage is typically 1V at 25 C, 125 C and 1.1V at -55 C.

Separate ground pins are provided for each BTL output to minimize induced ground noise during simultaneous switching.

The device's unique drive circuitry meets a maximum slew rate of 0.5V/ns which allows controlled rise and fall times to reduce noise coupling to adjacent lines.

The transceiver's high impedance control and driver inputs are fully TTL compatible.

The receiver is a high speed comparator that utilizes a bandgap reference for precision threshold control allowing maximum noise immunity to the BTL 1V signaling level.

Separate QVcc and QGND pins are provided to minimize the effects of high current switching noise. Output pins FR1-FR3 are the filtered outputs and R1-R6 are unfiltered outputs. All receiver outputs are fully TTL compatible.

The DS3884A supports live insertion as defined for Futurebus+ through the LI (Live Insertion) pin. To implement live insertion the LI pin should be connected to the live insertion power connector. If this function is not supported the LI pin must be tied to the Vcc pin. The DS3884A also provides power up/down glitch free protection during power sequencing.

The DS3884A has two types of power connections in addition to the LI pin. They are the Logic Vcc (Vcc) and the Quiet Vcc (QVcc). There are two Vcc pins on the DS3884A that provide the supply voltage for the logic and control circuitry. Multiple connections are provided to reduce the effects of package inductance and thereby minimize switching noise. As these pins are common to the Vcc bus internal to the device, a voltage difference should never exist between these pins and the voltage difference between Vcc and QVcc should never exceed $\pm$0.5V because of ESD circuitry. Additionally, the ESD circuitry between the Vcc pins and all other pins except for BTL I/Os and LI pins requires that any voltage on these pins should not exceed the voltage on Vcc + 0.5V.

There are three different types of ground pins on the DS3884A. They are the Logic ground (GND), BTL grounds (B1GND-B6GND) and the Bandgap reference ground (QGND). All of these ground reference pins are isolated within the chip to minimize the effects of high current switching transients. For optimum performance the QGND should be returned to the connector through a quiet channel that does not carry transient switching current. The GND and B1GND-B6GND should be connected to the nearest backplane ground pin with the shortest possible path.

General Description (Continued)

Since many different grounding schemes could be implemented and ESD circuitry exist on the DS3884A, it is important to note that any voltage difference between ground pins, QGND, GND or B1GND-B6GND should not exceed ±0.5V including power up/down sequencing.

Additional transceivers included in the Futurebus+ family are; the DS3886A, BTL 9-bit Latching Data Transceiver, the DS3885 BTL Arbitration transceiver with arbitration competition logic for the AB<7:0>/$\overline{ABP}$ signal lines, and the featuring edge triggered latches in the driver which may be bypassed during a fall-through mode and a transparent latch in the receiver.

The DS3875 Arbitration Controller included in the Futurebus+ family supports all the required and optional modes for Futurebus+ arbitration protocol. It is designed to be used in conjuction with the DS3884A and DS3885 transceivers.

The DS3805 (LIFE) is a high performance Futurebus+ Protocol Controller. The DS3805 will handle all handshaking signals between the Futurebus+ and the local bus interface.

All of the transceivers are offered in 48-pin CERPAC package.

Industry Part Number

DS3884A

NS Part Numbers

DS3884AW/883

Prime Die

T3884

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Fast propagation delay
- 6-bit BTL transceiver
- Selective receiver glitch filtering (FR1-FR3)
- Supports live insertion
- Glitch free power-up/down protection
- Typically less than 5pF bus-port capacitance
- Low Bus-port voltage swing (typically 1V) at 80mA
- TTL compatible driver and control inputs
- Separate TTL I/O
- Open collector bus-port outputs allow wired-OR connection
- Controlled rise and fall time to reduce noise coupling to adjacent lines
- Built in bandgap reference with separate QVcc and QGND pins for precise receiver thresholds
- Individual bus-port ground pins
- Product offered in CERPAC package style

(Absolute Maximum Ratings)

Supply Voltage	6.5V
Control Input Voltage	6.5V
Driver Input and Receiver Output	5.5V
Receiver Input Current	±15mA
Bus Termination Voltage	2.4V
Power Dissipation at 25 C (CERPAC) Derate at 11.5 mW/ C above 25 C	1.7W
Storage Temperature Range	-65 C to +150 C
Lead Temperature (Soldering, 4 seconds)	260 C

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Recommended Operating Conditions

	Min.	Max.
Supply Voltage, Vcc	4.5V	5.5V
Bus Termination Voltage (Vt)	2.06V	2.14V
Operating Free Air Temperature	-55 C	125 C

Electrical Characteristics

DC: DRIVER AND CONTROL INPUT: (Dn, $D\bar{E}$, PS1 & PS2)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 5V ±10%

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vih	Logical 1 Input Voltage	Vcc = 4.5			2		V	1, 2, 3
Vil	Logical 0 Input Voltage	Vcc = 4.5				0.8	V	1, 2, 3
Ii	Input Leakage Current	Vcc = 5.5V, Vin = 5.5V				100	uA	1, 2, 3
Iih	Input High Current	Vcc = 5.5V, Vin = 2.4V <Dn Inputs>				40	uA	1, 2, 3
		Vcc = 5.5V, Vin = 2.4V <DE/PS Inputs>				40	uA	1, 2, 3
Iil	Input LOW Current	Vcc = 5.5V, Vin = 0.5V			-100	100	uA	1, 2, 3
Vcl	Input Clamp Diode Voltage	Vcc = 4.5V, Ii = -12mA				-1.2	V	1, 2, 3

DC PARAMETERS: DRIVER OUTPUT/RECEIVER INPUT: (Bn)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 5V ±10%

VOLB	Output Low Bus Voltage	Vcc = 4.5V, 5.5V, Io=80mA, Dn=2.4V, DE=0V	1		0.75	1.1	V	1, 2
			1		0.75	1.15	V	3
IOLBZ	Output Low Bus Current	Vcc=5.5V, Dn=0.5V, DE=2.1V, Bn=0.75V			-100	100	uA	1, 2, 3
IOHBZ	Output High Bus Current	Vcc=5.5V, Dn=0.5V, DE=2.1V, Bn=2.1V			-100	100	uA	1, 2, 3
VTH	Receiver Input Threshold	Vcc = 4.5V, 5.5V, DE = 2.4V			1.47	1.62	V	1, 2, 3
Vclp	Positive Clamp Diode Voltage	Vcc = 5.5 or 0V, Ibn = 1mA			2.4	4.5	V	1, 2, 3
		Vcc = 5.5 or 0V, Ibn = 10mA			2.9	5.0	V	1, 2, 3
IOLB	Output Low Bus Current	Vcc=5.5V, Dn=0.5V, DE=0V, Bn=0.75V			-100	100	uA	1, 2, 3
IOHB	Output High Bus Current	Vcc=5.5V, Dn=0.5V, DE=0V, Bn=2.1V			-100	100	uA	1, 2, 3
Vcln	Negative Clamp Diode Voltage	Vcc = 5.5V, Iclamp = -12mA				-1.2	V	1, 2, 3

Electrical Characteristics

DC PARAMETERS: RECEIVER OUTPUT: (FRn and Rn)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 5V ±10%

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Voh	Logical "1" Output Voltage	Vcc=4.5V, Ioh = -2mA, Bn=1.1V, DE=2.4V			2.4		V	1, 2, 3
Vol	Logical "0" Output Voltage	Vcc=4.5V, DE=2.4V, Bn=2.1V, Iol=8mA				0.4	V	1, 2, 3
		Vcc=4.5V, DE=2.4V, Bn=2.1V, Iol=24mA				0.5	V	1, 2, 3
Ios	Output Short Circuit Current	Vcc = 5.5V, 4.5V, BN = 1.1V, DE = 2.4V	2		-100	-40	mA	1, 2, 3

DC PARAMETERS: SUPPLY CURRENT

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 5V ±10%

Icc	Supply Current Includes Vcc, QVcc and Ll	Vcc = 5.5V, DE = 0.5V, All Dn = 2.4V				80	mA	1, 2, 3
		Vcc = 5.5V, DE = 2.4V, All Bn = 2.1V				80	mA	1, 2, 3
Ili	Live Insertion Current	Vcc = 5.5V, DE = 0.5V, All Dn = 2.4V				5	mA	1, 2, 3
		Vcc = 5.5V, DE = 2.4V, All Bn = 2.1V				3	mA	1, 2, 3

AC PARAMETERS: DRIVER

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 5V ±10%

tPHLD	DN to BN Propagation Delay	DE = 0V, RL = 12.5, CL = 30pF			1	7		9, 10, 11
tPLHD	DN to BN Propagation Delay	DE = 0V, CL = 30pF, RL = 12.5			1	7		9, 10, 11
tPHLDE	DE to BN: Enable Time	Dn = 3V, RL = 12.5, CL = 30pF			1	9	nS	9, 10, 11
tPLHDE	DE to BN: Disable Time	Dn = 3V, RL = 12.5, CL = 30pF			1	9	nS	9, 10, 11
tr	Transition Time 20% to 80%				1	3.5	nS	9, 10, 11
tf	Transition Time 80% to 20%				1	4.5	nS	9, 10, 11
SR	Slew Rate	From 1.3 to 1.8V			1		nS	9, 10, 11
tskewD	Skew		3			5	nS	9, 10, 11

Electrical Characteristics

AC PARAMETERS: RECEIVER

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 5V ±10%

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tPHLR	Bn to Rn Proparation Delay	De = 3V, RL = 1k, CL = 50pF			1	8	nS	9, 10, 11
tPLHR	Bn to Rn Proparation Delay	De = 3V, CL = 50pF			1	8	nS	9, 10, 11
tskewR	Skew between receivers in the same package		3			5	nS	9, 10, 11

AC PARAMETERS: FILTERED RECEIVER

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 5V ±10%

tPHLFR	BN to FRn Propagation Delay	DE = PS1 = PS2 = 3V, REXT = 15K Ohm, CL = 50pF, RL = 1K			22	66	nS	9, 10, 11
		DE=3V, PS1=PS2=0V, REXT=15K Ohm, CL=50pF, RL=1K			6	21	nS	9, 10, 11
		DE=PS1=3V, PS2=0V, REXT=15K Ohm, CL=50pF, RL=1K			16	41	nS	9, 10, 11
		DE = PS2 = 3V, PS1 = 0V, REXT = 15K Ohm, CL = 50pF, RL = 1K			11	31	nS	9, 10, 11
tPLHFR	BN to FRn Propagation Delay	DE = 3V, REXT = 15K	4		2	8	nS	9, 10, 11
tGR	Glitch Rejection	DE = PS1 = PS2 = 3V, REXT = 15K			20	65	nS	9, 10, 11
		DE = 3V, PS1 = PS2 = 0V, REXT = 15K			5	20	nS	9, 10, 11
		DE = PS1 = 3V, PS2 = 0V, REXT = 15K			14	40	nS	9, 10, 11
		DE = PS2 = 3V, PS1 = 0V, REXT = 15K			10	30	nS	9, 10, 11

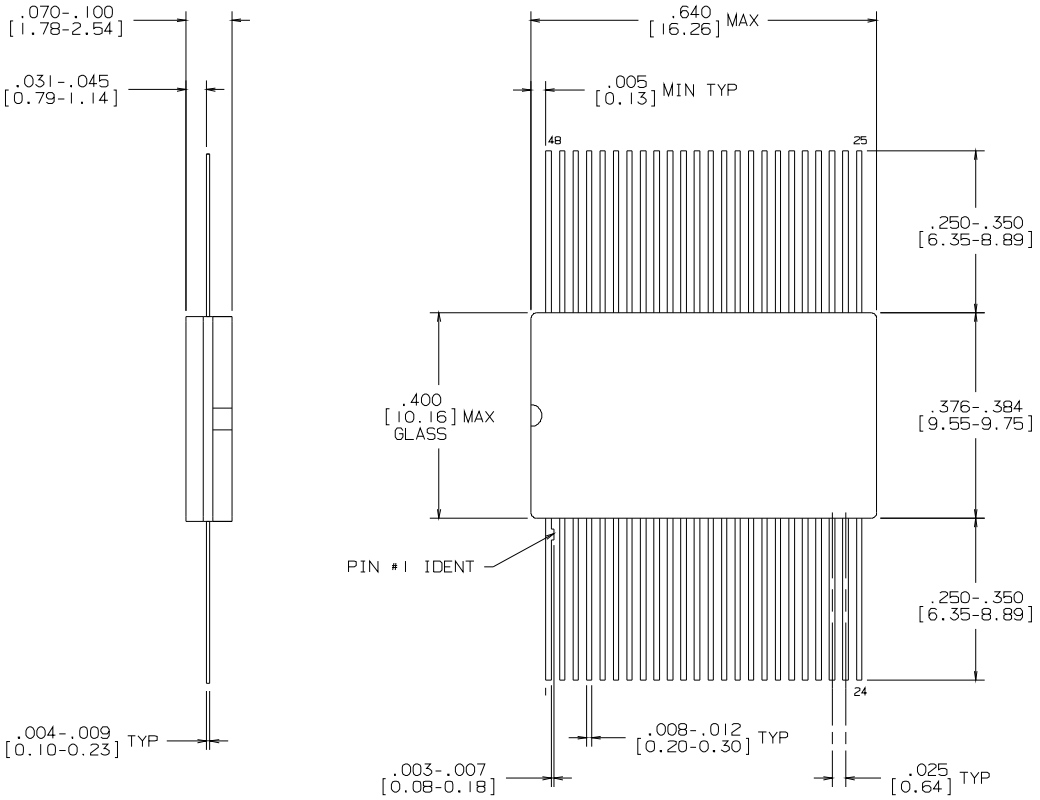
Note 1: Referenced to appropriate signal ground. Do not exceed maximum power dissipation of pkg.
Note 2: Only one output at a time should be shorted, and duration of the short should not exceed one second.
Note 3: tskew is an absolute value defined as differences seen in propagation delays between drivers/receivers in the same pkg.
Note 4: Filtered receiver tPLH is independent of filter setting.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
6298HRC1	CERPAC, 48 LEAD, .025 LEAD PITCH (B/I CKT)
WA48ARB	CERPAC, 48 LEAD, .025 LEAD PITCH (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	09283	08/11/92	MS/SL
B	DIM .003-.007[0.08-0.18] WAS .006-.010[0.15-0.25]; DIM .031-.045[0.79-1.14] WAS .040-.054[1.02-1.37]	09489	01/25/93	MS/



MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH:
   200 MICROINCHES/ 5.08 MICROMETERS MINIMUM SOLDER
   MEASURED AT THE CREST OF THE MAJOR FLATS.
2. THE LEAD FINISH, NICKEL UNDERPLATE, AND BASIS METAL
   SHALL CONFORM TO THE REQUIREMENTS OF MIL-M-38510.
3. REFERENCE JEDEC METRIC BALLOT JC-11.10-92-75, ITEM 10-320,
   VARIATION AA, DATED JULY 9,1992.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN MARTA SUCHY	08/11/92
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

NATIONAL SEMICONDUCTOR CORPORATION
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CERPAC, 48 LEAD,
.025 LEAD PITCH

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-WA48A	B

DO NOT SCALE DRAWING | SHEET 1 OF 1