National Semiconductor

MILITARY DATA SHEET

MNLF11333-X REV 0A0

Original Creation Date: 08/30/95
Last Update Date: 09/18/95
Last Major Revision Date: 08/30/95

QUAD SPST JFET ANALOG SWITCH 2 NORMALLY CLOSED SWITCHES AND 2 NORMALLY OPEN SWITCHES WITH DISABLE

General Description

This device is a monolithic combination of bipolar and JFET technology producing the industry's first one chip quad JFET switch. A unique circuit technique is employed to maintain a constant resistance over the analog voltage range of ±10V. The input is designed to operate from minimum TTL levels, and switch operation also ensures a break-before-make action.

This device operates from ±15V supplies and swings a ±10V analog signal. The JFET switches are designed for applications where a dc to medium frequency analog signal needs to be controlled.

Industry Part Number

LF11333

NS Part Numbers

LF11333D/883

Prime Die

LM3653

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Analog signals are not loaded
- Constant "ON" resistance for signals up to ±10V and 100KHz
- Pin compatible with CMOS switches with the advantage of blow out free handling
- Small signal analog signals to 50MHz
- Break-before-make action tOFF < tON
- High open switch isolation at 1.0MHz -50dB
- Low leakage in "OFF" state
- TTL, DTL, RTL compatibility
- Single disable pin opens all switches.

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage (Vcc-Vee)	36V
Reference Voltage	Vee ≤ Vr ≤ Vcc
Logic Input Voltage	Vr-4.0V ≤Vin≤ Vr+6.0V
Analog Voltage	Vee≤Va≤Vcc+6V; Va≤Vee+36V
Analog Current	|Ia|<20mA
Power Dissipation (Note 2)	900mW
Operating Temperature Range	-55 C to +125 C
Storage Temperature	-65 C to +150 C
Maximum Junction Temperature	150 C
Soldering Information (10 seconds)	300 C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: For operating at high temperature the molded DIP products must be derated based on a +100 C maximum junction temperature and a thermal resistance of +150 C/W, devices in the cavity DIP are based on a +150 C maximum junction temperature and are derated at ±100 C/W.

Electrical Characteristics

DC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = +15V, Vee = -15V, Vref = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Icc	Positive Supply Current	Vcc = 18V, Vee = -18V				15	mA	1
		Vs = -10V				6	mA	1
						9	mA	2, 3
Iee	Negative Supply Current	Vcc = 18V, Vee = -18V			-15		mA	1
		Vs = -10V			-5		mA	1
					-7.5		mA	2, 3
Iref	Reference Supply Current				-4		mA	1
					-6		mA	2, 3
Iih	Logical "1" input Current	Vin = 6V				10	uA	1
						25	uA	2, 3
Iil	Logical "0" input Current	Vin = -4V			-0.1	+0.1	uA	1
					-1	1	uA	2, 3
Ron	"ON" Resistance (Drain to Source)	Va = 0, Id = 1mA	2			200	Ohm	1
			2			300	Ohm	2, 3
Ron(match)	"ON" Resistance (Matching)		2		-20	20	Ohm	1
Is(OFF)	"OFF" State Source Current	Vd = -20V			-5	5	nA	1
					-100	100	nA	2, 3
Id(OFF)	"OFF" State Drain Current	Vs = 20V			-5	5	nA	1
					-100	100	nA	2, 3
Is(ON) & Id(ON)	"ON" State Leakage Current	Vcc = 5V, Vee = -25V, Vs = 0V			-5	5	nA	1
					-100	100	nA	2, 3
Idis	Disable Current		1		-1		mA	1
			1		-1.5		mA	2, 3
Va	Analog Voltage Range		1		$\pm$10		V	1, 2, 3
Vih	Logical "1" input Voltage		1		2		V	1, 2, 3
Vil	Logical "0" input Voltage		1			.8	V	1, 2, 3

Electrical Characteristics

AC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = +15V, Vee = -15V, Vref = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tON	"ON" Delay Time	Vs = ±10V	3			1500	nS	9
tOFF	"OFF" Delay Time	Vs = ±10V	3			500	nS	9

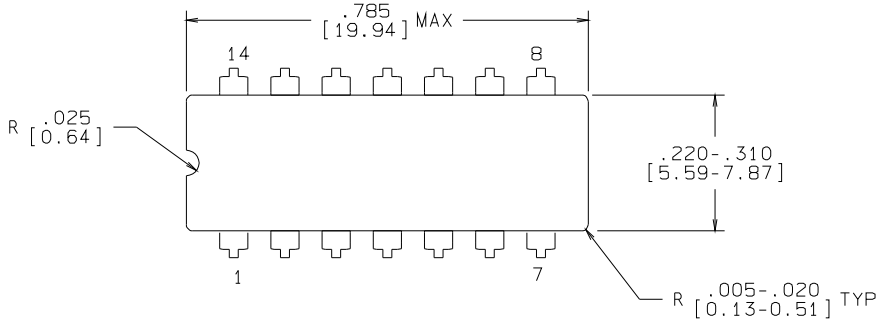
Note 1: Parameter tested go-no-go only.
Note 2: Datalog conversions are: 20 Ohms = .02K, 200 Ohms = .2K, 300 Ohms = .3K
Note 3: Bench tested, test box No. 70256641.

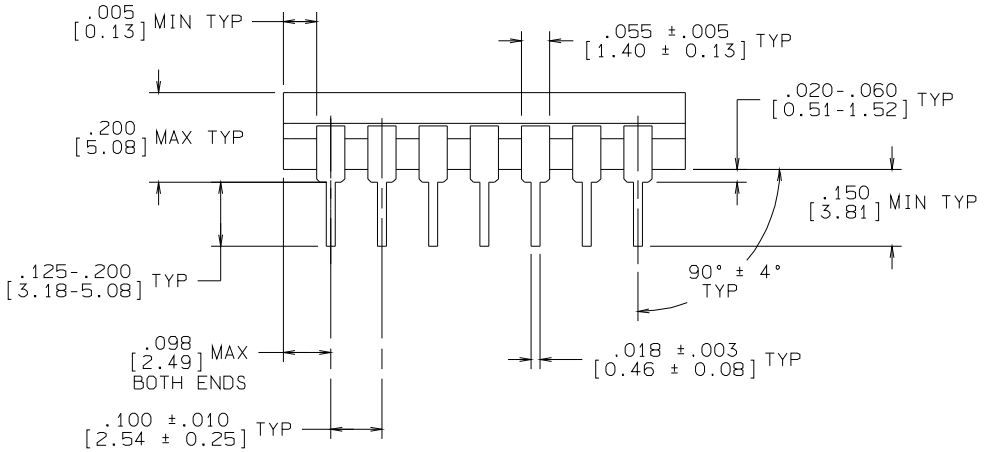
Graphics and Diagrams

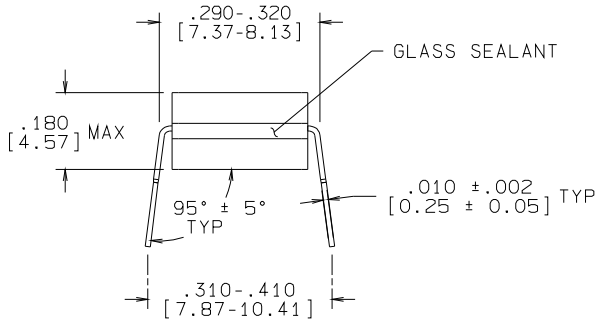
GRAPHICS#	DESCRIPTION
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/







CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
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CERDIP (J), 14 LEAD,

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1