National Semiconductor

MICROCIRCUIT DATA SHEET

MJLM139-X REV 0C0

Original Creation Date: 05/18/95
Last Update Date: 12/20/96
Last Major Revision Date: 05/18/95

LOW POWER LOW OFFSET VOLTAGE QUAD COMPARATORS

General Description

The LM139 series consists of four independent precision voltage comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possile and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application area include limit comparators, simple analog to digital converters, pulse, squarewave and the time delay generators, wide range VCO, MOS clock timers, multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic-where the low power drain of the LM339 is a distinct advantage over standard comparators.

Industry Part Number

LM139

Prime Die

LM139

Controlling Document

38510/11201, AMEND. 3 REV A

NS Part Numbers

JL139BCA
JL139BDA
JL139SCA
JL139SDA

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

MJLM139-X - Wide supply voltage range 5Vdc to 36Vdc
or ±2.5V to ±18Vdc
- Very low supply current drain (0.8mA Typ)
independent of supply voltage
- Low input biasing current 25nA
- Low input offset current ±5nA
and offset voltage ±3mV
- Differential input voltage range
equal to the power supply voltage
- Low output saturation voltage 250mV at 4mA
- Output voltage compatible with TTL,
DTL, ECL, MOS and CMOS logic systems

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage	
V+	36Vdc or ±18Vdc
Differential Input Voltage (Note 5)	36V
Output Voltage	36V
Input Voltage	-0.3V to +36V
Input Current (Note 6)	
(Vin < -0.3Vdc)	50mA
Power Dissipation (Note 2, 3)	
CERDIP	400mW at TA = 125 C
CERPACK	350mW at TA = 125 C
Maximum Junction Temperature	175 C
Output Short-Circuit to GND (Note 4)	Continuous
Storage Temperature Range	-65 C to +150 C
Operating Temperature Range	-55 C to +125 C
Lead Temperature	
(Soldering, 10 seconds)	260 C
Thermal Resistance	
ThetaJA	
CERDIP (Still Air)	103 C/W
(500LF/Min Air flow)	65 C/W
CERPACK (Still Air	183 C/W
(500LF/Min Air flow)	120 C/W
ThetaJC	
CERDIP	23 C/W
CERPACK	23 C/W
ESD Tolerance (Note 7)	600V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax -TA/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: The low bias dissipation and the ON-OFF characteristic of the outputs keeps the chip dissipation very small (Pd ≤ 100mW), provided the output transistors are allowed to saturate.

Note 4: Short circuits from the output to V+ can cause excessive heating and eventual destruction. When considering short to ground, the maximum output current is approximately 20mA independent of the magnitude of V+.

Note 5: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide the proper output state. The low input voltage state must not be less than -3.0Vdc (or 0.3Vdc below the magnitude of the negative power supply, if used) (at 25 C).

(Continued)

Note 6: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3Vdc.

Note 7: Human body model, 1.5K Ohms in series with 100pF.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: -Vcc = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	+Vcc = 30V, -Vcc = 0V, Vo = 15V			-5	5	mV	1
					-7	7	mV	2, 3
		+Vcc = 2V, -Vcc = -28V, Vo = -13V			-5	5	mV	1
					-7	7	mV	2, 3
		+Vcc = 5V, -Vcc = 0V, Vo = 1.4V			-5	5	mV	1
					-7	7	mV	2, 3
		+Vcc = 2V, -Vcc = -3V, Vo = -1.6V			-5	5	mV	1
					-7	7	mV	2, 3
Iio	Input Offset Current	+Vcc = 30V, -Vcc = 0V, Rs = 20K Ohms, Vo = 15V	1		-25	25	nA	1, 2
			1		-75	75	nA	3
		+Vcc = 2V, -Vcc = -28V, Rs = 20K Ohms, Vo = -13V	1		-25	25	nA	1, 2
			1		-75	75	nA	3
		+Vcc = 5V, -Vcc = 0V, Rs = 20K Ohms, Vo = 1.4V	1		-25	25	nA	1, 2
			1		-75	75	nA	3
		+Vcc = 2V, -Vcc = -3V, Rs = 20K Ohms, Vo = -1.6V	1		-25	25	nA	1, 2
			1		-75	75	nA	3
+Iib	Input Bias Current	+Vcc = 30V, -Vcc = 0V, Rs = 20K Ohms, Vo = 15V	1		-100	+0.1	nA	1, 2
			1		-200	+0.1	nA	3
		+Vcc = 2V, -Vcc = -28V, Rs = 20K Ohms, Vo = -13V	1		-100	+0.1	nA	1, 2
			1		-200	+0.1	nA	3
		+Vcc = 5V, -Vcc = 0V, Rs = 20K Ohms, Vo = 1.4V	1		-100	+0.1	nA	1, 2
			1		-200	+0.1	nA	3
		+Vcc = 2V, -Vcc = -3V, Rs = 20K Ohms, Vo = -1.6V	1		-100	+0.1	nA	1, 2
			1		-200	+0.1	nA	3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: -Vcc = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
-Iib	Input Bias Current	+Vcc = 30V, -Vcc = 0V, Rs = 20K Ohms, Vo = 15V	1		-100	+0.1	nA	1, 2
			1		-200	+0.1	nA	3
		+Vcc = 2V, -Vcc = -28V, Rs = 20K Ohms, Vo = -13V	1		-100	+0.1	nA	1, 2
			1		-200	+0.1	nA	3
		+Vcc = 5V, -Vcc = 0V, Rs = 20K Ohms, Vo = 1.4V	1		-100	+0.1	nA	1, 2
			1		-200	+0.1	nA	3
		+Vcc = 2V, -Vcc = -3V, Rs = 20K Ohms, Vo = -1.6V	1		-100	+0.1	nA	1, 2
			1		-200	+0.1	nA	3
CMR	Input Voltage Common Mode Rejection	+Vcc = 30V			76		dB	1, 2, 3
		+Vcc = 5V			70		dB	1, 2, 3
ICEX	Output Leakage	+Vcc = 30V, -Vcc = 0V, Vo = +30V				1	uA	1, 2, 3
+Iil	Input Leakage Current	+Vcc = 36V, -Vcc = 0V, V+i = 34V, V-i = 0V			-500	500	nA	1, 2, 3
-Iil	Input Leakage Current	+Vcc = 36V, -Vcc = 0V, V+i = 0V, V-i = 34V			-500	500	nA	1, 2, 3
Vol	Logical "0" Output Voltage	+Vcc = 4.5V, Io = 4mA				0.4	V	1
						0.7	V	2, 3
		+Vcc = 4.5V, Io = 8mA				1.5	V	1
						2	V	2, 3
Icc	Power Supply Current	+Vcc = 5V, Vid = 15mV				2	mA	1, 2
						3	mA	3
		+Vcc = 30V, Vid = 15mV				3	mA	1, 2
						4	mA	3
DELTA Vio/ DELTA T	Temperature Coefficient of Input Offset Voltage	25 C ≤ TA ≤ 125 C	2		-25	25	uV/C	2
		-55 C ≤ TA ≤ 25 C	2		-25	25	uV/C	3
DELTA Iio/ DELTA T	Temperature Coefficient of Input Offset Current	25 C ≤ TA ≤ 125 C	2		-300	300	pA/C	2
		-55 C ≤ TA ≤ 25 C	2		-400	400	pA/C	3
AVS	Open Loop Voltage Gain	+Vcc=15V, Rl=15K Ohms, 1V ≤ Vo ≤ 11V	3		50		V/mV	4
		+Vcc=15V, Rl=15K Ohms, 1V ≤ Vo ≤ 11V	3		25		V/mV	5, 6

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: -Vcc = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Tempco Screen					4	mV	
CMRR	Tempco Screen					70	dB	
Iio	Tempco Screen					13	nA	
Iib	Tempco Screen					12	nA	

AC PARAMETERS

tRLH	Response Time: Low-to-High	+Vcc=5V, Vin=100mV, Rl=5.1K Ohms, Vod=5mV				5	uS	7, 8B
						7	uS	8A
		+Vcc=5V, Vin=100mV, Rl=5.1K Ohms, Vod=50mV				0.8	uS	7, 8B
						1.2	uS	8A
tRHL	Response Time: High-to-Low	+Vcc=5V, Vin=100mV, Rl=5.1K Ohms, Vod=5mV				2.5	uS	7, 8B
						3	uS	8A
		+Vcc=5V, Vin=100mV, Rl=5.1K Ohms, Vod=50mV				0.8	uS	7, 8B
						1	uS	8A
CS	Channel Separation	+Vcc = 20V, -Vcc = -10V, A to B			80		dB	7
		+Vcc = 20V, -Vcc = -10V, A to C			80		dB	7
		+Vcc = 20V, -Vcc = -10V, A to D			80		dB	7
		+Vcc = 20V, -Vcc = -10V, B to A			80		dB	7
		+Vcc = 20V, -Vcc = -10V, B to C			80		dB	7
		+Vcc = 20V, -Vcc = -10V, B to D			80		dB	7
		+Vcc = 20V, -Vcc = -10V, C to A			80		dB	7
		+Vcc = 20V, -Vcc = -10V, C to B			80		dB	7
		+Vcc = 20V, -Vcc = -10V, C to D			80		dB	7
		+Vcc = 20V, -Vcc = -10V, D to A			80		dB	7
		+Vcc = 20V, -Vcc = -10V, D to B			80		dB	7
		+Vcc = 20V, -Vcc = -10V, D to C			80		dB	7
VLAT	Voltage Latch (Logical "1" Input)	+Vcc = 5V, Vin = 10V, Io = 4mA				0.4	V	9

Electrical Characteristics

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: -Vcc = 0V. "Delta calculations performed on JAN S and QMLV devices at group B, subgroup 5 ONLY."

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	+Vcc = 30V, -Vcc = 0V, Vo = 15V			-1	1	mV	1
+Iib	Input Bias Current	+Vcc = 30V, -Vcc = 0V, Rs = 20K Ohms, Vo = 15V			-15	15	nA	1
-Iib	Input Bias Current	+Vcc = 30V, -Vcc = 0V, Rs = 20K Ohms, Vo = 15V			-15	15	nA	1

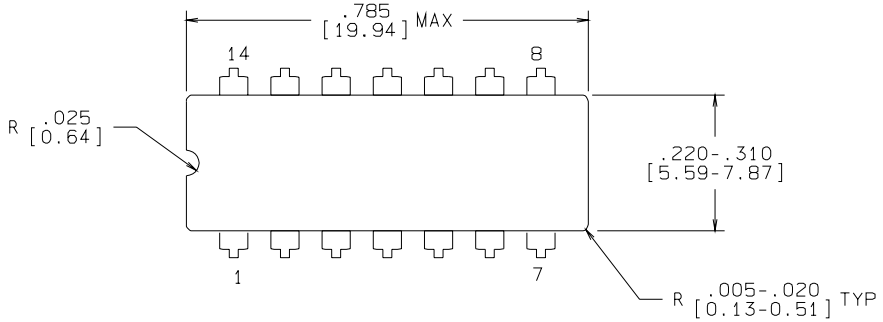
Note 1: S/S Rs = 20K Ohms, tested at Rs = 10K Ohms as equivalent test.
Note 2: Calculated parameter; for Delta Vio/Delta T use Vio test at +Vcc=30V, -Vcc=0V, Vo=15V, and for Delta Iib/Delta T use Iib test at +Vcc=30V, -Vcc=0V, Vo=15V.
Note 3: Datalog of K = V/mV.

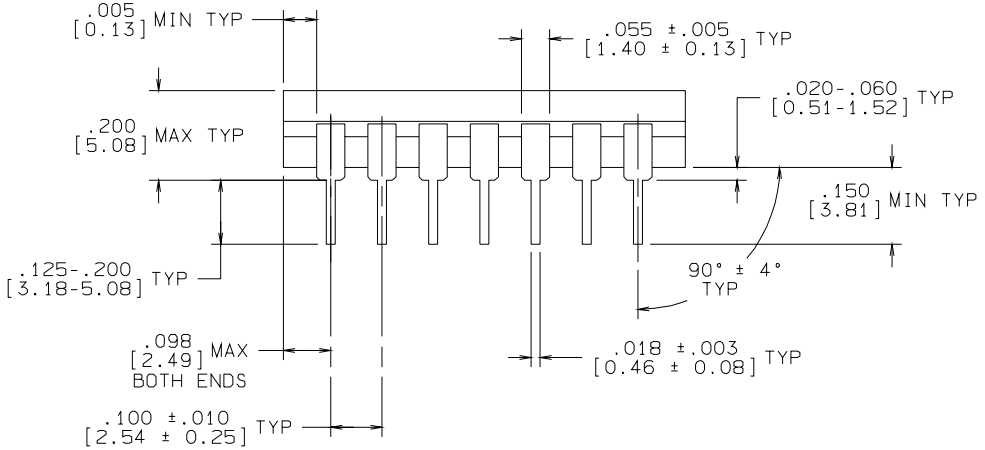
Graphics and Diagrams

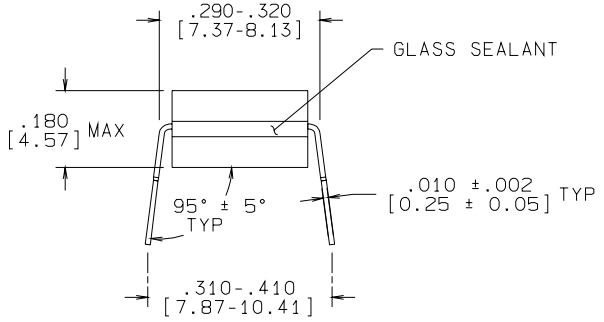
GRAPHICS#	DESCRIPTION
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
W14BRM	(blank)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/







CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

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2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 14 LEAD,

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

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