National Semiconductor

MICROCIRCUIT DATA SHEET

MNLM111-X REV 0A0

Original Creation Date: 06/28/95
Last Update Date: 11/12/98
Last Major Revision Date: 08/14/98

VOLTAGE COMPARATOR

General Description

The LM111 is a voltage comparator that has input currents nearly a thousand times lower than devices such as the LM106 or LM710. It is also designed to operate over a wider range of supply voltages; from standard ± 15V op amp supplies down to the single 5V supply used for IC logic. The output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, it can drive lamp or relay switching voltages up to 50V at currents as high as 50 mA.

Both the inputs and the output of the LM111 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided, and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40 ns) the device is also much less prone to spurious oscillations. The LM111 has the same pin configuration as LM106 and LM710.

Industry Part Number

LM111

Prime Die

LM111

NS Part Numbers

LM111E/883
LM111H/883
LM111J-8/883
LM111J/883
LM111W/883
LM111WG/883

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Operates from single 5V supply
- Input current: 150 nA max. over temperature
- Offset current: 20 nA max. over temperature
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

(Absolute Maximum Ratings)
(Note 1)

Total Supply Voltage		36V
Output to Negative Supply Voltage		50V
Ground to Negative Supply Voltage		30V
Differential Input Voltage		± 30V
Input Voltage (Note 3)		± 15V
Power Dissipation (Note 2)		500mW
Output Short Circuit Duration		10 Sec
Operating Temperature Range		-55 C to +125 C
Thermal Resistance ThetaJA		
Metal Can Pkg	(Still Air @ 0.5W)	162 C/W
	(500LF/Min Air flow @ 0.5W)	92 C/W
CERDIP (8-LEAD)	(Still Air @ 0.5W)	134 C/W
	(500LF/Min Air flow @ 0.5W)	76 C/W
CERDIP (14-LEAD)	(Still Air @ 0.5W)	97 C/W
	(500LF/Min Air flow @ 0.5W)	65 C/W
CERPACK (10-Lead)	(Still Air @ 0.5W)	231 C/W
	(500LF/Min Air flow @ 0.5W)	153 C/W
LCC (20-Lead)	(Still Air @ 0.5W)	90 C/W
	(500LF/Min Air flow @ 0.5W)	65 C/W
CERAMIC SOIC (10-Lead)	(Still Air @ 0.5W)	231 C/W
	(500LF/Min Air flow @ 0.5W)	153 C/W
ThetaJC		
Metal Can Pkg		50 C/W
CERDIP (8-Lead)		21 C/W
CERDIP (14-Lead)		20 C/W
CERPACK (10-Lead)		24 C/W
LCC (20-Lead)		21 C/W
CERAMIC SOIC (10-Lead)		24 C/W
Storage Temperature Range		-65 C to 150 C
Lead Temperature (Soldering, 10 seconds)		260 C
Voltage at Strobe Pin		V+ -5V
ESD Rating (Note 4)		300V

(Absolute Maximum Ratings) (Continued)

(Note 1)

Package Weight (Typical)	
Metal Can Pkg	TBD
CERDIP (8-Lead)	TBD
CERDIP (14-Lead)	TBD
CERPACK (10-Lead)	TBD
CERAMIC SOIC	220mg

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is PDmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: This rating applies for $\pm$15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 4: Human body model, 1.5K Ohms in series with 100pF.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V56=0, Rs=0 Ohm, ±Vcc=±15V, Vcm=0, Vout=1.4V WRT -Vcc

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Iio	Input Offset Current	Vcm=13.5V, Rs=50K Ohms			-10	10	nA	1
					-20	20	nA	2, 3
		Vcm=13.5V, V85=V86=0V, Rs=50K Ohms			-30	30	nA	1
		Vcm=-14.5V, Rs=50K Ohms			-10	10	nA	1
					-20	20	nA	2, 3
		Vcm=-14.5V, V85=V86=0V, Rs=50K Ohms			-30	30	nA	1
		Rs=50K Ohms			-10	10	nA	1
					-20	20	nA	2, 3
		V85=V86=0V, Rs=50K Ohms			-30	30	nA	1
Iib	Input Bias Current	Vcm=13.5V, Rs=50K Ohms				100	nA	1
						150	nA	2, 3
		Vcm = -14.5V, Rs=50K Ohms				100	nA	1
						150	nA	2, 3
		Rs=50K Ohms				100	nA	1
						150	nA	2, 3
Ilout	Output Leakage Current	Vcc=± 18V, Vout=35V WRT -Vcc, I5+I6=5mA				10	nA	1
						500	nA	2, 3
Ilg	Ground Leakage Current	Vcc= ± 18V, Vout=50V WRT -Vcc, I5+I6=5mA				25	nA	1
						500	nA	2
Vsat	Saturation Voltage	Vin= -5mV, I7=50mA				1.5	V	1, 2, 3
		Vin= -6mV, I7=8mA				0.4	V	1, 2, 3
Icc-	Negative Supply Current					5	mA	1, 2
						15	mA	3
Icc+	Positive Supply Current					6	mA	1, 2
						15	mA	3
Il1	Input Leakage Current	Vcc= ± 18V, V28=1V, V38=30V, Vout=50V WRT -Vcc, I5+I6=5mA				10	nA	1
						30	nA	2
Il2	Input Leakage Current	Vcc= ± 18V, V38=1V, V28=30V, Vout=50V WRT -Vcc, I5+I6=5mA				10	nA	1
						30	nA	2

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V56=0, Rs=0 Ohm, ±Vcc=±15V, Vcm=0, Vout=1.4V WRT -Vcc

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vo(STB)	Collector Output Voltage (ST)		1		14		V	1
		ISTB = 3mA	1		14		V	1
Vio	Input Offset Voltage	Vcm=13.5V			-3	3	mV	1
					-4	4	mV	2, 3
		Vcm=13.5V, V85=V86=0V			-3	3	mV	1
		Vcm= -14.5V			-3	3	mV	1
					-4	4	mV	2, 3
		Vcm= -14.5V, V85=V86=0V			-3	3	mV	1
					-3	3	mV	1
					-4	4	mV	2, 3
		V85=V86=0V			-3	3	mV	1
		Vout=0.4V, +Vcc=4.5V, -Vcc=0V, Vcm=3V			-5	5	mV	1
					-6	6	mV	2, 3
		Vout=4.5V, +Vcc=4.5V, -Vcc=0V, Vcm=3V			-3	3	mV	1
					-4	4	mV	2, 3
		Vout=0.4V, +Vcc=4.5V, -Vcc=0V, Vcm=0.5V			-5	5	mV	1
					-6	6	mV	2, 3
		Vout=4.5V, +Vcc=4.5V, -Vcc=0V, Vcm=0.5V			-3	3	mV	1
					-4	4	mV	2, 3
Avs	Large Signal Gain	-12V ≤ Vout ≤ 35V, Rl=1K Ohm	2		40		V/mV	4
			2		30		V/mV	5, 6

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: V56=0, Rs=0 Ohm, ±Vcc=±15V, Vcm=0, Vout=1.4V WRT -Vcc

tr	Response Time					400	nS	7

Electrical Characteristics

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V56=0, Rs=0 Ohms, ±Vcc = ±15V, Vcm=0, Vout=1.4V WRT -Vcc. "Deltas not required on B-Level product. Deltas required for S-Level product ONLY as specified on Internal Processing Instructions (IPI)."

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Iib	Input Bias Current	Rs=50K Ohms			-10	10	nA	1
Vio	Input Offset Voltage				-0.5	0.5	mV	1

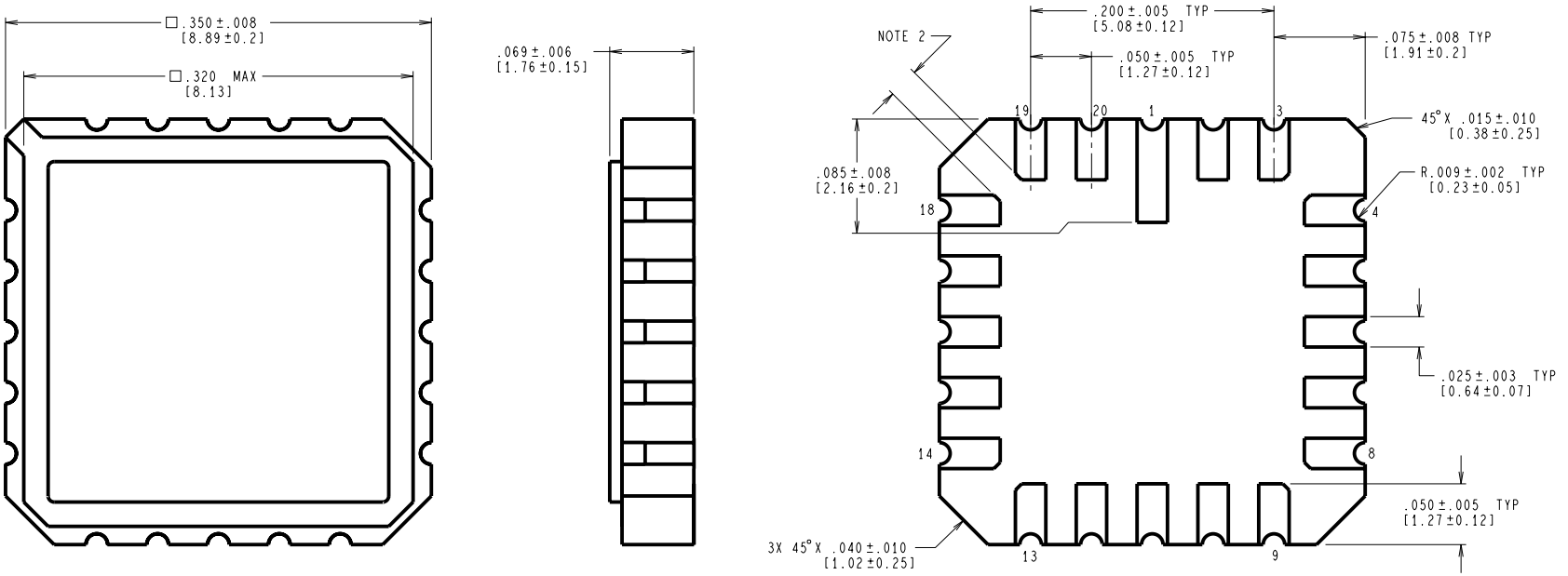
Note 1: Tested on LTX system.
Note 2: Datalog reading in K = V/mV.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
05815HRA3	LCC (E), TYPE C, 20 TERMINAL (B/I CKT)
06047HRA2	CERDIP (J), 8 LEAD (B/I CKT)
08358HRB2	METAL CAN, (H) TO-99,8 LEAD,.200 DIA P.C.(B/I CKT)
08570HRA1	CERDIP (J), 14 LEAD (B/I CKT)
09569HRC2	CERPACK (W), 10 LEAD (B/I CKT)
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
H08CRF	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000264A	METAL CAN (H), 8 LEAD (PINOUT)
P000265A	CERDIP (J), 8 LEAD (PINOUT)
P000266A	CERDIP (J), 14 LEAD (PINOUT)
P000267A	CERPACK (W), 10 LEAD (PINOUT)
P000314B	LCC (E), 20 LEAD (PINOUT)
P000373A	CERAMIC SOIC (WG), 10 LEAD (PINOUT)
W10ARG	CERPACK (W), 10 LEAD (P/P DWG)
WG10ARC	CERAMIC SOIC (WG), 10 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION INCH [MM]

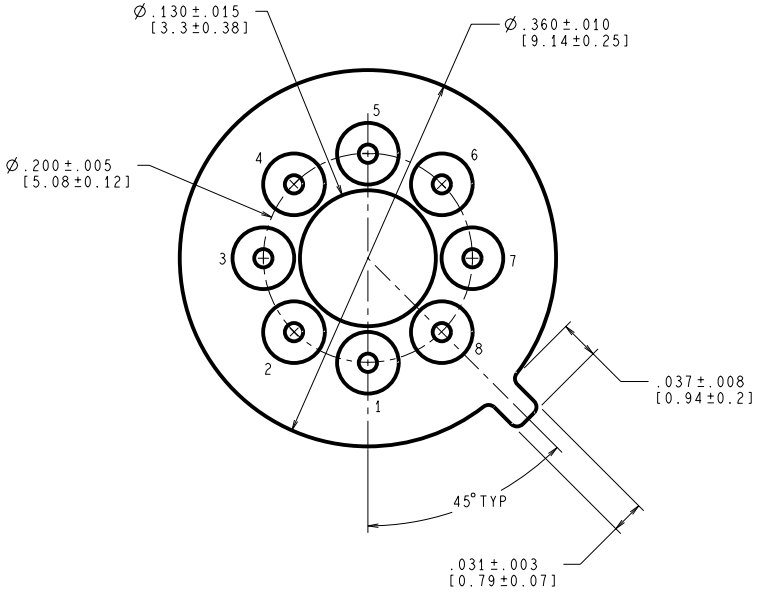
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

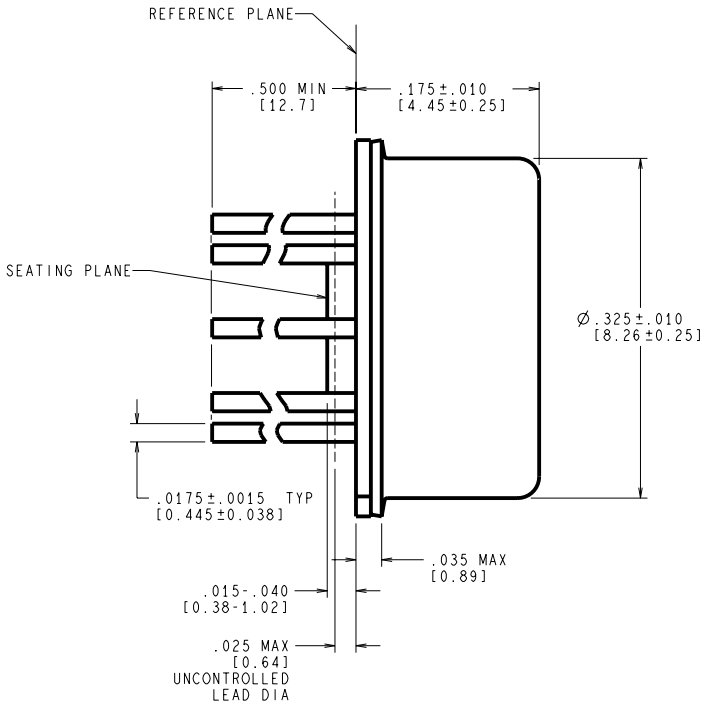
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE & REDRAW PER CURRENT STANDARD; UPDATE MIL/AERO STAMP & TITLE.	11002	06/22/95	MS/





CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEADS TO BE LOCATED WITHIN .007 IN/ 0.18 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
2. STANDARD METAL CAN TYPE: SOLID BASE WITH CERAMIC STANDOFF.
3. APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
4. REFERENCE JEDEC REGISTRATION TO-99, JEDEC PUBLICATION No.95.

APPROVALS	DATE
DRAWN: MARTA SUCHY	06/22/95
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

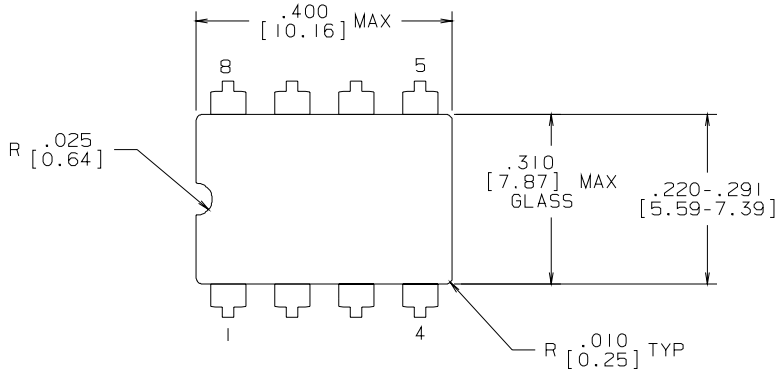
METAL CAN, TO-99, 8 LEAD, .200 DIA P.C.

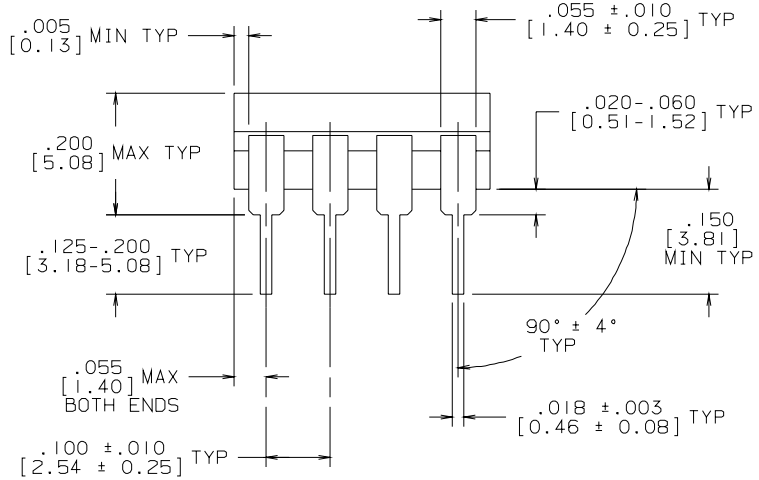
PROJECTION — INCH [MM]

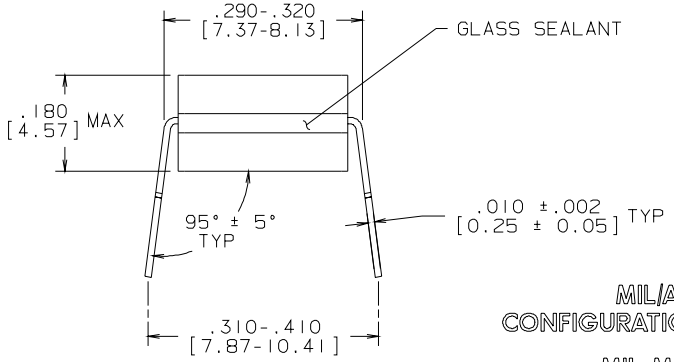
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-H08C	F

DO NOT SCALE DRAWING — SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

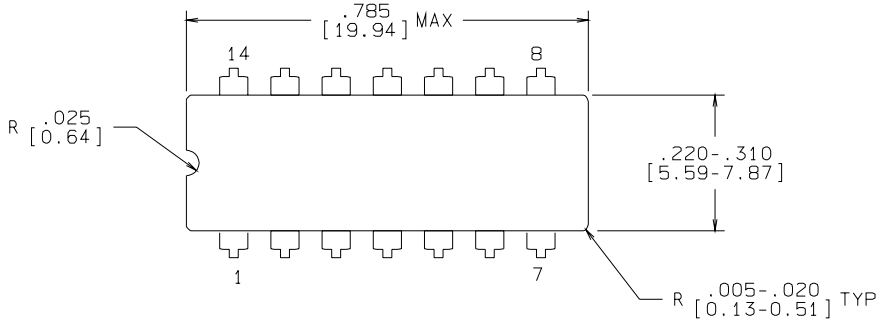
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

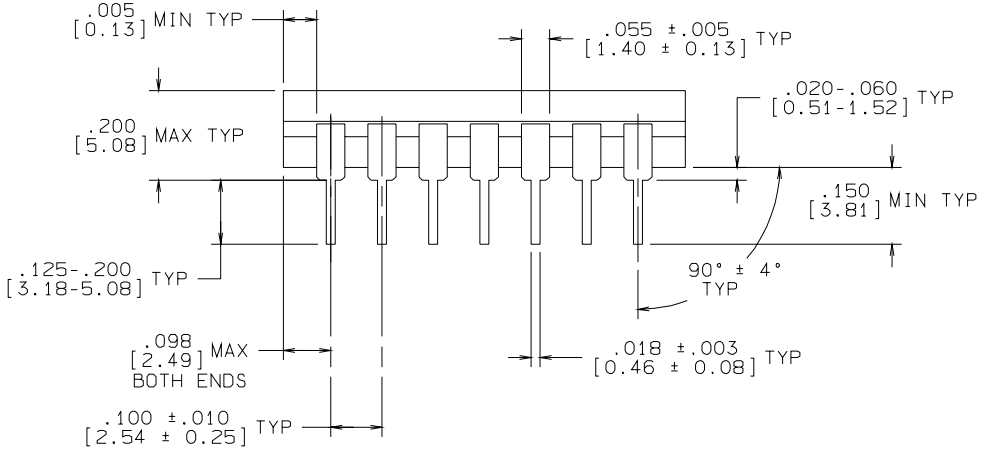
CERDIP (J), 8 LEAD

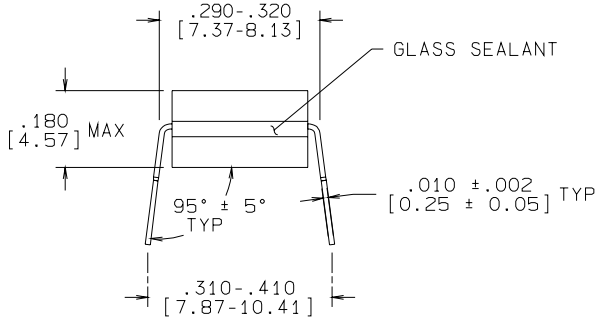
SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/







CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

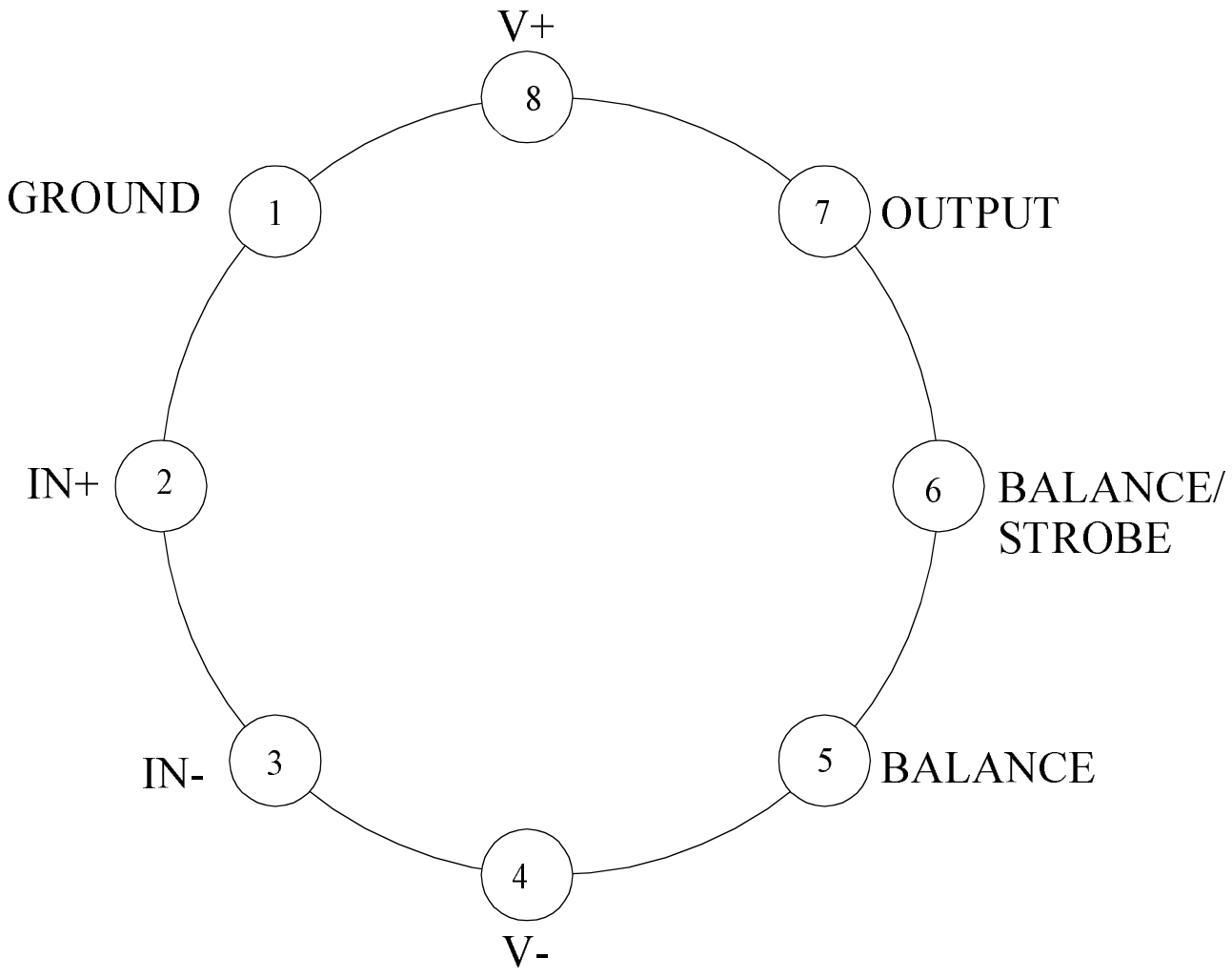
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 14 LEAD,

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1



LM111H
8 - PIN METAL CAN
CONNECTION DIAGRAM
TOP VIEW
P000264A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

LM111J-8

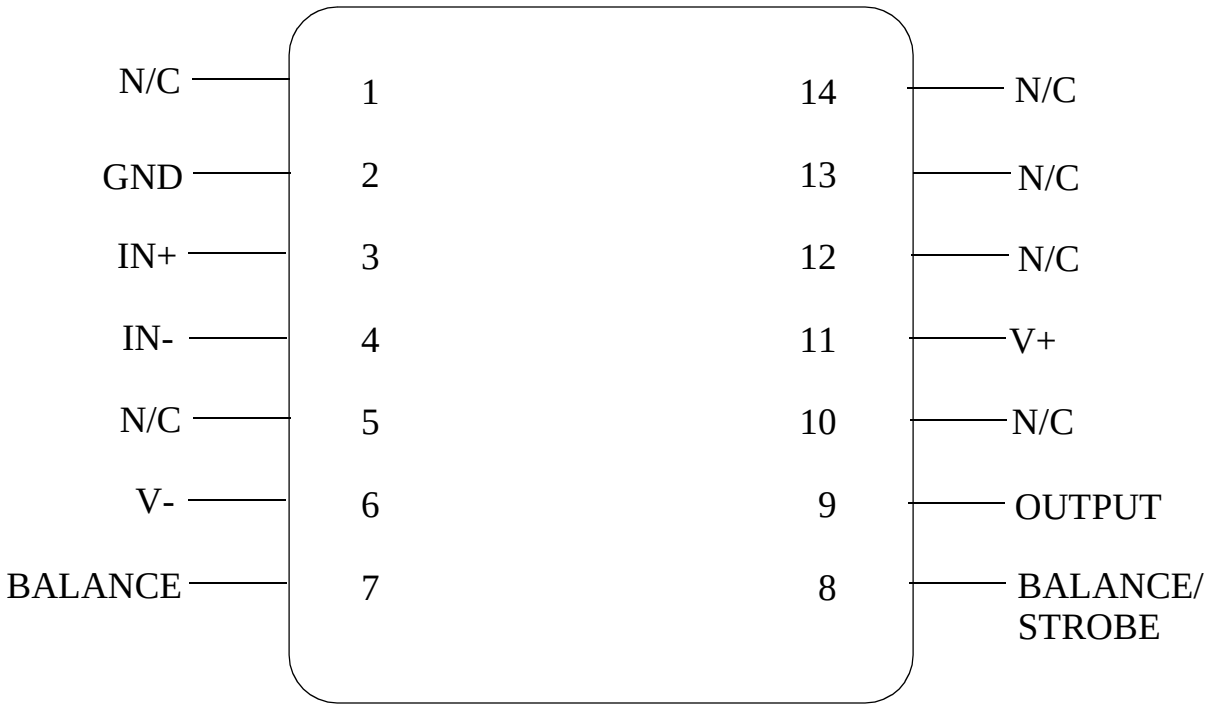
8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

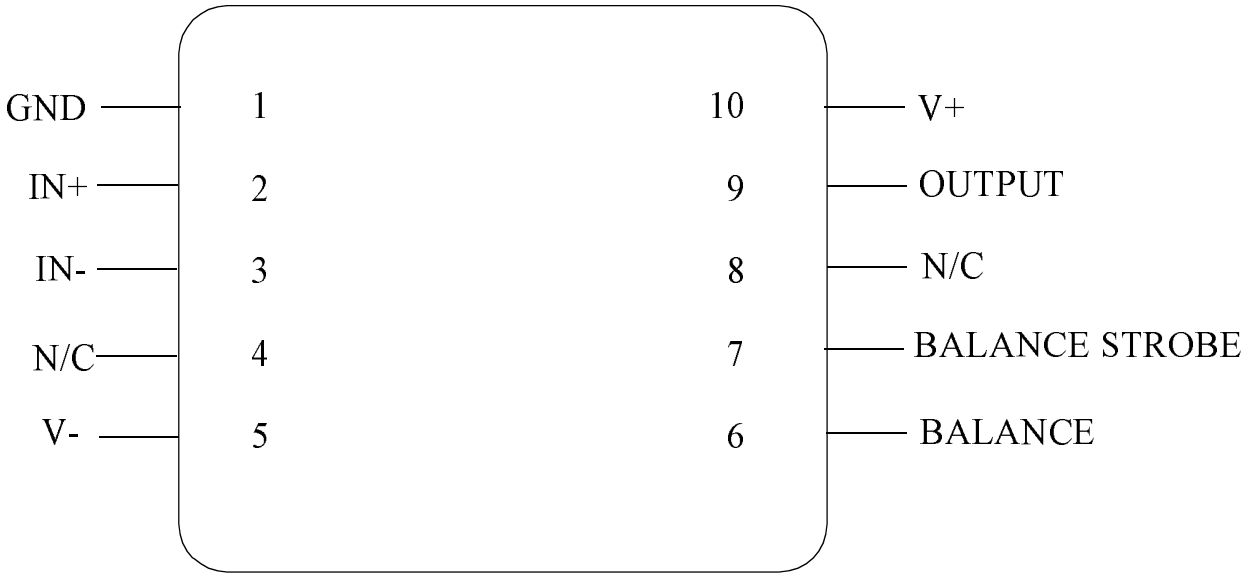
P000265A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM111J
14 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000266A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM111W

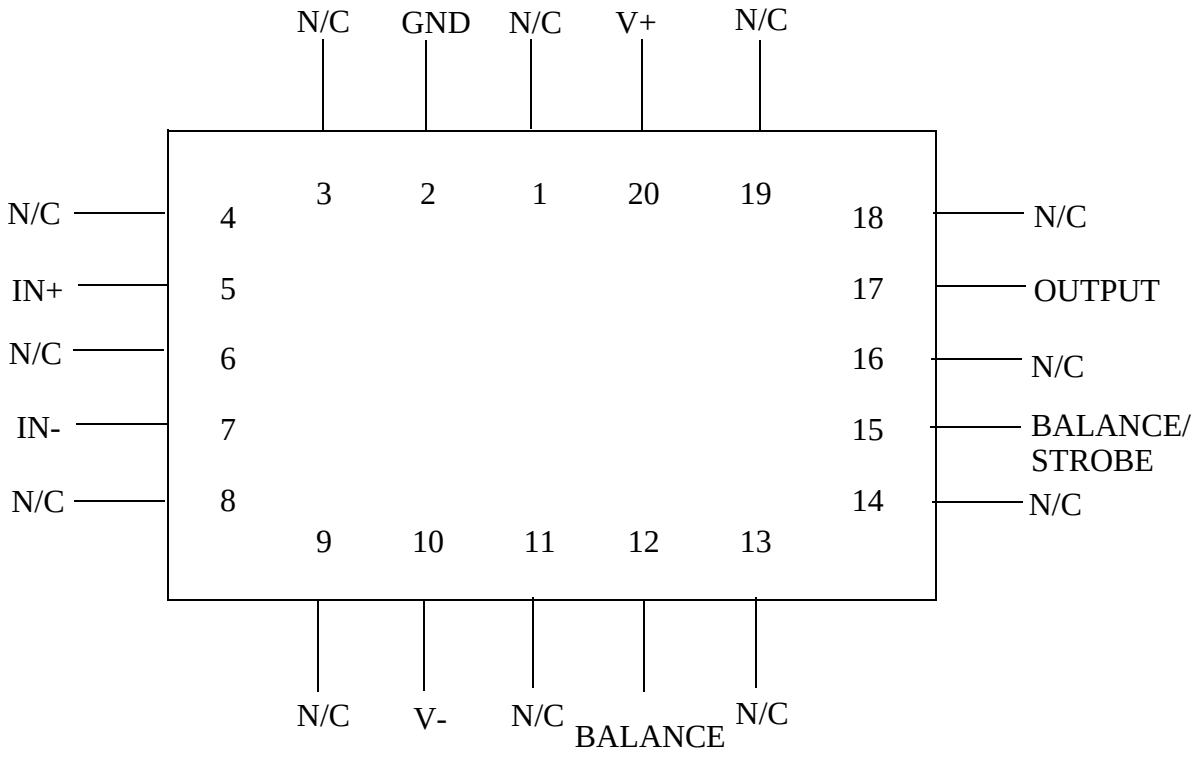
10 - LEAD CERPACK

CONNECTION DIAGRAM

TOP VIEW

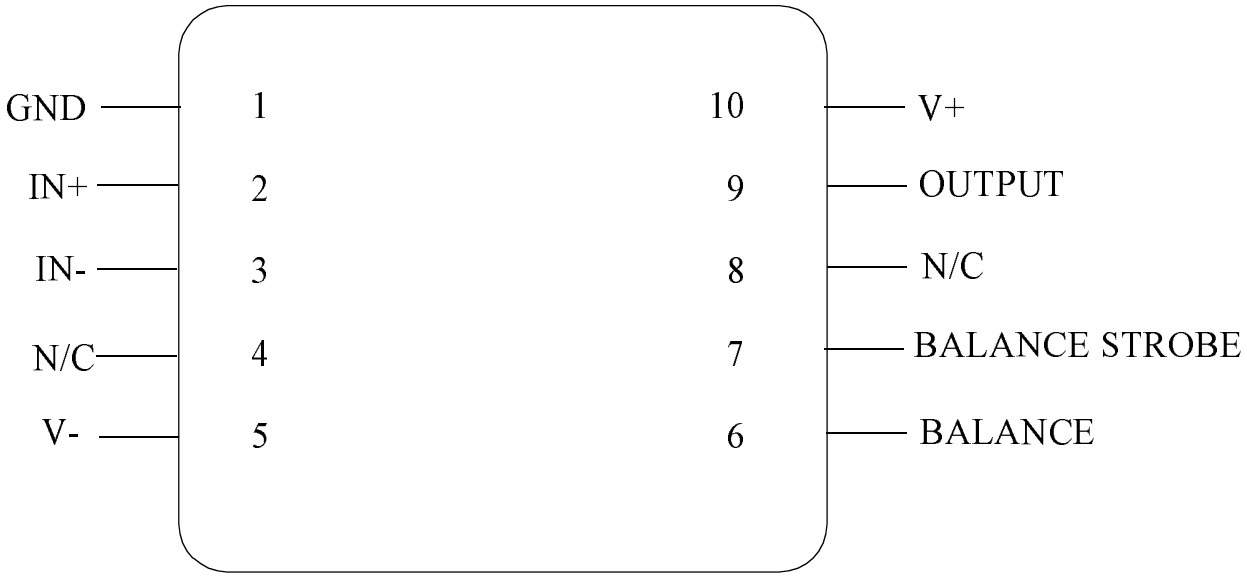
P000267A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM111E
20 - LEAD LCC
CONNECTION DIAGRAM
TOP VIEW
P000314B

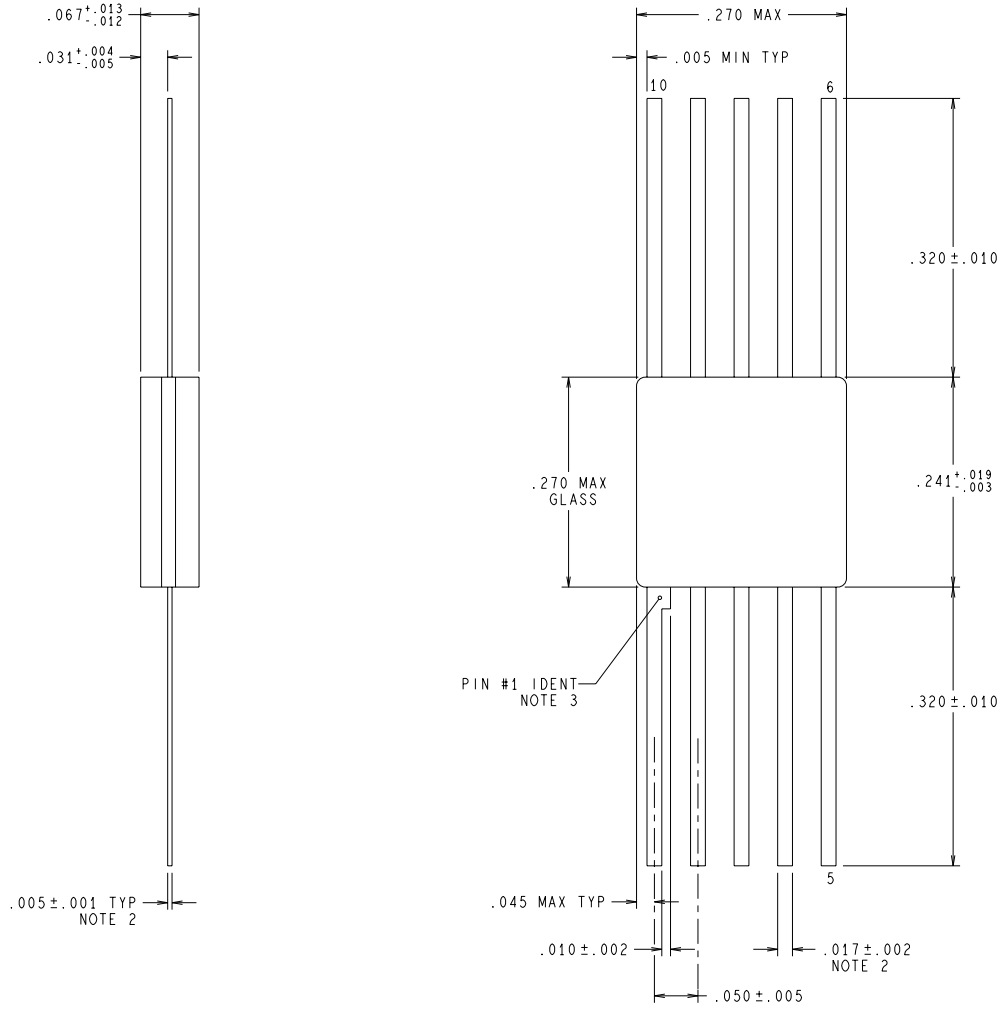
National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM111WG
10 - LEAD CERAMIC SOIC
CONNECTION DIAGRAM
TOP VIEW
P000373A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE AND REDRAW PER NEW STANDARD.	10510	07/28/94	DEG/AEP
G	.017±.002 WAS .017±.020.	10654	10/21/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
4. REFERENCE JEDEC REGISTRATION MO-003, VARIATION AG, DATED 06/01/76.

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: D.E.Grady	07/28/94
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

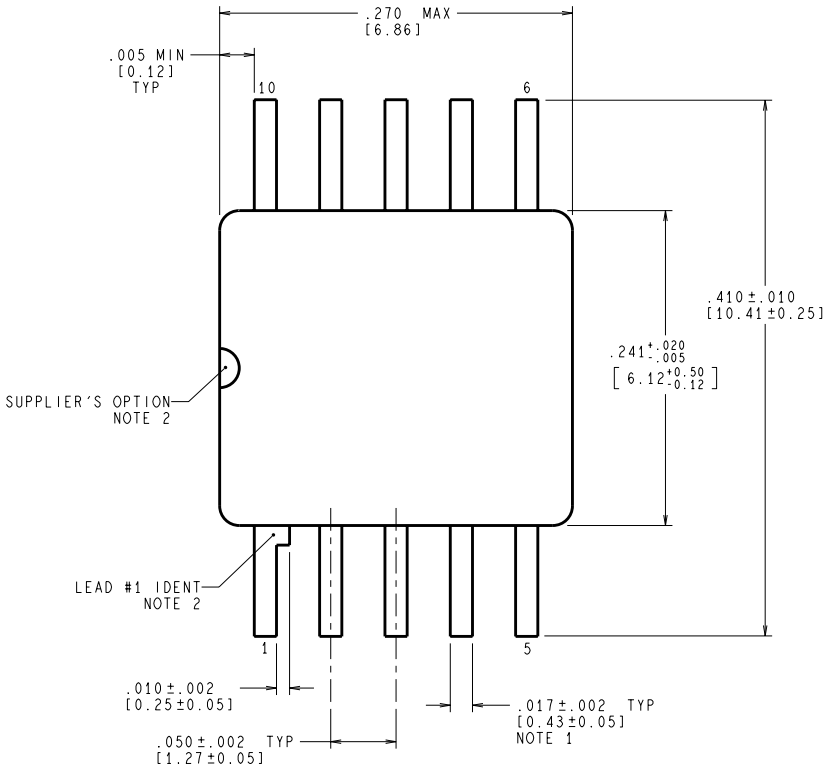
CERPACK, 10 LEAD

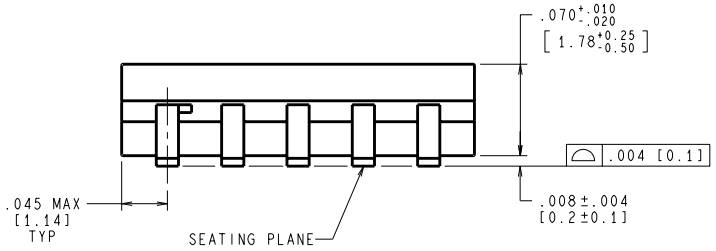
PROJECTION — INCH [MM]

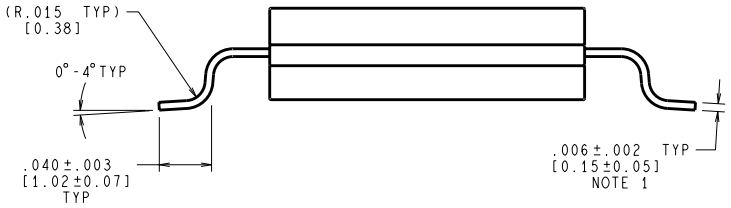
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W10A	G

DO NOT SCALE DRAWING — SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11374	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002 DIM .040±.003 WAS .037±.003	11441	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11838	10/08/1997	TL/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 10 LEAD, GULL WING

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG10A	C

DO NOT SCALE DRAWING | SHEET 1 of 1