National
Semiconductor

MICROCIRCUIT DATA SHEET

MNLM158A-X-RH REV 0A0

Original Creation Date: 01/14/99
Last Update Date: 02/04/99
Last Major Revision Date: 01/14/99

LOW POWER, DUAL OPERATIONAL AMPLIFIER: ALSO AVAILABLE GUARANTEED TO 50K RAD (Si) TESTED TO MIL-STD-883, METHOD 1019

General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5V DC power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ± 15V DC power supplies.

Industry Part Number

LM158

Prime Die

LM158

Controlling Document

SEE FEATURES SECTION

NS Part Numbers

LM158AH-QMLV
LM158AH-SMD
LM158AH/883
LM158AHLQML
LM158AHLQMLV
LM158AJ-QMLV
LM158AJ/883
LM158AJLQML
LM158AJLQMLV

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- CONTROLLING DOCUMENTS:

LM158AH-QMLV	5962-8771002VGA
LM158AH-SMD	5962-8771002GA
LM158AH/883	
LM158AHLQML	5962L8771002QGA
LM158AHLQMLV	5962L8771002VGA
LM158AJ-QMLV	5962-8771002VPA
LM158AJ/883	5962-8771002PA
LM158AJLQML	5962L8771002QPA
LM158AJLQMLV	5962L8771002VPA

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage, V+	32Vdc
Differential Input Voltage	32Vdc
Input Voltage	-0.3Vdc to +32Vdc
Power Dissipation (Note 2)	830 mW
Output Short-Circuit to GND (Note 3)	
(One Amplifier)	
V+ ≤ 15Vdc and TA = 25 C	Continuous
Maximum Junction Temperature	150 C
Input Current (Vin < -0.3Vdc) (Note 4)	50mA
Operating Temperature Range	-55 C to +125 C
Storage Temperature Range	-65 C to +150 C
Lead Temperature	
(Soldering, 10 seconds)	
H-Pkg	300 C
J-Pkg	260 C
Thermal Resistance	
ThetaJA	
H-Pkg (Still Air)	155 C/W
(500LF/Min Air Flow)	80 C/.W
J-Pkg (Still Air)	132 C/W
(500LF/Min Air Flow)	81 C/W
ThetaJC	
H-Pkg	42 C/W
J-Pkg	23 C/W
Package Weight	
(Typcial)	
H-Pkg	TBD
J-Pkg	TBD
ESD Tolerance (Note 5)	250V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Short circuits from ther output to V+ from Vdc, can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

(Continued)

Note 4: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward baised and thereby a acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater that -0.3Vdc (at 25C).

Note 5: Human body model, 1.5 K ohms in series with 100 pF.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: All voltages referenced to device ground.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Icc	Power Supply Current	V+ = 5V, Rl = 100K, Vo = 1.4V				1.2	mA	1, 2, 3
		V+ = 30V, Rl = 100K, Vo = 1.4V				3	mA	1
						4	mA	2, 3
Voh	Output Voltage High	V+ = 30V, Rl = 2K Ohms			26		V	1, 2, 3
		V+ = 30V, Rl = 10K Ohms			27		V	1, 2, 3
Vol	Output Voltage Low	V+ = 30V, Rl = 10K Ohms				40	mV	1
						100	mV	2, 3
		V+ = 30V, Isink = 1uA				40	mV	1
						100	mV	2, 3
		V+ = 5V, Rl = 10K Ohms				40	mV	1
						100	mV	2, 3
Isink	Output Sink Current	V+ = 15V, Vout = 200mV, Vin = 65 mV			12		uA	1
		V+ = 15V, Vout = 2V, Vin = 65mV			10		mA	1
					5		mA	2, 3
Isource	Output Source Current	V+ = 15V, Vin = 65mV, Vout = 2V				-20	mA	1
						-10	mA	2, 3
Ios	Short Circuit Current	V+ = 5V, Vout = 0V			-60		mA	1
Vio	Input Offset Voltage	V+ = 30V, Vcm = 0V, Rs = 50 Ohms, Vo = 1.4V			-2	2	mV	1
					-4	4	mV	2, 3
		V+ = 30V, Vcm = 28V, Rs = 50 Ohms, Vo = 1.4V			-4	4	mV	2, 3
		V+ = 5V, Vcm = 0V, Rs = 50 Ohms, Vo = 1.4V			-2	2	mV	1
					-4	4	mV	2, 3
		V+ = 30V, Vcm = 28.5V, Rs = 50 Ohms,Vo = 1.4V			-2	2	mV	1
CMRR	Common Mode Rejection Ratio	V+ = 30V, Vin = 0V to 28.5V, Rs = 50 Ohms			70		dB	1
Iib+	Input BIas Current	V+ = 5V, Vcm = 0V			-50	-1	nA	1
					-100	-1	nA	2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: All voltages referenced to device ground.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Iib-	Input BIas Current	V+ = 5V, Vcm = 0V			-50	-1	nA	1
					-100	-1	nA	2, 3
Iio	Input Offset Current	V+ = 5V, Vcm = 0V			-10	10	nA	1
					-30	30	nA	2, 3
PSRR	Power Supply Rejection Ratio	V+ = 5V to 30V, Vcm = 0V			65		dB	1
Vcm	Common Mode Voltage Range	V+ = 30V	1			28.5	V	1
			1			28.0	V	2, 3
Vdiff	Differential Input Voltage		2			32	V	1, 2, 3
Avs	Large Signal Gain	V+ = 15V, Rl = 2K Ohms, Vo = 1V to 11V			50		V/mV	4
					25		V/mV	5, 6

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: All voltages referenced to device ground. "Delta calculations performed on Jan "S" and "QMLV" devices at Group B, Subgroup 5 only."

Vio	Input Offset Voltage	V+ = 30V, Vcm = 0V, Rs = 50 Ohms, Vo = 1.4V			-0.5	0.5	mV	1
		V+ = 30V, Vcm = 28V, Rs = 50 Ohms, Vo = 1.4V			-0.5	0.5	mV	1
		V+ = 5V, Vcm = 0V, Rs = 50 Ohms, Vo = 1.4V			-0.5	0.5	mV	1
Iib+	Input Bias Current	V+ = 5V, Vcm = 0V			-10	10	nA	1
Iib-	Input Bias Current	V+ = 5V, Vcm = 0V			-10	10	nA	1

DC/AC PARAMETERS: POST RADIATION LIMITS +25 C

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: All voltages referenced to device ground.

Vio	Input Offset Voltage	V+ = 30V, Vcm = 0V, Rs = 50 Ohms, Vo = 1.4V	3		-4	4	mV	1
		V+ = 30V, Vcm = 28V, Rs = 50 Ohms, Vo = 1.4V	3		-4	4	mV	1
		V+ = 5V, Vcm = 0V, Rs = 50 Ohms, Vo = 1.4V	3		-4	4	mV	1
±Iib	Input Bias Current	V+ = 5V, Vcm = 0V	3		-60	-1	nA	1

Note 1: Parameter tested go-no-go only.
Note 2: Guaranteed parameter not tested.
Note 3: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, Method 1019.5.

Graphics and Diagrams

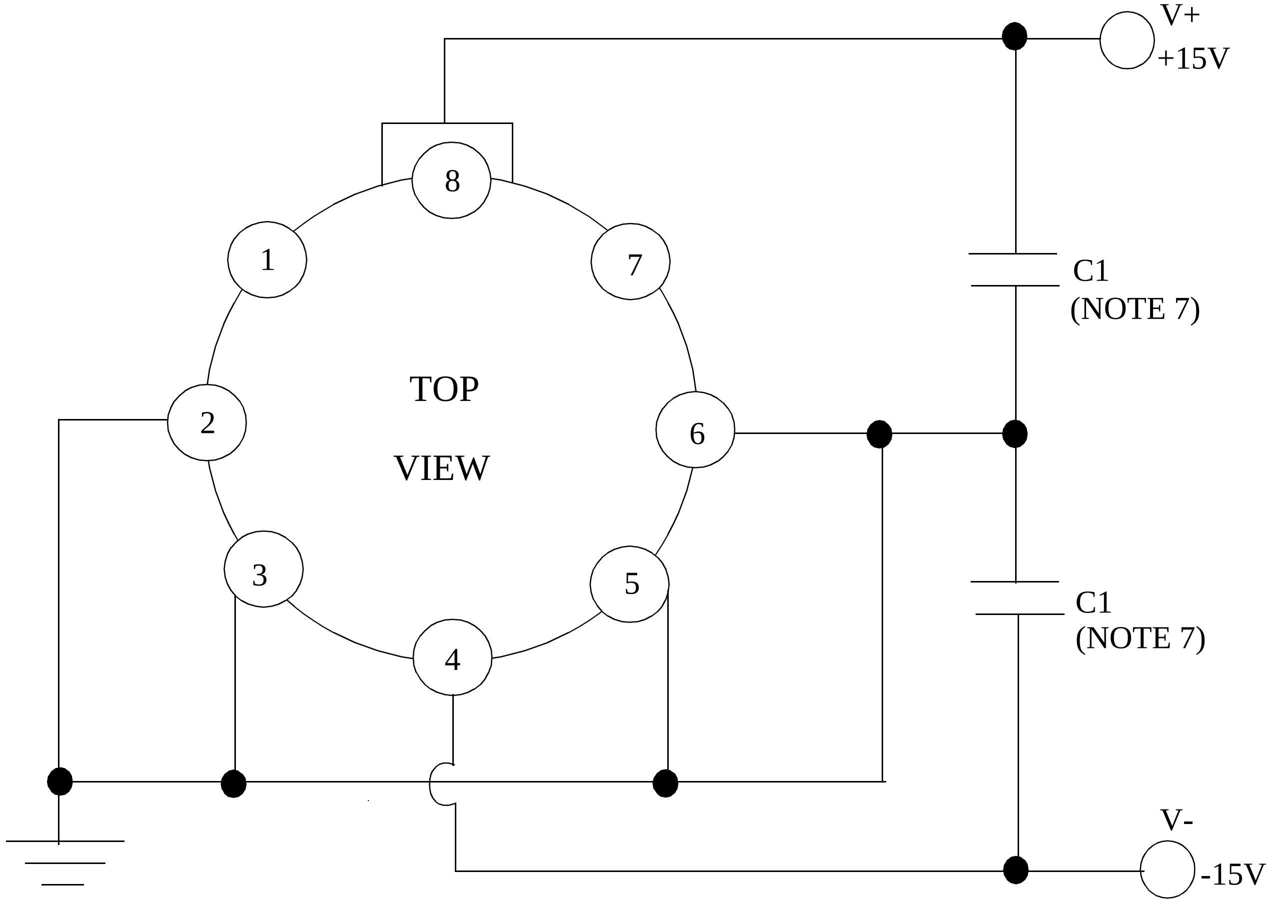
GRAPHICS#	DESCRIPTION
08571HRC2	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (B/I CKT)
09294HR01	CERDIP (J), 8 LEAD (B/I CKT)
H08CRF	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000273A	METAL CAN (H), TO-99, 8 LD, .200 DIA P.C. (PINOUT)
P000274A	CERDIP (J), 8 LEAD (PINOUT)

See attached graphics following this page.

GENERAL NOTES:

1. GENERIC - INDUSTRY TYPE DEVICES THAT MAY BE USED WITH THIS CIRCUIT SHALL BE AS SPECIFIED IN NSC BURN-IN CIRCUIT LIST R512B-04.
2. ALL 1/4 AND 1/2 WATT RESISTORS SHALL BE METAL FILM. ALL 1, 2, AND 3 WATT RESISTORS SHALL BE WIRE WOUND. TOLERANCE SHALL BE +/-5% UNLESS OTHERWISE SPECIFIED.
3. ALL VOLTAGES SPECIFIED SHALL BE MEASURED AT THE "DEVICE UNDER TEST" PIN AND SHALL BE MINIMUM VALUES UNLESS OTHERWISE SPECIFIED.
4. WHEN APPLICABLE, CLOCK PULSES SPECIFIED SHALL HAVE 50% DUTY CYCLE.
5. THIS DRAWING COMPLIES WITH MIL-PRF-38535, WHEN APPLICABLE.

ECN	REV	APPROVALS	DATE
1596	C	TM	9/25/80
BIC- 00376	C1	R.Wallace	11/7/83
07375	C2	J.GOMEZ	9/17/97



DUT CONDITIONS

SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS	SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS
V+	15	16	VOLTS				
V-	-16	-15	VOLTS				

COMPONENT REQUIREMENTS PER POSITION

REF DESIG.	QTY	DESCRIPTION
C1	2	0.005µf X7R

NOTES:

6. DFC Pin 1, 7
7. C1 EVERY 6th Socket (Min)
8. LM1558, LM158

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MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

BURN-IN CIRCUIT

SH 1 OF 1

CUSTOMER	PACKAGE TYPE	MIL	NSC	TEST CONDITION
	H08		NOTE 8	A

ORIGINATOR	DATE	CHECKED BY	DATE	DRAWING NUMBER	REV
J.GOMEZ	9/17/97			08571HR	C2

GENERAL NOTES:

1. GENERIC - INDUSTRY TYPE DEVICES THAT MAY BE USED WITH THIS CIRCUIT SHALL BE AS SPECIFIED IN NSC BURN-IN CIRCUIT LIST R512B-04.
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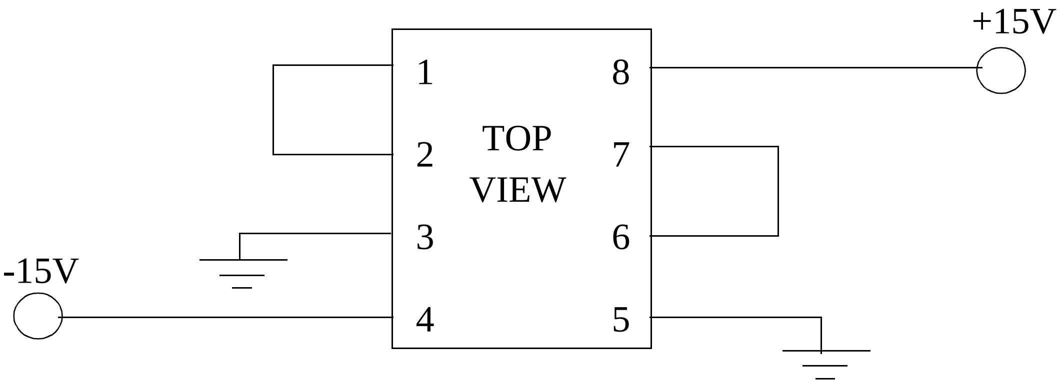
3. ALL VOLTAGES SPECIFIED SHALL BE MEASURED AT THE "DEVICE UNDER TEST" PIN AND SHALL BE MINIMUM VALUES UNLESS OTHERWISE SPECIFIED.
4. WHEN APPLICABLE, CLOCK PULSES SPECIFIED SHALL HAVE 50% DUTY CYCLE.
5. THIS DRAWING COMPLIES WITH MIL-PRF-38535, WHEN APPLICABLE.

ECN	REV	APPROVALS	DATE
0256	—	CD	3/3/76
	01	J. GOMEZ	3/17/98



DUT CONDITIONS

SYMBOL	LIMITS		UNITS		SYMBOL	LIMITS		UNITS
	MIN.	MAX.				MIN.	MAX.	
V+	14	16	VOLTS					
V-	-16	-14	VOLTS					

COMPONENT REQUIREMENTS PER POSITION

REF DESIG.	QTY	DESCRIPTION

Notes:

6. LM1558, LM158, LM158A

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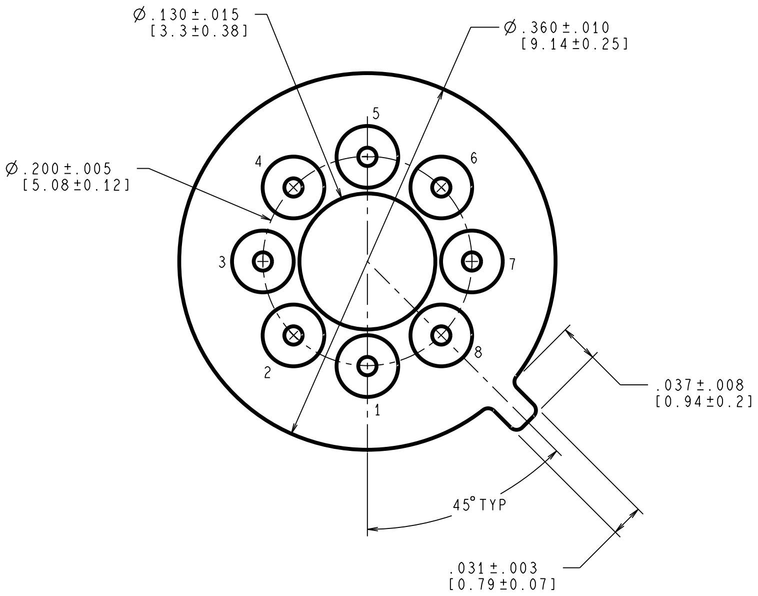
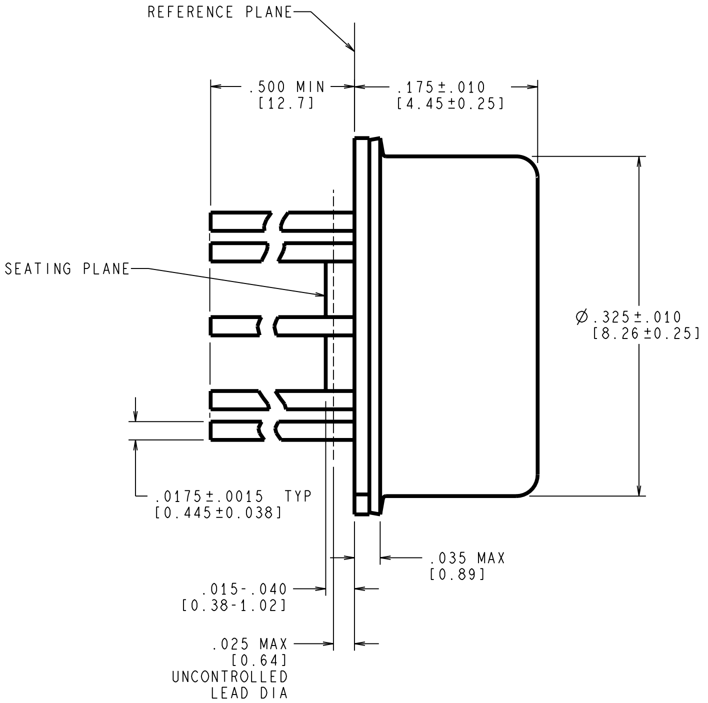
BURN-IN CIRCUIT

SH **1** OF **1**

CUSTOMER	PACKAGE TYPE **J08**	MIL	NSC **Note 6**	TEST CONDITION **C**	
ORIGINATOR **J. GOMEZ**	DATE **3/17/98**	CHECKED BY	DATE	DRAWING NUMBER **09294HR**	REV **01**

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE & REDRAW PER CURRENT STANDARD; UPDATE MIL/AERO STAMP & TITLE.	11002	06/22/95	MS/





CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEADS TO BE LOCATED WITHIN .007 IN/ 0.18 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
2. STANDARD METAL CAN TYPE: SOLID BASE WITH CERAMIC STANDOFF.
3. APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
4. REFERENCE JEDEC REGISTRATION TO-99, JEDEC PUBLICATION No.95.

APPROVALS	DATE
DRAWN MARTA SUCHY	06/22/95
DFTG. CHK.	
ENGR. CHK.	
PROJECTION INCH [MM]	

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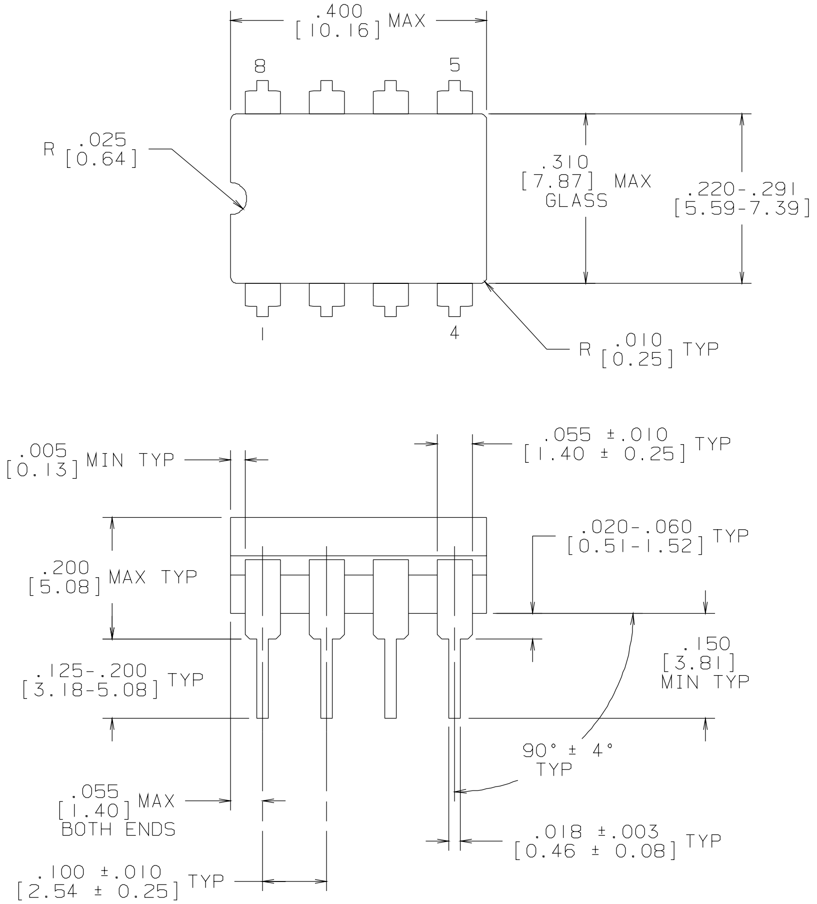
2900 Semiconductor dr, Santa Clara, CA 95052-8090

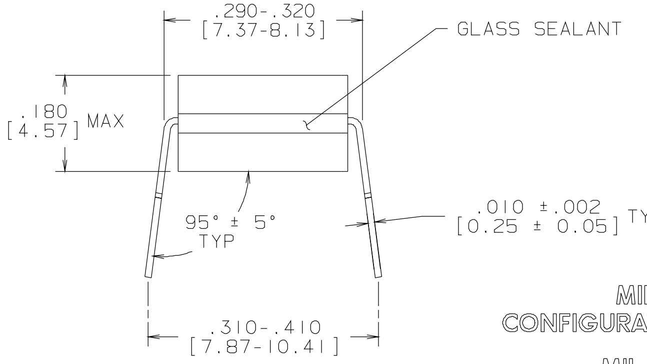
METAL CAN,
TO-99, 8 LEAD,
.200 DIA P.C.

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-H08C	F

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/





MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

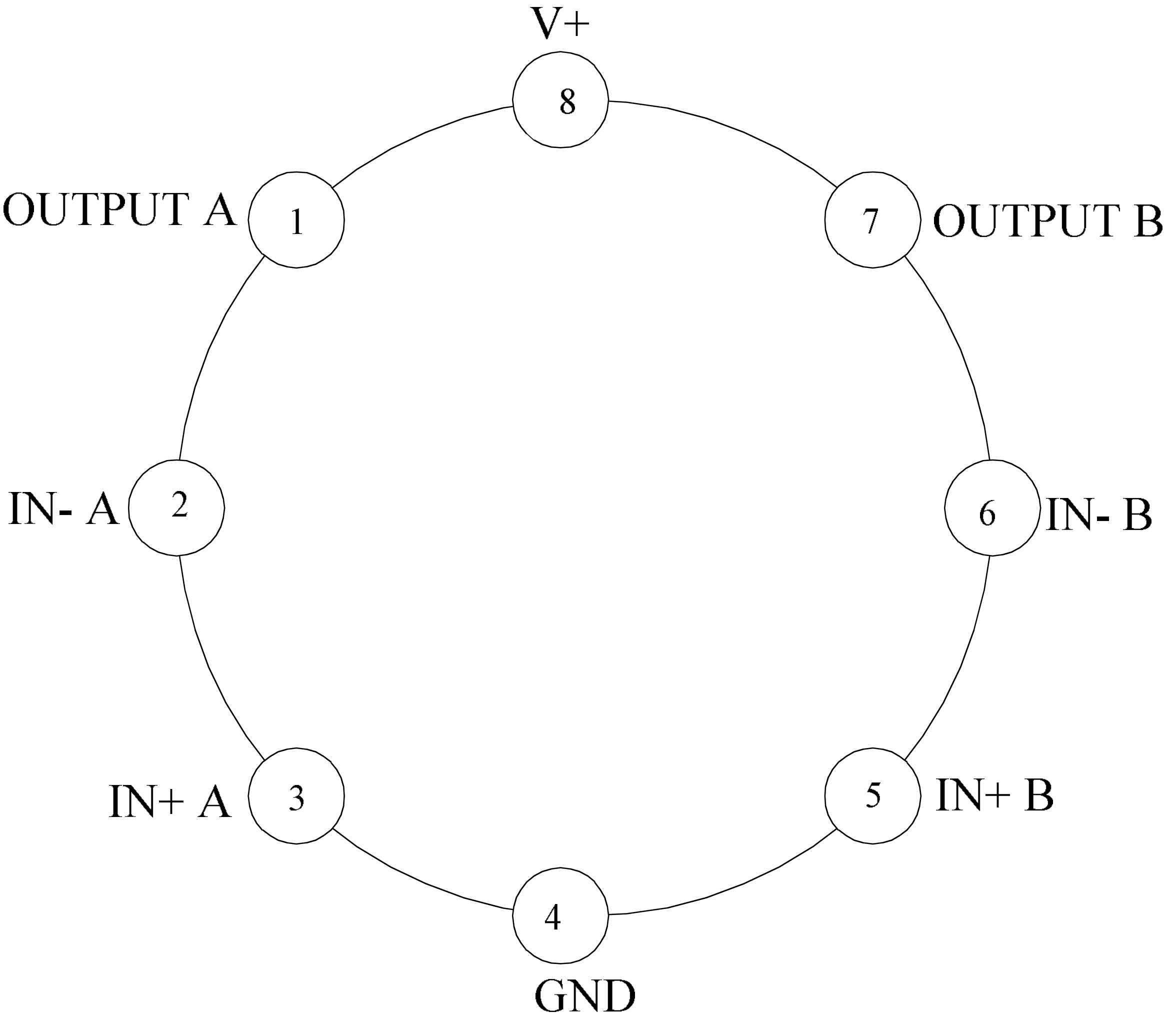
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J),
8 LEAD

PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
INCH [MM]	N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING

SHEET 1 OF 1



LM158AH, LM158H
8 - PIN METAL CAN
CONNECTION DIAGRAM
TOP VIEW
P000273A

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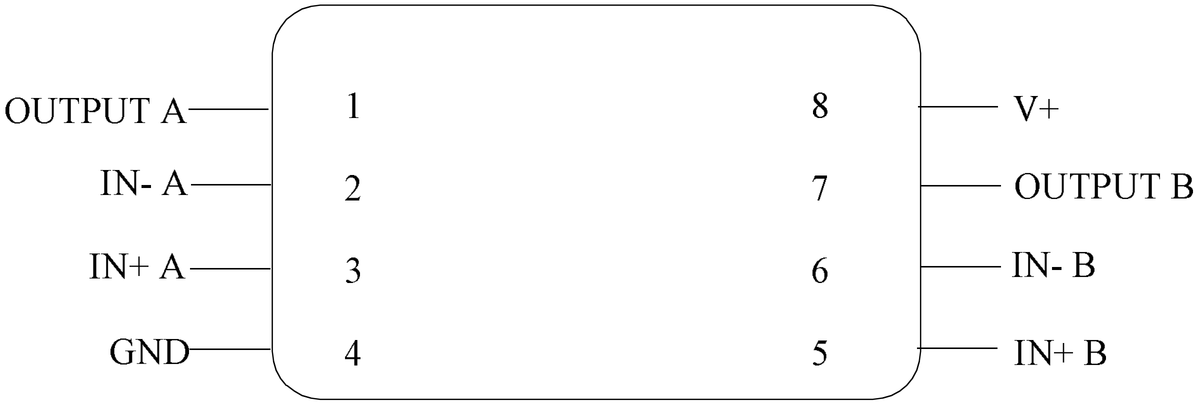

LM158AJ, LM158J
8 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000274A

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2900 SEMICONDUCTOR DRIVE
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Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003236	02/04/99	Rose Malone	Initial MDS Release: MNLM158A-X-RH, Rev. 0A0 - Added Rad Hard Devices and Limits. Replaces MNLM158A-X, Rev. 3A0.