National Semiconductor

MICROCIRCUIT DATA SHEET

MNLM193-X REV 0D1

Original Creation Date: 05/18/95
Last Update Date: 10/05/98
Last Major Revision Date: 05/18/95

LOW POWER LOW OFFSET VOLTAGE DUAL COMPARATORS

General Description

The LM193 consists of two independent precision voltage comparators with an offset voltage specification as low as 5.0mV max for two comparators which were designed specically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristics in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193 was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

Industry Part Number

LM193

NS Part Numbers

LM193H/883
LM193J/883

Prime Die

LM193

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Wide supply
  - Voltage range 2.0Vdc to 36Vdc
  - Single or dual supplies ±1.0Vdc to ±18Vdc
- Very low supply current drain (0.4mA) independent of supply voltage
- Low input biasing current 25nA Typ
- Low input offset current ±3nA Typ
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage 250mV at 4mA Typ
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage, V+	36Vdc or ±18Vdc
Differential Input Voltage (Note 6)	36Vdc
Input Voltage	-0.3Vdc to +36Vdc
Input Current (Vin < -0.3 Vdc) (Note 5)	50mA
Maximum Junction Temperature	150 C
Power Dissipation (Note 2, 3)	
METAL CAN	660mW
CERDIP	TBD
Output Short-Circuit to Gnd (Note 4)	Continuous
Operating Temperature Range	-55 C to +125 C
Thermal Resistance	
ThetaJA	
METAL CAN (Still Air)	174 C/W
(500LF/Min Air flow)	99 C/W
CERDIP (Still Air)	146 C/W
(500LF/Min Air flow)	85 C/W
ThetaJC	
METAL CAN	44 C/W
CERDIP	33 C/W
Storage Temperature Range	-65 C to +150 C
Lead Temperature (Soldering, 10 seconds)	+260 C
ESD Tolerance (Note 7)	500V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (Ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: The LM193 must be derated based on a 150 C maximum junction temperature. The low bias dissipation and the ON-OFF characteristic of the outputs keeps the chip dissipation very small (PD≤100mV), provided the output transistors are allowed to saturate.

Note 4: Short circuits from the output to V+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20mA independent of the magnitude of V+.

(Continued)

Note 5: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltagge, which was negative, again returns to a value great than -0.3Vdc.

Note 6: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3Vdc (or 0.3Vdc below the magnitude of the negative power supply, if used).

Note 7: Human body model, 1.5K Ohms in series with 100pF.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V+ = 5V, Vcm = 0

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Icc	Supply Current	V+ = 5V				1	mA	1, 2, 3
		V+ = 36V				2.5	mA	1, 2, 3
Icex	Output Leakage Current	V+ = 30V, Vo=30V, Vin- = 0, Vin+ = 1V			-0.65	0.65	uA	1
					-1	1	uA	2, 3
Isink	Output Sink Current	Vo = 1.5V, Vin- = 1V, Vin+ = 0			6		mA	1
Vsat	Output Saturation Voltage	Iout = 4mA, Vin- = 1V, Vin+ = 0				0.4	V	1
						0.7	V	2, 3
Vio	Input Offset Voltage				-5	5	mV	1
					-9	9	mV	2, 3
		V+ = 30V			-5	5	mV	1
					-9	9	mV	2, 3
		V+ = 30V, Vcm = 28.5V			-5	5	mV	1
		V+ = 30V, Vcm = 28.0V			-9	9	mV	2, 3
+Iib	Input Bias Current				-100	-1	nA	1
					-300	-1	nA	2, 3
-Iib	Input Bias Current				-100	-1	nA	1
					-300	-1	nA	2, 3
Iio	Input offset Current	Rs = 50 Ohms			-25	25	nA	1
					-100	100	nA	2, 3
Vcm	Common Mode Voltage	V+ = 30V	1			28.5	V	1
			1			28	V	2, 3
PSRR	Power Supply Rejection Ratio	V+ = 5V to 30V, Rs = 50 Ohms			60		dB	1
CMRR	Common Mode Rejection Ratio	V+ = 30V, Vcm = 0V to 28.5V, Rs = 50 Ohms			60		dB	1
Vdiff	Differential Input Voltage	V+ = 30V, Vin+ = 36V, Vin- = 0V				500	nA	1, 2, 3
		V+ = 30V, Vin+ = 0V, Vin- = 36V				500	nA	1, 2, 3
Avs	Voltage Gain	V+ = 15V, 1V <= Vout <= 11V, RPULLUP = 15K	2		50		V/mV	4

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: V+ = 5V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tRLH	Response Time	Vod = 5mV	3			5	uS	7
		Vod = 50mV	3			0.8	uS	7
tRHL	Response Time	Vod = 5mV	3			2.5	uS	7
		Vod = 50mV	3			.8	uS	7

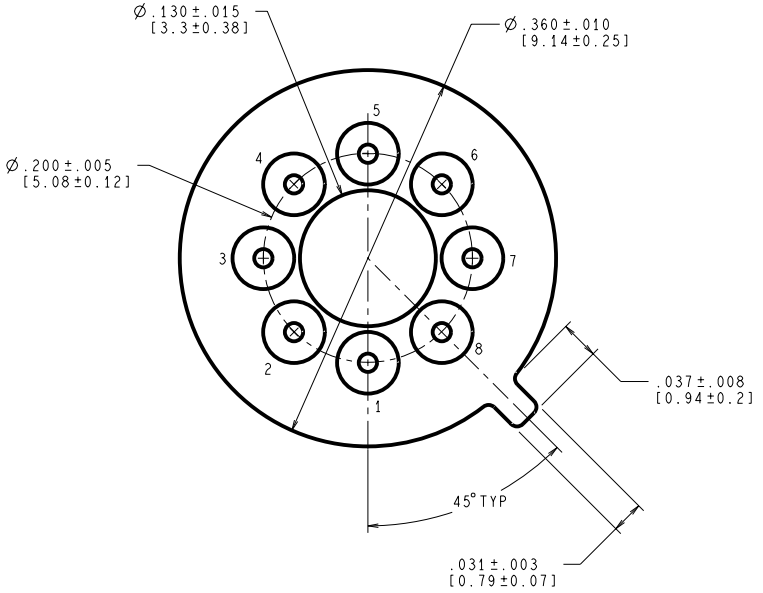
Note 1: Parameter guaranteed by the Vio tests
Note 2: Datalog in K = V/mV
Note 3: Bench tested

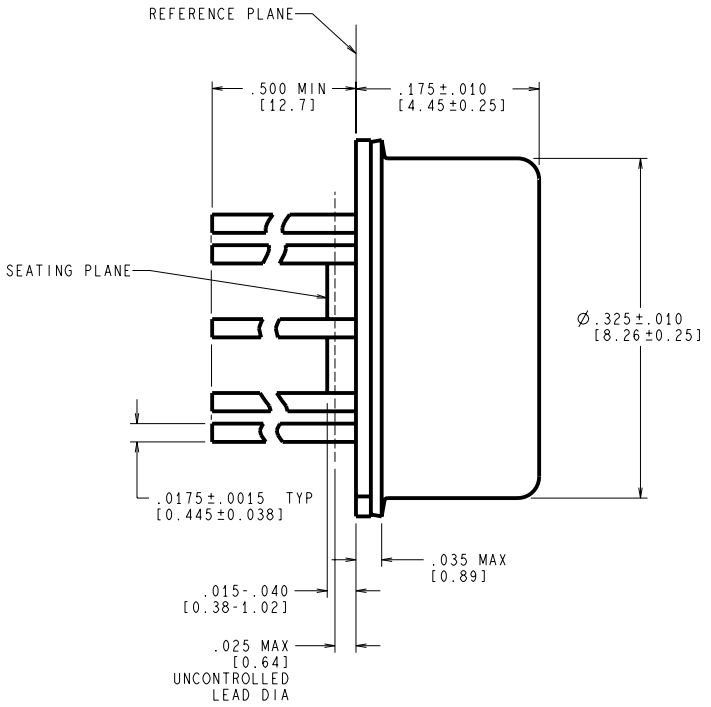
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
06048HRA2	CERDIP (J), 8 LEAD (B/I CKT)
09319HRA2	METAL CAN (H), TO-99, 8 LD, .200 DIA P.C.(B/I CKT)
H08CRF	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000171A	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (PINOUT)
P000172B	CERDIP (J), 8 LEAD (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE & REDRAW PER CURRENT STANDARD; UPDATE MIL/AERO STAMP & TITLE.	11002	06/22/95	MS/





CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEADS TO BE LOCATED WITHIN .007 IN/ 0.18 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
2. STANDARD METAL CAN TYPE: SOLID BASE WITH CERAMIC STANDOFF.
3. APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
4. REFERENCE JEDEC REGISTRATION TO-99, JEDEC PUBLICATION No.95.

APPROVALS	DATE
DRAWN: MARTA SUCHY	06/22/95
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

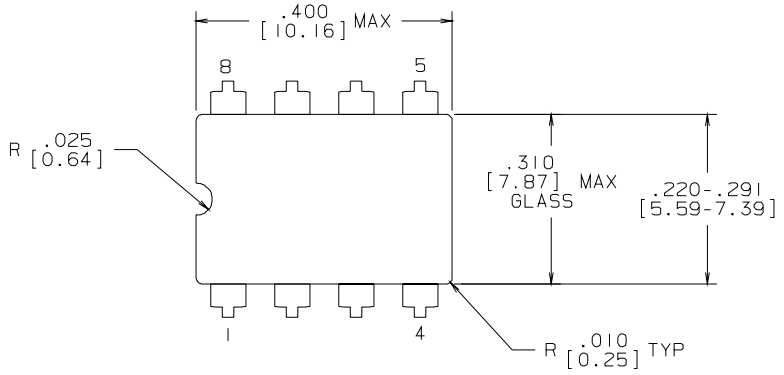
METAL CAN, TO-99, 8 LEAD, .200 DIA P.C.

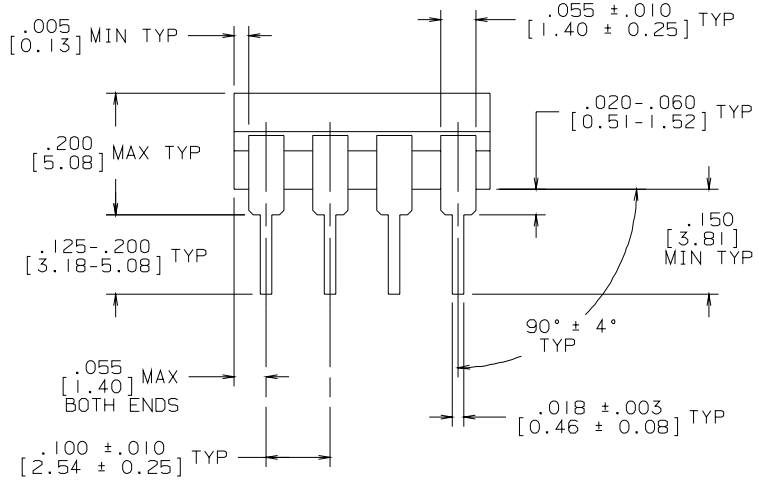
PROJECTION — INCH [MM]

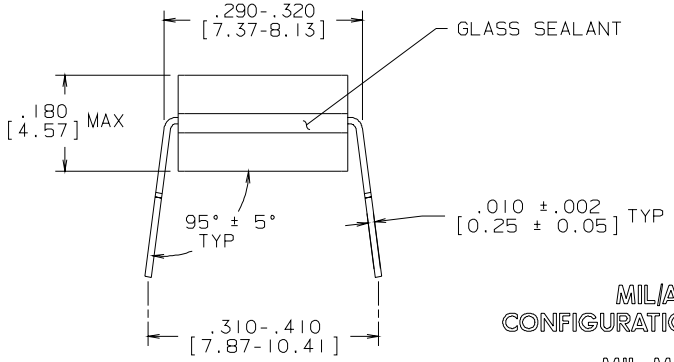
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-H08C	F

DO NOT SCALE DRAWING — SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

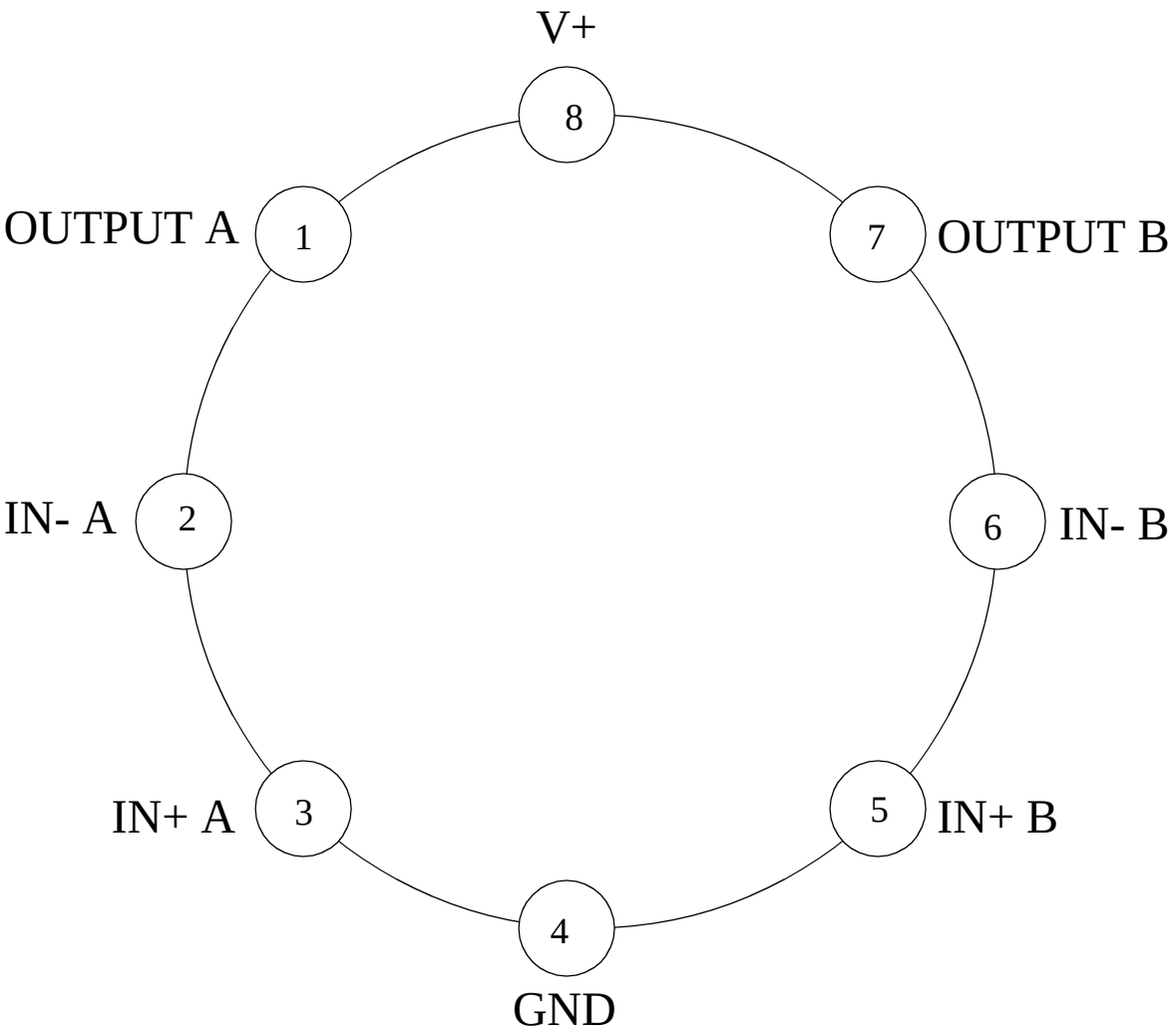
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



LM193AH, LM193H

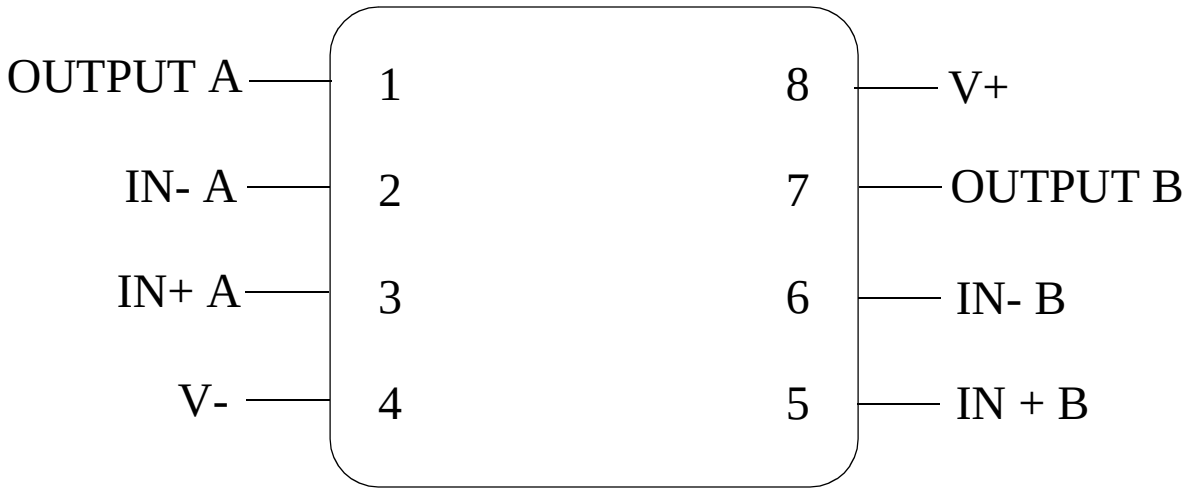
8 - PIN METAL CAN

CONNECTION DIAGRAM

TOP VIEW

P000171A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM193J, LM193AJ

8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000172B

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SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0D1	M0002497	10/05/98	Rose Malone	Updated MDS: MNLM193-X Rev. 0D0 to MNLM193-X Rev. 0D1. Added Burn-In and Pinout graphics for H and J Pkgs.