National Semiconductor

MICROCIRCUIT DATA SHEET

MNLMX2315-X REV 2A1

Original Creation Date: 09/05/97
Last Update Date: 07/30/99
Last Major Revision Date: 05/10/99

PLL FREQUENCY SYNTHESIZER

General Description

The LMX2315 is a high performance frequency synthesizer with integrated prescalers designed for RF operation up to 1.2 GHz. They are fabricated using National's ABiC IV BiCMOS process.

A 64/65 or a 128/129 divide ratio can be selected for the LMX2315 RF synthesizer at input frequencies of up to 1.2 GHz. Using a proprietary digital phase locked loop technique, the LMX2315's linear phase detector characteristics can generate very stable, low noise signals for controlling a local oscillator.

Serial data is transferred into the LMX2315 via a three line MICROWIRE(TM) interface (Data Enable, Clock). Supply voltage can range from 2.7V to 5.5V. The LMX2315 features very low current consumption, typically 6 mA.

The LMX2315, is available in a SOIC 20-pin surface mount ceramic package.

Industry Part Number

LMX2315

NS Part Numbers

LMX2315WG-QML

Prime Die

LMX2315

Controlling Document

SEE FEATURES SECTION:

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+105
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+105
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+105
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+105
11	Switching tests at	-55

Features

- RF operation up to 1.2 GHz.
- 2.7V to 5.5V operation.
- Low current consumption.
- Dual modulus prescaler: 64/65 or 128/129
- Internal balanced, low leakage charge pump.
- Power down feature for sleep mode:
  Icc = 30 uA (typ) at Vcc = 3V
- Small-outline ceramic surface mount SOIC, 0.300" wide.
- CONTROLLING DOCUMENT:
  LMX2315WG-QML 5962-9855001QXA

Applications

- Satellite Communications Payloads
- Navigation Systems
- Military Wireless Communications

(Absolute Maximum Ratings)

(Note 1)

Power Supply Voltage	
Vcc	-0.3V to +6.5V
Vp	-0.3V to +6.5V
Voltage on Any Pin with Gnd = 0V (Vi)	-0.3V to +6.5V
Storage Temperature Range (Ts)	-65 C to +150 C
Power Dissipation (Note 2)	
Pd	1 Watt
Junction Temperature (Note 2)	
Tj	+150 C
Lead Temperature (Tl)	
(Solder, 4 sec.)	+260 C
Thermal Resistance (Note 2)	
ThetaJA	
(Still Air @ 0.5W)	120 C/W
(500LF/Min Air Flow @ 0.5W)	86 C/W
ThetaJC	19 C/W
Package Weight	
(Typical)	600mg
ESD Tolerance (Note 3)	Less Than 500V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guaranteed specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient theraml resistance), and TA (ambient temperature). The maximum allowable power dissiaption at any temperature is Pdmax = (Tjmax -TA) /ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: This device is a high performance RF integrated circuit with an ESD rating <500V and is ESD sensitive. Handling and assembly of this device should be done at ESD workstations.

Recommended Operating Conditions

Power Supply Voltage	
Vcc	2.7V to 5.5V
Vp	Vcc to +5.5V
Operating Temperature (TA)	-55 C to +105 C

Electrical Characteristics

DC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 5.5V, Vp = 5.5V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Icc	Power Supply Current	Vcc = 5.5V				8.5	mA	1, 3
						9.5	mA	2
Icc-pwdn	Power Down Current	Vcc = 2.7V				180	uA	1, 2, 3
		Vcc = 5.5V				350	uA	1, 2, 3
VIH	High Level Input Voltage	Vcc = Vp = 2.7V	1, 4		0.7Vcc		V	1, 2, 3
VIL	Low Level Input Voltage	Vcc = Vp = 2.7V	1, 4			0.3Vcc	V	1, 2, 3
IIH	High Level Input Current (Clock Data)	VIH = Vcc = 5.5V			-1.0	1.0	uA	1, 2, 3
IIL	Low Level Input Current (Clock Data)	VIL = 0, Vcc = 5.5V			-1.0	1.0	uA	1, 2, 3
IIH	Oscillator Input Current	VIH = Vcc = 5.5V				100	uA	1, 2, 3
IIL	Oscillator Input Current	VIL = 0, Vcc = 5.5V			-100		uA	1, 2, 3
IIH	High Level Input Current (LE, FC, PWDN)	VIH = Vcc = 5.5V			-1.0	1.0	uA	1, 2, 3
IIL	Low Level Input Current (LE, FC, PWDN)	VIL = 0, Vcc = 5.5V			-100	1.0	uA	1, 2, 3
IDO-Tri	Charge Pump TRI-STATE Current	0.5V $\leq$ Vdo $\leq$ 3.1V, Vcc = Vp = 3.6V			-2.5	2.5	nA	1, 3
					-25	25	nA	2
IDO-Source	Charge Pump Output Current	Vcc = Vp = 2.7V, Vdo = 1.35V			-3.2		mA	1, 2, 3
		Vcc = Vp = 5.0V, Vdo = 2.5V			-8.0		mA	1, 2, 3
IDO-Sink	Charge Pump Output Current	Vcc = Vp = 2.7V, Vdo = 1.35V				3.2	mA	1, 2, 3
		Vcc = Vp = 5.0V, Vdo = 2.5V				8.0	mA	1, 2, 3
IDO vs VDO	Charge Pump Output Current Magnitude Variation vs Voltage	Vcc = Vp = 5.0V, 0.5V $\leq$ Vdo $\leq$ 4.5V				15	%	1, 2, 3

Electrical Characteristics

DC PARAMETERS:(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 5.5V, Vp = 5.5V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IDOsink vs IDOsource	Charge Pump Output Current Sink vs Source Mismatch	Vcc = Vp = 5.0V, VDO = 2.5V				10	%	1, 2, 3
VOH	High Level Output Voltage	IOH = -1.0mA	2		Vcc -0.8		V	1, 2, 3
VOL	Low Level Output Voltage	IOL = 1.0mA	2			0.4	V	1, 2, 3
VOH (OSCout)	High Level Output Voltage	IOH = -200uA, Vcc = Vp = 3.0V			Vcc -0.8		V	1, 2, 3
VOL (OSCout)	Low Level Output Voltage	IOL = 200uA, Vcc = Vp = 3.0V				0.4	V	1, 2, 3
IOL	Open Drain Output Current (PHP)	VOL = 0.4V	4		1.0		mA	1, 2, 3
IOH	Open	VOH = 5.5V				100	uA	1, 2, 3

Electrical Characteristics

AC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 2.7V, Vp = 2.7V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tCS	Data to Clock Setup Time	See Data Input Timing for Figure 3	4		50		nS	9, 10, 11
tCH	Data to Clock Hold Time	See Data Input Timing for Figure 3	4		10		nS	9, 10, 11
tCWH	Clock Pulse Width High	See Data Input Timing for Figure 3	4		50		nS	9, 10, 11
tCWL	Clock Pulse Width Low	See Data Input Timing for Figure 3	4		50		nS	9, 10, 11
tES	Clock to Enable Setup Time	See Data Input Timing for Figure 3	4		50		nS	9, 10, 11
tEW	Enable Pulse Width	See Data Input Timing for Figure 3	4		50		nS	9, 10, 11
fIN	Maximum Operating Frequency	Divide Ratio 193, fout (diff) = $\pm$322Hz	5		1.2		GHz	9, 10, 11
		Divide Ratio 385, fout (diff) = $\pm$243Hz	5		1.2		GHz	9, 10, 11
Pfin	Input Sensitivity	Vcc = 2.7V	4		-15	+5	dBm	9, 10, 11
		Vcc = 5.5V	4		-9	+6	dBm	9, 10
			4		-7	+6	dBm	11
	Locktime	Freq. Jump 51MHz (f = 864 to 915Mhz), lock time within $\pm$5KHz, Vcc = Vp = 5.0V	3			500	uS	9
	Phase Noise	fop = 900Mhz at 1KHz offset, Vcc = Vp = 5.0V	3			-70	dBc	9
		fop = 900Mhz at 10KHz offset, Vcc = Vp = 5.0V	3			-70	dBc	9
	Spurs	fop = 900Mhz, fref = 200KHz, Vcc = Vp = 5.0V	3			-60	dBc	9

Note 1: Except fIN and OSCin.
Note 2: Except OSCout.
Note 3: QMLV/MLS only
Note 4: Used as Setup Conditions for Functional Testing.
Note 5: The limits shown are the maximum operating frequency. It is tested by dividing the 1.2GHz by the divide ratio in the condition column and measuring the difference between output frequency pin and the expected output frequency.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
06346HRA3	CERPACK, 20 LEAD GULL WING (B/I CKT)
AN00035A	(LMX2305/15/25) TIMING DIAGRAM
P000390A	CERAMIC SOIC (WG), 20 LEAD (PINOUT)
WG20ARB	CERPACK, 20 LEAD GULL WING (P/P DWG)

See attached graphics following this page.

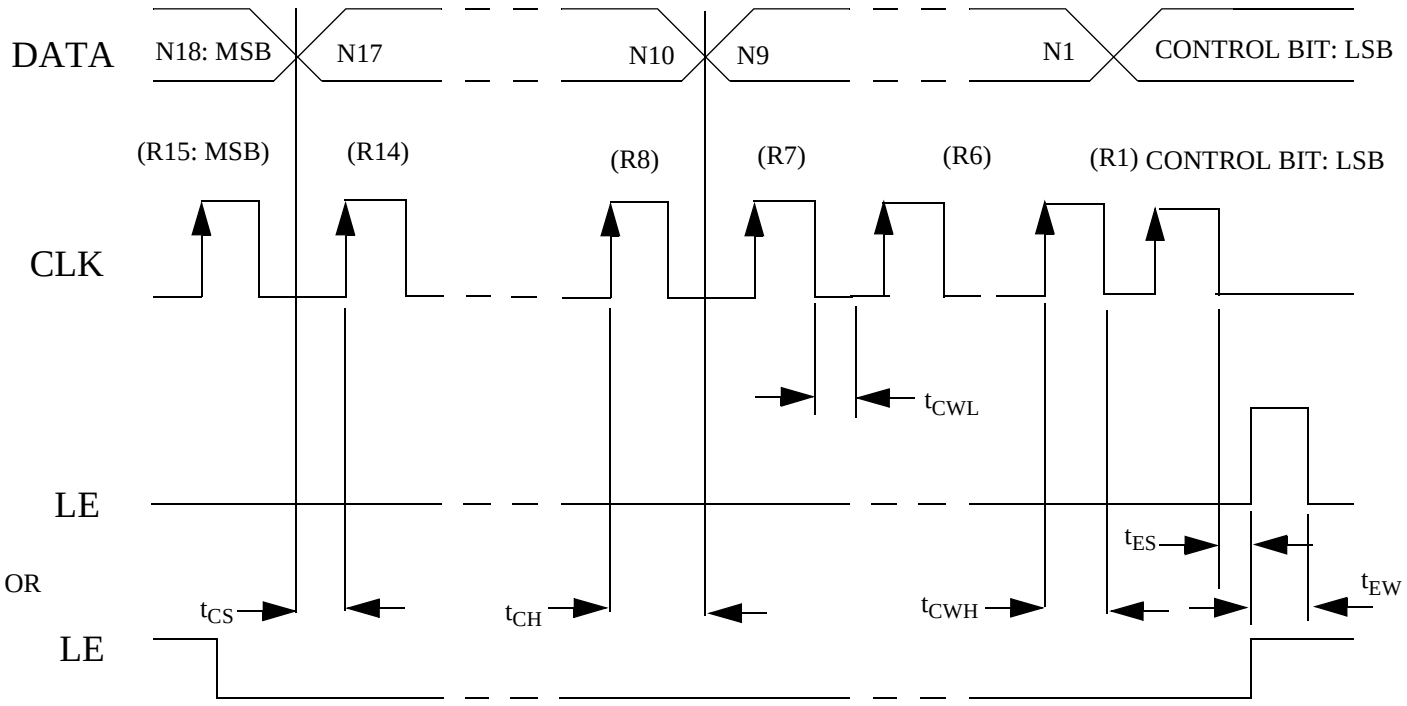

figure 3

AN00035A

Notes:
1. Parenthesis data indicates programmable reference divider data.
2. Data shifted into register in clock rising edges.
3. Data is shifted in MSB first.

National Semiconductor™
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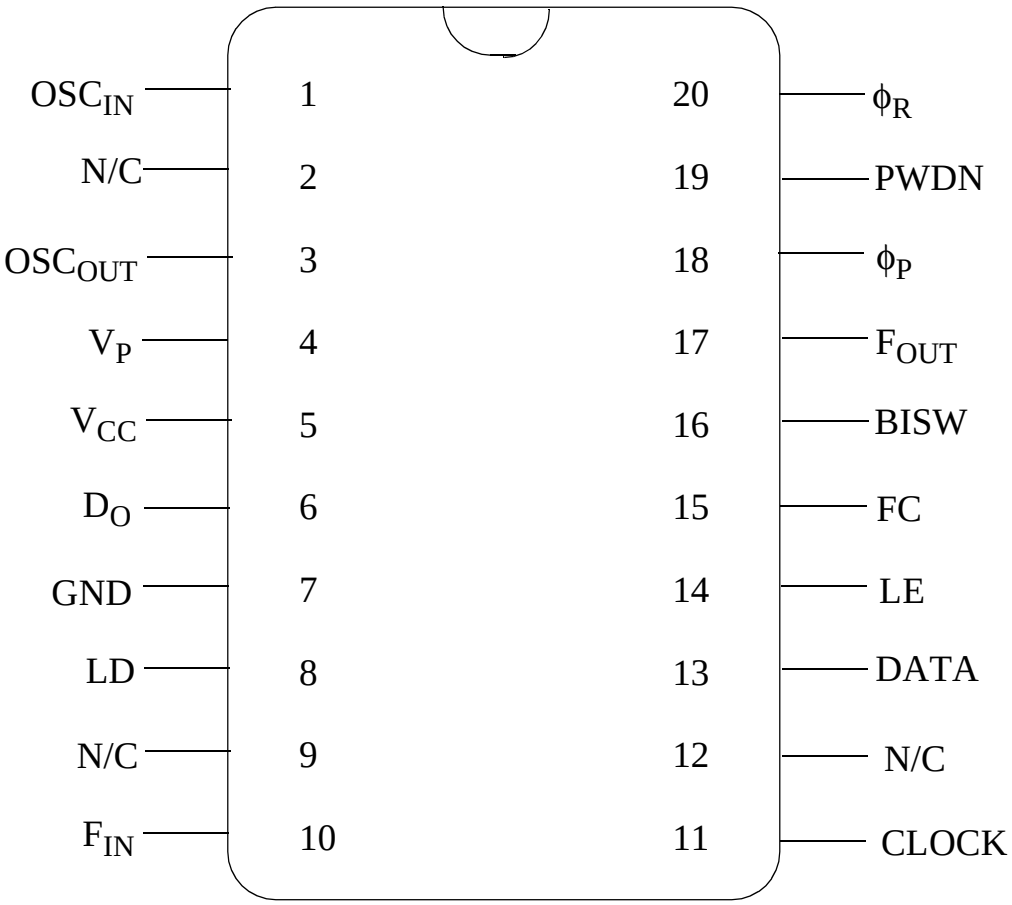
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LMX2315WG
20 - LEAD CERAMIC SOIC
CONNECTION DIAGRAM
TOP VIEW
P000390A

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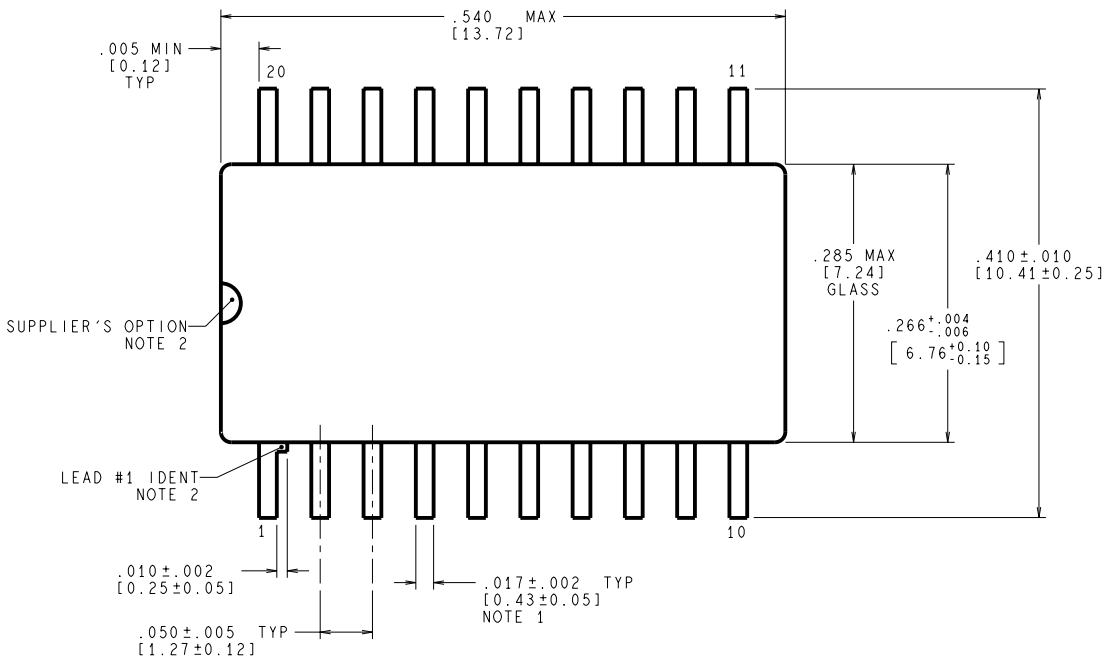
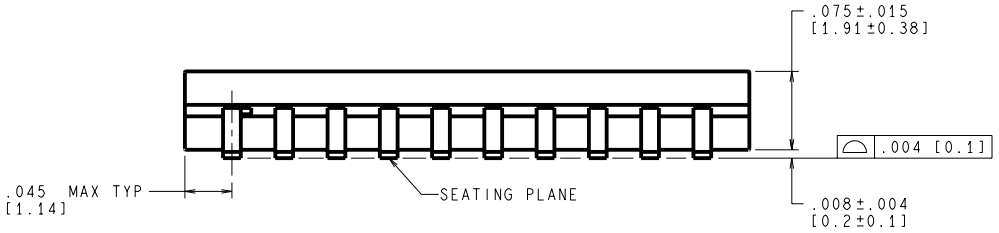
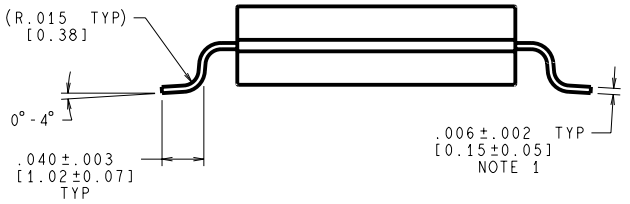
REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11842	10/13/1997	TL/KH
B	DIM .410 WAS .391; UPDATE NOTE 3.	12013	06/15/1998	MS/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF JUNE 1998.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN T LEQUANG	10/13/1997
DFTG. CHK.	
ENGR. CHK.	

PROJECTION INCH [MM]

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK,
20 LEAD,
GULL WING

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG20A	B

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0002486	03/16/99	Rose Malone	Initial Release of MDS:
1A1	M0003258	07/30/99	Rose Malone	Update MDS: MNLMX2315-X, Rev. 0A0 to MNLMX2315-X, Rev. 1A1. Moved Reference to Controlling Document to Features Section. Added Power Dissipation and Junction Temperature reference to Absolute Section. Changed Electrical Conditions for VIH, VIL, IDO-Tri, IDO vs VDO, IDOsink vs IDOsource, VOH(OSCout), VOL(OSCout) and IOL. Added NOTE 4 to VIH, VIL, IOL, fIN and Pfin. Updated B/I graphic.
2A1	M0003448	07/30/99	Rose Malone	Update MDS: MNLMX2315-X, Rev. 1A1 to MNLMX2315-X, Rev. 2A1. Deleted Vosc Electrical parameter, Corrected typo in parameter field for IIH from High Level Input Current (LE, PC, PWDN) to High Level Input Current (LE, FC, PWDN) and IIL from Low Level Input Current (LE, PC, PWDN) to Low Level Input Current (LE, FC, PWDN). Added Condition to fIN Parameter, NOTE 4 and NOTE 5.