

MRLM108A-X-RH REV 1A0

Original Creation Date: 12/21/98

Last Update Date: 04/16/99

Last Major Revision Date: 04/06/99

OPERATIONAL AMPLIFIERS (SINGLE) GUARANTEED TO 100K RAD(Si) TESTED TO MIL-STD-883, METHOD 1019.5

General Description

The LM108A is a precision operational amplifier having specifications a factor of ten better than FET amplifiers over a -55 C to +125 C temperature range.

The device operates with supply voltages from $\pm 2V$ to $\pm 20V$ and has sufficient supply rejection to use unregulated supplies. Although the circuit is interchangeable with and uses the same compensation as the LM101A, an alternate compensation scheme can be used to make it particularly insensitive to power supply noise and to make supply bypass capacitors unnecessary.

The low current error of the LM108A makes possible many designs that are not practical with conventional amplifiers. In fact, it operates from 10M Ohms source resistances, introducing less error than devices like the 709 with 10K Ohms sources. Integrators with drifts less than 500 $\mu V/sec$ and analog time delays in excess of one hour can be made using capacitors no larger than 1 μF .

Industry Part Number

LM108A

Prime Die

LM108A

Controlling Document

SEE FEATURES SECTION

NS Part Numbers

 LM108AHRQML
 LM108AHRQMLV
 LM108AJ-8RQML
 LM108AJ-8RQMLV
 LM108AJRQML
 LM108AJRQMLV
 LM108AWGRQML
 LM108AWGRQMLV
 LM108AWRQML
 LM108AWRQMLV

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

CONTROLLING DOCUMENT:

LM108AHRQML	5962R9863702QGA
LM108AHRQMLV	5962R9863702VGA
LM108AJ-8RQML	5962R9863702QPA
LM108AJ-8RQMLV	5962R9863702VPA
LM108AJRQML	5962R9863702QCA
LM108AJRQMLV	5962R9863702VCA
LM108AWGRQML	5962R9863702QZA
LM108AWGRQMLV	5962R9863702VZA
LM108AWRQML	5962R9863702QHA
LM108AWRQMLV	5962R9863702VHA

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage

 $\pm 22\text{V}$

Power Dissipation

(Note 2)

METAL CAN

330mW @ +125 C

CERDIP, 14 Lead

400mW @ +125 C

CERDIP, 8 Lead

400mW @ +125 C

CERPACK, 10 Lead

330mW @ +125 C

CERAMIC SOIC

330mW @ +125 C

Differential Input Current

(Note 3)

 $\pm 10\text{mA}$

Differential Input Voltage

(Note 5)

 $\pm 30\text{V}$

Input Voltage

(Note 4)

 $\pm 20\text{V}$

Output Short-Circuit Duration

Continuous

Operating Temperature Range

-55 C to +125 C

Storage Temperature Range

-65 C to +150 C

Thermal Resistance

ThetaJA

METAL CAN

(Still Air)

150 C/W

(500LF/Min Air flow)

86 C/W

CERDIP, 14 Lead

(Still Air)

94 C/W

(500LF/Min Air flow)

55 C/W

CERDIP, 8 Lead

(Still Air)

120 C/W

(500LF/Min Air flow)

68 C/W

CERPACK, 10 Lead

(Still Air)

225 C/W

(500LF/Min Air flow)

142 C/W

CERAMIC SOIC

(Still Air)

225 C/W

(500LF/Min Air flow)

142 C/W

ThetaJC

METAL CAN

38 C/W

CERDIP, 14 Lead

13 C/W

CERDIP, 8 Lead

17 C/W

CERPACK, 10 Lead

21 C/W

CERAMIC SOIC

21 C/W

Package Weight

(Typical)

METAL CAN

990mg

CERDIP, 14 Lead

2180mg

CERDIP, 8 Lead

1090mg

CERPACK, 10 Lead

225mg

CERAMIC SOIC

210mg

Maximum Junction Temperature

175 C

Soldering Information

(Soldering, 10 seconds)

300 C

ESD Tolerance

(Note 6)

2000V

- Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{jmax} (maximum junction temperature), Θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{dmax} = (T_{jmax} - T_A) / \Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
- Note 3: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.
- Note 4: For supply voltages less than $\pm 20V$, the absolute maximum input voltage is equal to the supply voltage.
- Note 5: This rating is $\pm 1.0V$ unless resistances of 2K Ohms or greater are inserted in series with the inputs to limit current in the input shunt diodes to the maximum allowable value.
- Note 6: Human body model, 1.5K Ohms in series with 100pF.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $\pm V_{CC} = \pm 20V$, $V_{CM} = 0V$, $R_S = 50\ \Omega$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	$+V_{CC} = 35V$, $-V_{CC} = -5V$, $V_{CM} = -15V$			-0.5	0.5	mV	1
					-1	1	mV	2, 3
		$+V_{CC} = 5V$, $-V_{CC} = -35V$, $V_{CM} = 15V$			-0.5	0.5	mV	1
					-1	1	mV	2, 3
					-0.5	0.5	mV	1
					-1	1	mV	2, 3
		$+V_{CC} = +5V$, $-V_{CC} = -5V$			-0.5	0.5	mV	1
					-1	1	mV	2, 3
Delta Vio/Delta T	Temperature Coefficient of Input Offset Voltage	$25\ C \leq T_A \leq +125\ C$	1		-5	5	$\mu V/C$	2
		$25\ C \leq T_A \leq -55\ C$	1		-5	5	$\mu V/C$	3
Iio	Input Offset Current	$+V_{CC} = 35V$, $-V_{CC} = -5V$, $V_{CM} = -15V$			-0.2	0.2	nA	1
					-0.4	0.4	nA	2, 3
		$+V_{CC} = 5V$, $-V_{CC} = -35V$, $V_{CM} = 15V$			-0.2	0.2	nA	1
					-0.4	0.4	nA	2, 3
					-0.2	0.2	nA	1
					-0.4	0.4	nA	2, 3
		$+V_{CC} = +5V$, $-V_{CC} = -5V$			-0.2	0.2	nA	1
					-0.4	0.4	nA	2, 3
Delta Iio/Delta T	Temperature Coefficient of Input Offset Current	$25\ C \leq T_A \leq +125\ C$	1		-2.5	2.5	pA/C	2
		$25\ C \leq T_A \leq -55\ C$	1		-2.5	2.5	pA/C	3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $\pm V_{CC} = \pm 20V$, $V_{CM} = 0V$, $R_S = 50\ \Omega$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
+Iib	Input Bias Current	+Vcc = 35V, -Vcc = -5V, Vcm = -15V			-0.1	2	nA	1
					-1	2	nA	2
					-0.1	3	nA	3
		+Vcc = 5V, -Vcc = -35V, Vcm = 15V			-0.1	2	nA	1
					-1	2	nA	2
					-0.1	3	nA	3
					-0.1	2	nA	1
					-1	2	nA	2
					-0.1	3	nA	3
		+Vcc = +5V, -Vcc = -5V			-0.1	2	nA	1
					-1	2	nA	2
					-0.1	3	nA	3
-Iib	Input Bias Current	+Vcc = 35V, -Vcc = -5V, Vcm = -15V			-0.1	2	nA	1
					-1	2	nA	2
					-0.1	3	nA	3
		+Vcc = 5V, -Vcc = -35V, Vcm = 15V			-0.1	2	nA	1
					-1	2	nA	2
					-0.1	3	nA	3
					-0.1	2	nA	1
					-1	2	nA	2
					-0.1	3	nA	3
		+Vcc = +5V, -Vcc = -5V			-0.1	2	nA	1
					-1	2	nA	2
					-0.1	3	nA	3
+PSRR	Power Supply Rejection Ratio	+Vcc = 10V, -Vcc = -20V			-16	16	uV/V	1, 2, 3
-PSRR	Power Supply Rejection Ratio	+Vcc = 20V, -Vcc = -10V			-16	16	uV/V	1, 2, 3
CMRR	Common Mode Rejection Ratio	Vcm = $\pm 15V$			96		dB	1, 2, 3
Ios+	Short Circuit Current	+Vcc = +15V, -Vcc = -15V, $t \leq 25mS$			-15		mA	1, 2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $\pm V_{CC} = \pm 20V$, $V_{CM} = 0V$, $R_S = 50\ \Omega$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ios-	Short Circuit Current	$+V_{CC} = +15V$, $-V_{CC} = -15V$, $t \leq 25mS$				15	mA	1, 2, 3
Icc	Power Supply Current	$+V_{CC} = +15V$, $-V_{CC} = -15V$				0.6	mA	1, 2
						0.8	mA	3

AC/DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $\pm V_{CC} = \pm 20V$, $V_{CM} = 0V$, $R_S = 50\ \Omega$

AC: $\pm V_{CC} = \pm 20V$, $V_{CM} = 0V$, $R_S = 50\ \Omega$

+Vop	Output Voltage Swing	$R_L = 10K\ \Omega$			16		V	4, 5, 6
-Vop	Output Voltage Swing	$R_L = 10K\ \Omega$				-16	V	4, 5, 6
Avs+	Open Loop Voltage Gain	$R_L = 10K\ \Omega$, $V_{out} = +15V$	3		80		V/mV	4
			3		40		V/mV	5, 6
Avs-	Open Loop Voltage Gain	$R_L = 10K\ \Omega$, $V_{out} = -15V$	3		80		V/mV	4
			3		40		V/mV	5, 6
Avs	Open Loop Voltage Gain	$\pm V_{CC} = \pm 5V$, $R_L = 10K\ \Omega$, $V_{out} = \pm 2V$	3		20		V/mV	4, 5, 6
TR(tr)	Transient Response Rise Time	$R_L = 10K\ \Omega$, $C_L = 100pF$, $f < 1KHz$, $V_{in} = +50mV$	4			1000	nS	9, 10, 11
TR(os)	Transient Response Overshoot	$R_L = 10K\ \Omega$, $C_L = 100pF$, $f < 1KHz$, $V_{in} = +50mV$	4			50	%	9, 10, 11
Sr(+)	Slew Rate	$A_v = 1$, $V_{in} = -5V$ to $+5V$			0.05		V/ μS	9, 10, 11
Sr(-)	Slew Rate	$A_v = 1$, $V_{in} = +5V$ to $-5V$			0.05		V/ μS	9, 10, 11
NI(BB)	Noise Broadband	$BW = 10Hz$ to $5KHz$, $R_S = 0\ \Omega$	2			15	μV_{rms}	9
NI(PC)	Noise Popcorn	$BW = 10Hz$ to $5KHz$, $R_S = 100K\ \Omega$	2			40	μV_{pk}	9

Electrical Characteristics

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $\pm V_{CC} = \pm 20V$, $V_{CM} = 0V$, $R_S = 50\ \Omega$ Ohms. "Delta calculations performed on JAN S and QMLV devices at group B, subgroup 5 only".

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage				-0.25	0.25	mV	1
+Iib	Input Bias Current				-0.5	0.5	nA	1
-Iib	Input Bias Current				-0.5	0.5	nA	1

DC/AC PARAMETERS: POST RADIATION LIMITS +25 C (SEE NOTE 5)

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $\pm V_{CC} = \pm 20V$, $V_{CM} = 0V$, $R_S = 50\ \Omega$ Ohms.

+Iib	Input Bias Current	+Vcc = 35V, -Vcc = -5V, Vcm = -15V	5			5.0	nA	1
		+Vcc = 5V, -Vcc = -35V, Vcm = -15V	5			5.0	nA	1
			5			5.0	nA	1
		+Vcc = +5V, -Vcc = -5V	5			5.0	nA	1
-Iib	Input Bias Current	+Vcc = 35V, -Vcc = -5V, Vcm = -15V	5			5.0	nA	1
		+Vcc = 5V, -Vcc = -35V, Vcm = -15V	5			5.0	nA	1
			5			5.0	nA	1
		+Vcc = +5V, -Vcc = -5V	5			5.0	nA	1
Iio	Input Offset Current	+Vcc = 35V, -Vcc = -5V, Vcm = -15V	5			0.5	nA	1
		+Vcc = 5V, -Vcc = -35V, Vcm = -15V	5			0.5	nA	1
			5			0.5	nA	1
		+Vcc = +5V, -Vcc = -5V	5			0.5	nA	1

Note 1: Calculated parameter.

Note 2: Test on either A360, J273 AC or bench test.

Note 3: Datalog reading in K = V/mV.

Note 4: Bench test.

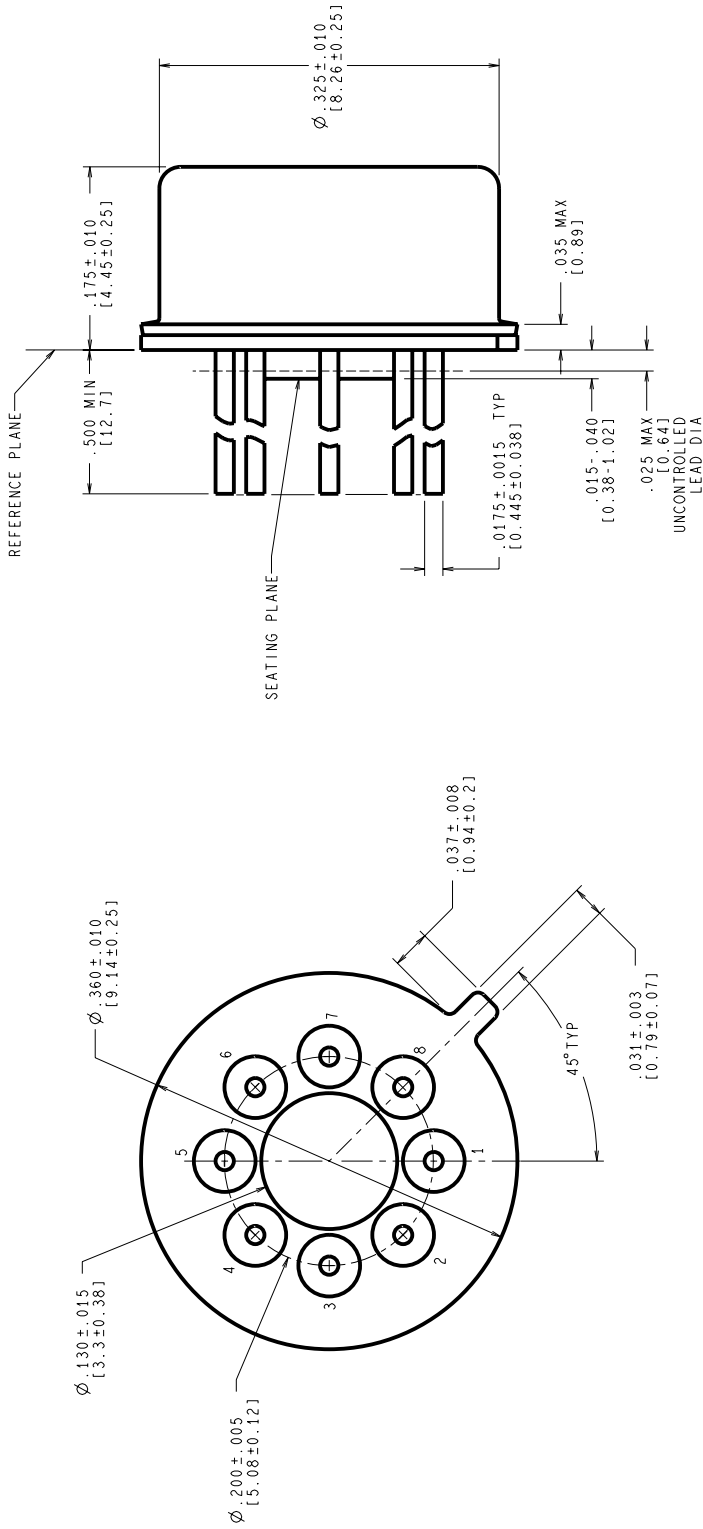
Note 5: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, Method 1019.5.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
H08CRF	METAL CAN (H), T0-99, 8LD, .200 DIA P.C. (P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000253A	CERAMIC SOIC (WG), 10 LEAD (PINOUT)
P000310A	METAL CAN (H), T0-99, 8LD, .200 DIA P.C. (PINOUT)
P000311A	CERDIP (J), 14 LEAD (PINOUT)
P000312A	CERDIP (J), 8 LEAD (PINOUT)
P000431A	CERPACK (W), 10 LEAD (PINOUT)
W10ARG	CERPACK (W), 10 LEAD (P/P DWG)
WG10ARC	CERAMIC SOIC (WG), 10 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
F	REVISE & REDRAW PER CURRENT STANDARD; UPDATE MIL/AERO STAMP & TITLE.	11002	06/22/95
			MS/



CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

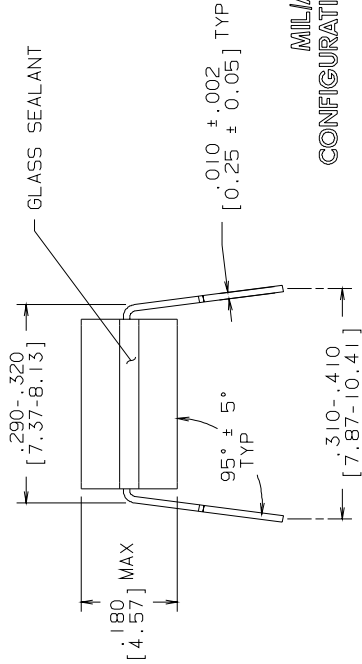
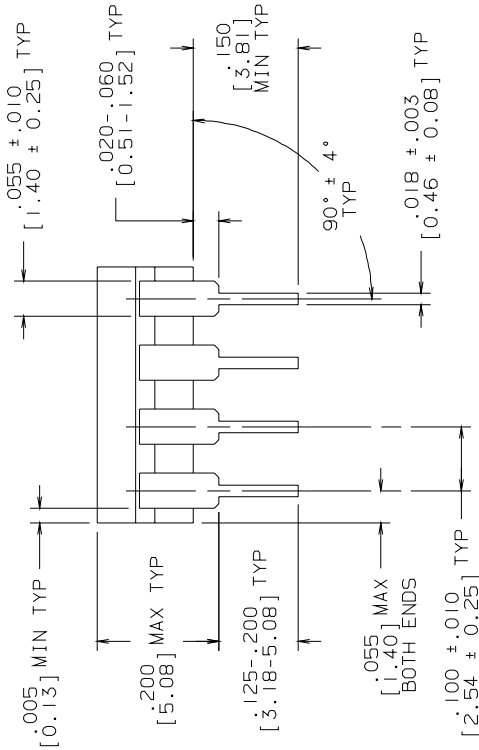
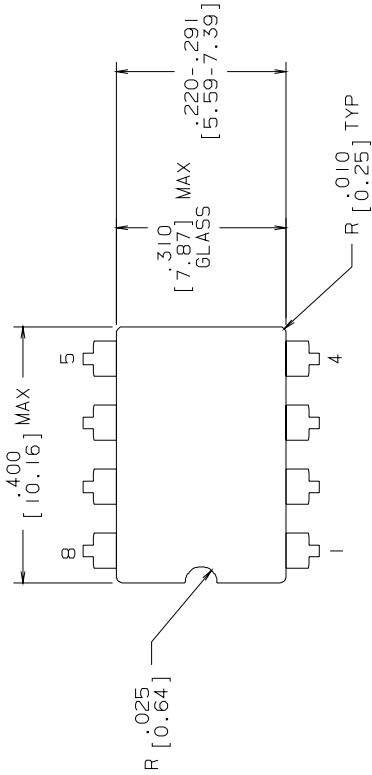
MIL-I-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

- LEADS TO BE LOCATED WITHIN .007 IN/ 0.18 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
- STANDARD METAL CAN TYPE: SOLID BASE WITH CERAMIC STANDOFF.
- APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
- REFERENCE JEDEC REGISTRATION TO-99, JEDEC PUBLICATION No. 95.

APPROVALS		DATE	National Semiconductor	
DESIGN	MARIA SUCHY	06/22/95	2000 Semiconductor dr., Santa Clara, CA 95052-8000	
DATE	CHK.			
DATE	CHK.			
PROJECTION				
SCALE	N/A	SIZE	C	DRAWING NUMBER
REV	F	REV	MKT-H08C	REV
DO NOT SCALE DRAWING		SHEET 1 of 1		

R E V I S I O N S				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/

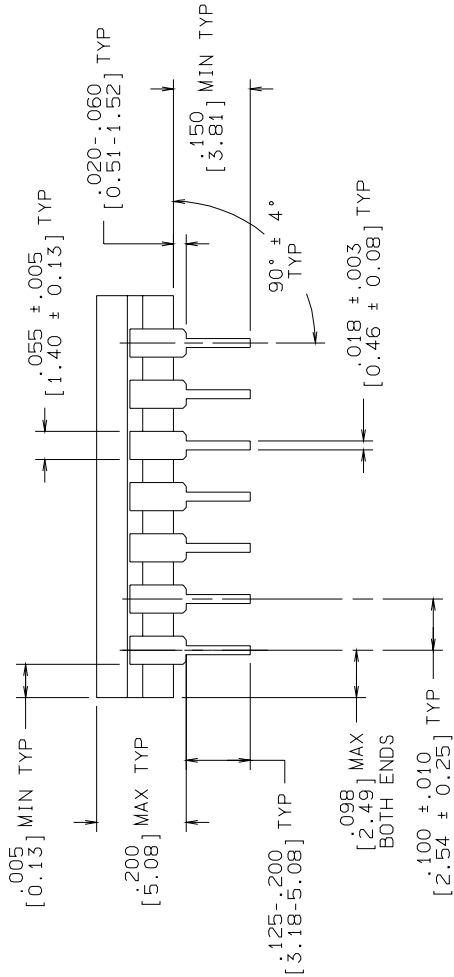
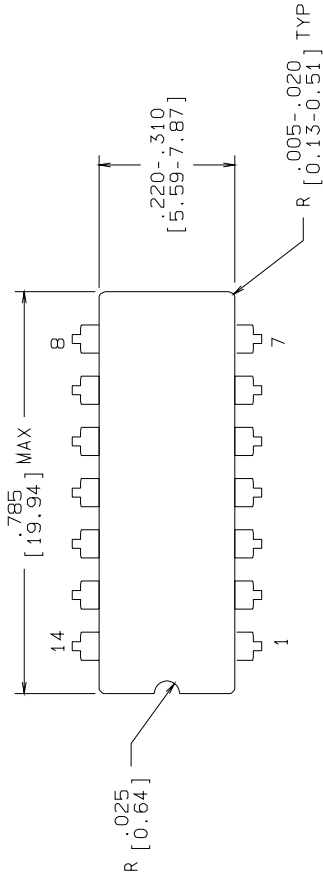


MIL-AERO
CONFIGURATION CONTROL
MIL-M-38510
CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH				
APPROVALS	DATE	NATIONAL SEMICONDUCTOR CORPORATION		
DRAWN LEQUANG	09/21/93	2900 Semiconductor Drive, Santa Clara, CA 95052-8090		
DFTG. CHK.		CERDIP (J) ,		
ENGR. CHK.		8 LEAD		
APPROVAL				
 PROJECTION 1 INCH [25.4]	SCALE	SIZE	DRAWING NUMBER	REV
	N/A	B	MKT-J08A	L
DO NOT SCALE DRAWING		SHEET	1	OF 1

- NOTES: UNLESS OTHERWISE SPECIFIED
1. LEAD FINISH TO BE 200 MICRONS / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
 2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

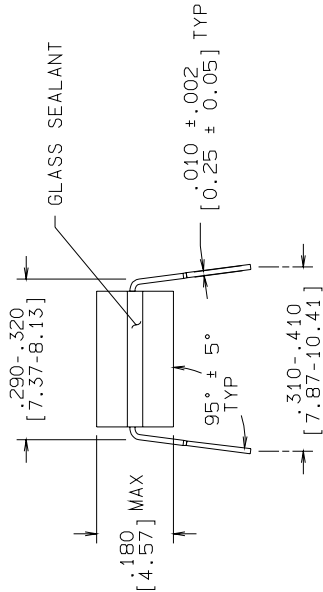
R E V I S I O N S				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/



CONTROLLING DIMENSION: INCH

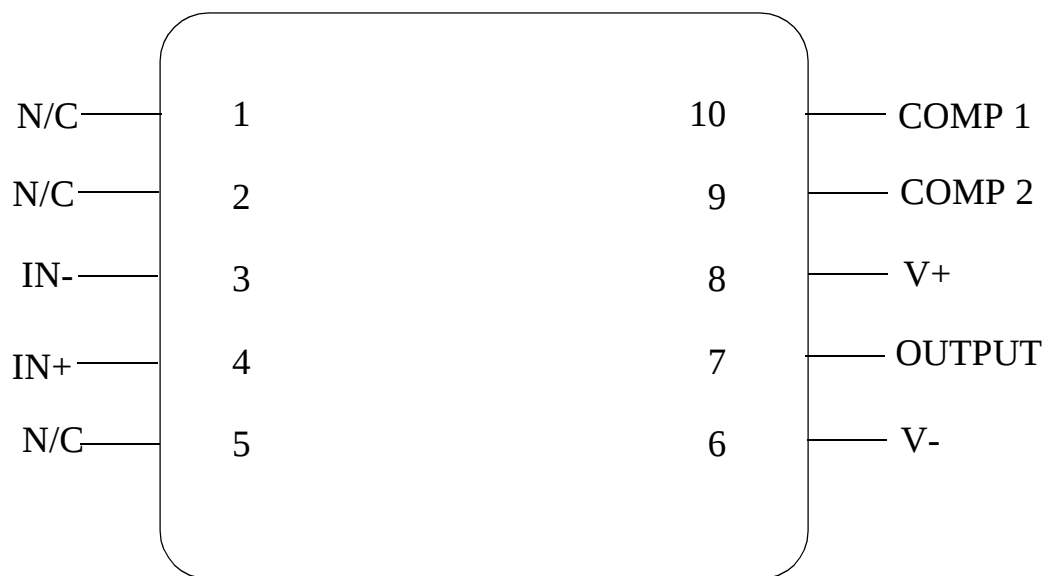
NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROMETERS / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.



MIL/AERO MIL-M-38510
CONFIGURATION CONTROL CONFIGURATION CONTROL

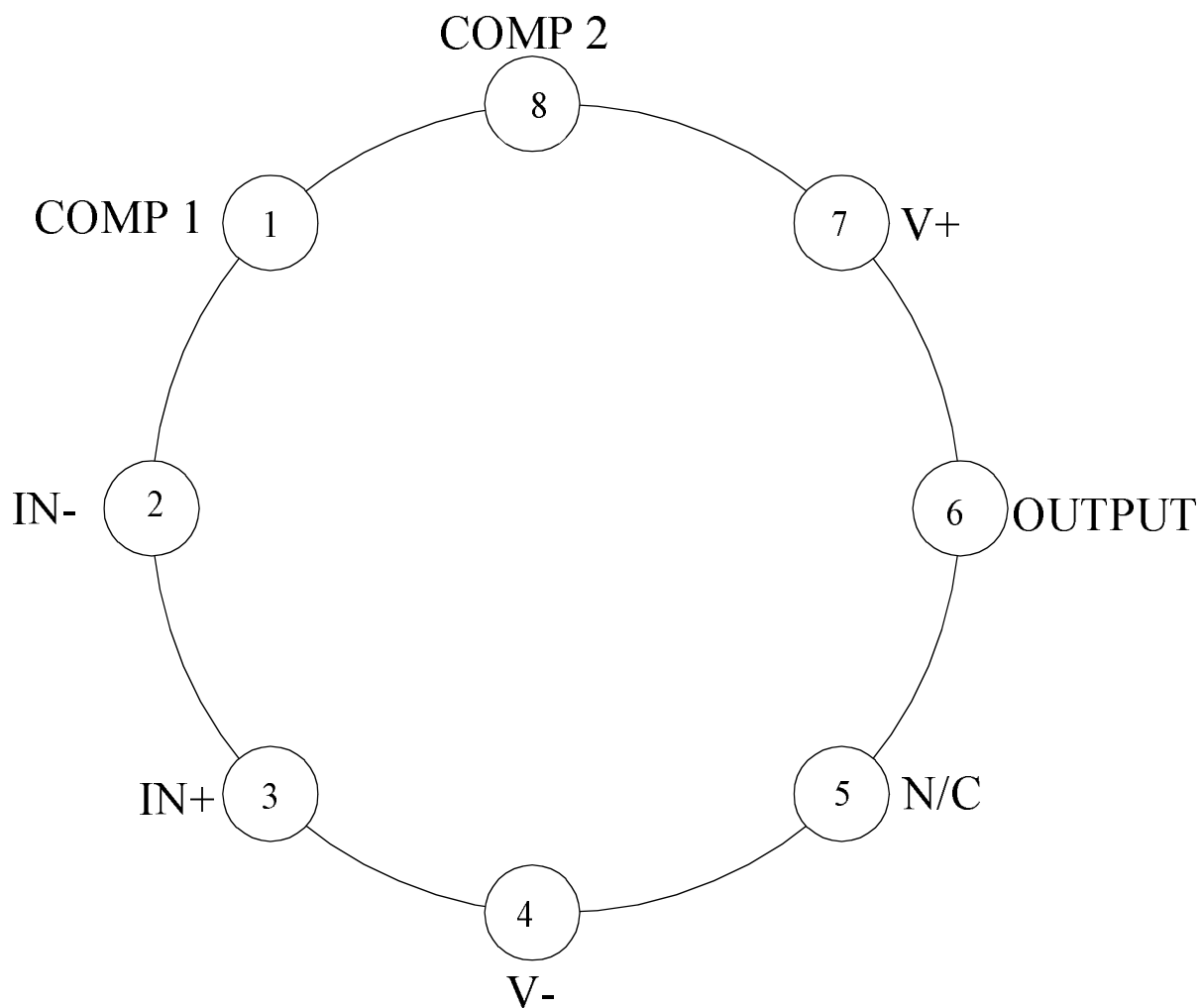
APPROVALS	DATE	NATIONAL SEMICONDUCTOR CORPORATION		
DRAWN LEQUANG	09/15/93	2900 Semiconductor Drive, Santa Clara, CA 95052-8090		
DFTG. CHK.				
ENGR. CHK.				
APPROVAL		CERDIP (J) , 14 LEAD,		
 PROJECTION 1 INCH [25.4]	SCALE	SIZE	DRAWING NUMBER	REV
	N/A	B	MKT-J14A	H
DO NOT SCALE DRAWING		SHEET	1	OF 1



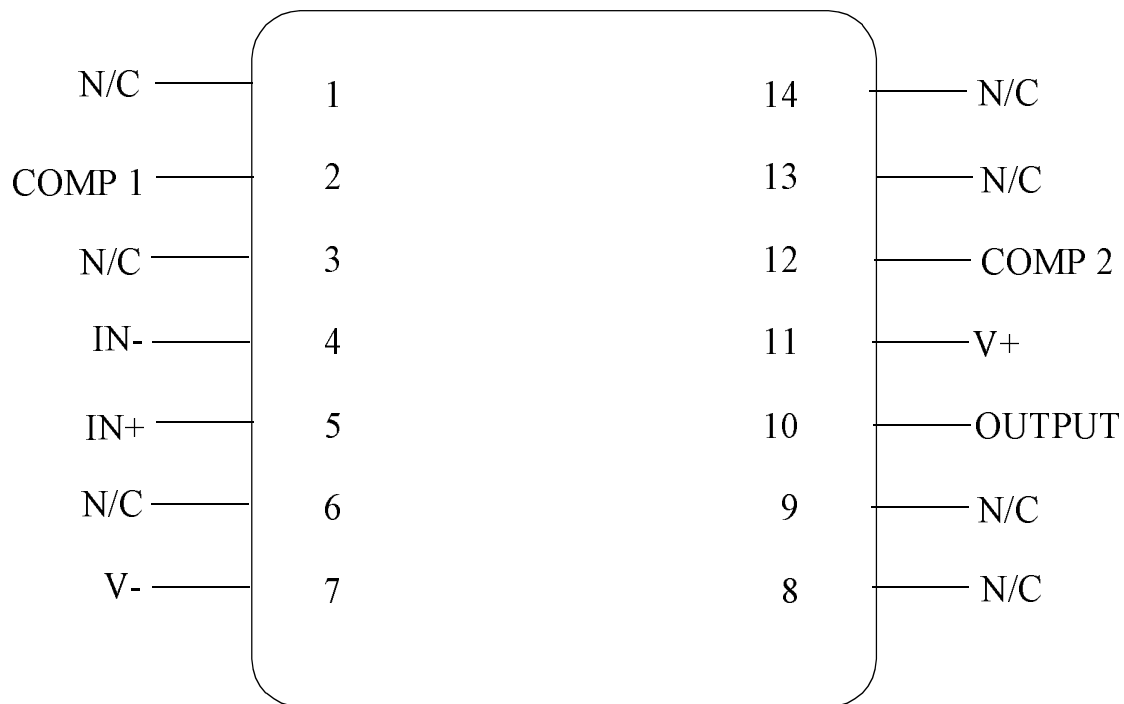
LM108AWG
10 - LEAD CERAMIC SOIC
CONNECTION DIAGRAM
TOP VIEW
P000253A



National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM108AH, LM108H
8 - PIN METAL CAN
CONNECTION DIAGRAM
TOP VIEW
P000310A



LM108AJ, LM108J
 14 - LEAD DIP
 CONNECTION DIAGRAM
 TOP VIEW
 P000311A



National Semiconductor™
 MIL/AEROSPACE OPERATIONS
 2900 SEMICONDUCTOR DRIVE
 SANTA CLARA, CA 95050



LM108AJ-8, LM108J-8

8 - LEAD DIP

CONNECTION DIAGRAM

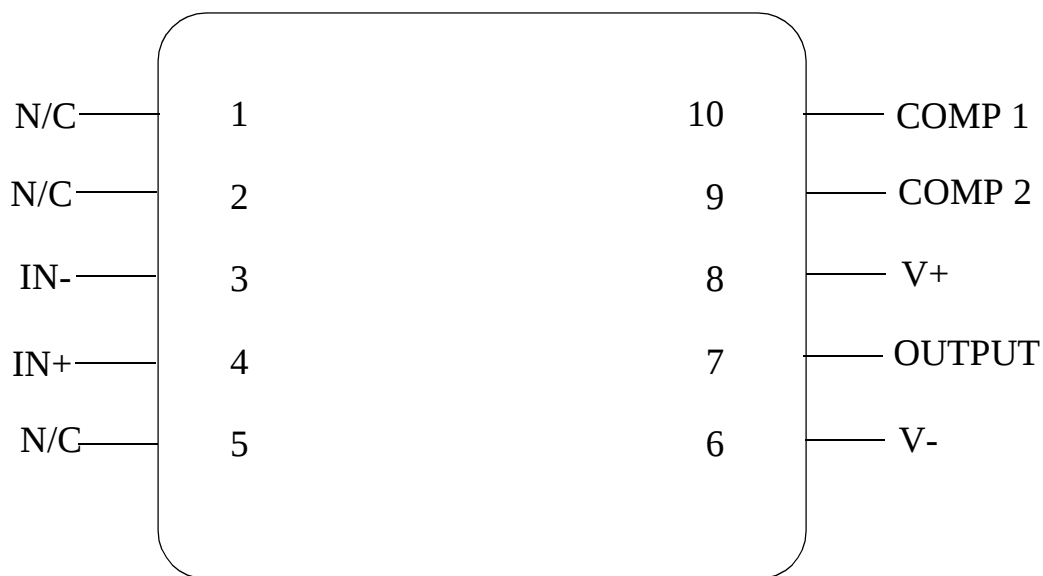
TOP VIEW

P000312A



National Semiconductor™

MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



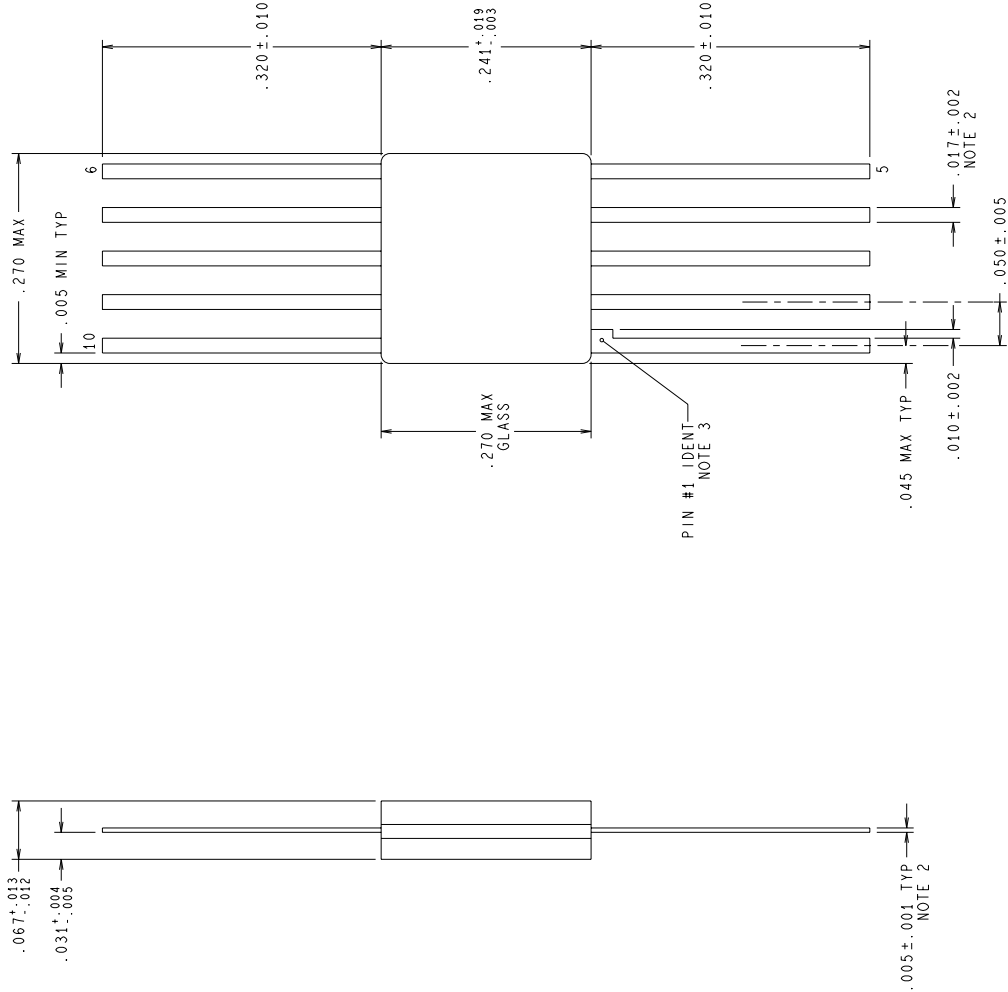
LM108AW
10 - LEAD CERPACK
CONNECTION DIAGRAM
TOP VIEW
P000431A



National Semiconductor™

MIL/AEROSPACE OPERATIONS
 2900 SEMICONDUCTOR DRIVE
 SANTA CLARA, CA 95050

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
F	REVISE AND REDRAW PER NEW STANDARD.	10510	07/28/94
G	.017±.002 WAS .017±.020.	10654	10/21/94



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
a) A NOTCH OR OTHER MARK WITHIN THIS AREA
b) A TAB ON LEAD 1, EITHER SIDE
4. REFERENCE JEDEC REGISTRATION M0-003, VARIATION AG, DATED 06/01/76.

MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

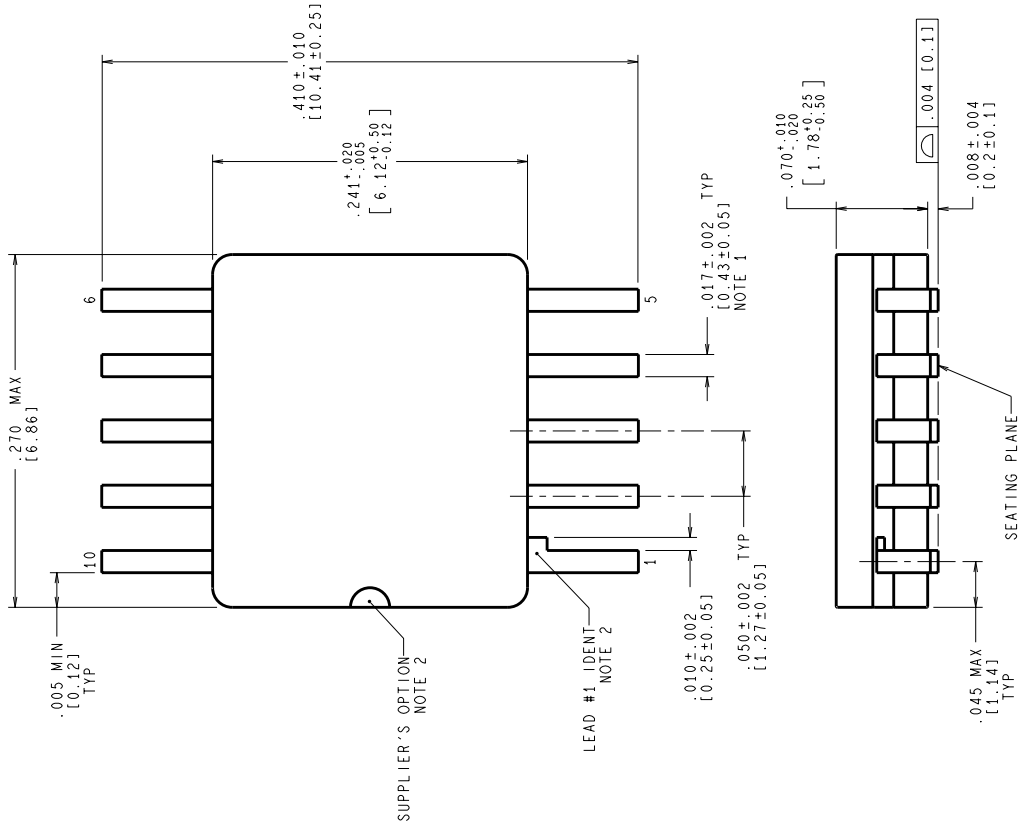
APPROVALS		DATE	
DRN	<i>D. F. Grady</i>		07/28/94
DFTG. CHK.			
ENGR. CHK.			
PROJECTION			
SCALE	N/A	SIZE	C
DRAWING NUMBER	MKT-W10A		
REV	G		
DO NOT SCALE DRAWING		SHEET 1 of 1	

 *National Semiconductor*
2000 Semiconductor dr., Santa Clara, CA 95052-8090

CERPACK, 10 LEAD

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
A	RELEASE TO DOCUMENT CONTROL	11374	02/29/1996
B	LD PITCH TOL WAS $\pm .005$; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R .006 $\pm .002$ DIM .040 $\pm .003$ WAS .037 $\pm .003$	11441	04/19/1996
C	R .015(0.38) WAS R .006(0.15)	11838	10/08/1997

BY/APP'D	DATE	MS/KH
MS/KH	02/29/1996	
MS/KH	04/19/1996	
TL/	10/08/1997	



CONTROLLING DIMENSION IS INCH
VALUES IN | | ARE MILLIMETERS

MIL-PRF-38535 CONFIGURATION CONTROL

APPROVALS	DATE	SCALE	SIZE	DRAWING NUMBER	REV
DRN MARTY SUCHY	02/29/96	N/A	C	(SC)MKT-WG10A	C
ESTD - CHK					
ENGR - CHK					

- NOTES: UNLESS OTHERWISE SPECIFIED
- LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICRONS/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASE METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
 - LEAD 1 IDENTIFICATION SHALL BE:
 - A NOTCH OR OTHER MARK WITHIN THIS AREA
 - A TAB ON LEAD 1, EITHER SIDE
 - NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

		CERPACK, 10 LEAD, GULL WING	
2000 Semiconductor Dr., Santa Clara, CA 95052-8000			

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003181	04/16/99	Rose Malone	Initial MDS Release: MRLM108A-X-RH, Rev. 0A0 - Rad Hard Data Sheet.
1A0	M0003364	04/16/99	Rose Malone	Update MDS: MRLM108A-X-RH, Rev. 0A0 to MRLM108A-X-RH, Rev. 1A0. Update Thermal Resistance - Cerpack (Still Air) from 150 C/W to 225 C/W, Electricals: DC and Drift Values and Post Radiation Section - Removed reference to Rs=5 Mohms from Iio, +Iib, -Iib. Correction made to correlate with test program.