MC100LVEP210

Product Preview

Low-Voltage 1:5 Dual Diff. LVECL/LVPECL/LVEPECL/HSTL Clock Driver

The MC100LVEP210 is a low skew 1–to–5 dual differential driver, designed with clock distribution in mind. The LVECL/LVPECL input signals can be either differential or single–ended if the V_{BB} output is used. The signal is fanned out to 5 identical differential outputs. HSTL inputs can be used when the EP210 is operating in LVPECL mode.

The LVEP210 specifically guarantees low output–to–output skew. Optimal design, layout, and processing minimize skew within a device and from lot to lot.

To ensure the tight skew specification is realized, both sides of the differential output need to be terminated identically into 50Ω even if only one side is being used. When fewer than all ten pairs are used, identically terminate all the output pairs on the same package side whether used or unused. If no outputs on a single side are used, then leave these outputs open (unterminated). This will maintain minimum output skew. Failure to do this will result in a 10–20ps loss of skew margin (propagation delay) in the output(s) in use.

The MC100LVEP210, as with most other LVECL devices, can be operated from a positive V_{CC} supply in LVPECL mode. This allows the LVEP210 to be used for high performance clock distribution in +3.3V or +2.5V systems. Single ended input operation is limited to a VCC ≥ 3.0V in PECL mode, or VEE ≤ –3.0V in ECL mode.

Designers can take advantage of the LVEP210's performance to distribute low skew clocks across the backplane or the board. In a LVPECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on using PECL, designers should refer to Application Note AN1406/D.

- 100ps Part–to–Part Skew
- 35ps Output–to–Output Skew
- Differential Design
- V_{BB} Output
- 475ps Typical Propagation Delay
- High Bandwidth to 1.5GHz Typical
- LVPECL and HSTL mode: 2.375V to 3.8V V_{CC} with V_{EE} = 0V
- LVECL mode: 0V V_{CC} with V_{EE} = –2.375V to –3.8V
- Internal Input Resistors: Pulldown on D, $\overline{D}$
- Pullup and Pulldown on $\overline{CLK}$
- ESD Protection: >2KV HBM, >100V MM
- Moisture Sensitivity Level 2
  For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 461 devices

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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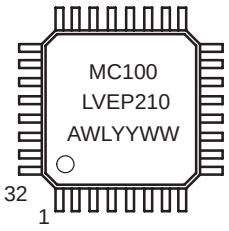
32–LEAD TQFP
FA SUFFIX
CASE 873A

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEP210FA	TQFP	250 Units/Tray
MC100LVEP210FAR2	TQFP	2000 Tape & Reel

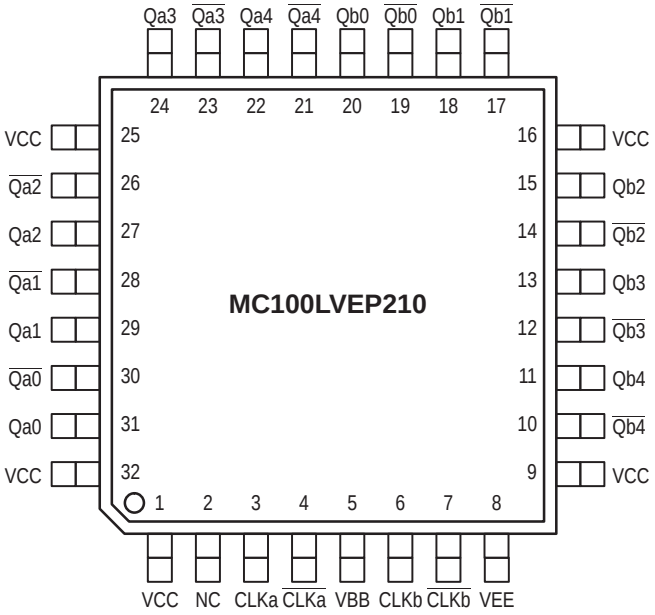


Figure 1. 32–Lead TQFP Pinout (Top View)

PIN DESCRIPTION	
PIN	**FUNCTION**
CLKn/$\overline{\text{CLKn}}$	LVECL/LVPECL/HSTL CLK Inputs
Qn0:4/$\overline{\text{Qn0:4}}$	LVECL/LVPECL Outputs
VBB	Reference Voltage Output
VCC	Positive Supply
VEE	Negative, 0 Supply

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

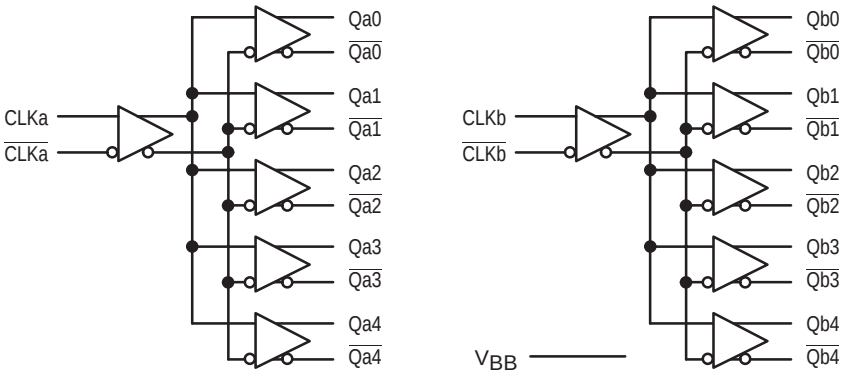


Figure 2. Logic Symbol

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) Still Air 500lfpm	80 55	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	12 to 17	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –3.3(+0.925, –0.5)V) (Note 5.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 1.)					70					mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
V_{BB}	Output Voltage Reference (Note 3.)	–1510	–1410	–1310	–1445	–1345	–1245	–1385	–1285	–1185	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 4.)	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK / $\overline{CLK}$	0.5 / –150			0.5 / –150			0.5 / –150			μA

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. Single ended input operation is limited $V_{EE} \le$ –3.0V in ECL/LVECL mode.
4. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
5. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.5V, V_{EE} = 0V) (Note 10.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 6.)					70					mA
V_{OH}	Output HIGH Voltage (Note 7.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 7.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
V_{BB}	Output Voltage Reference (Note 8.)	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 9.)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK / $\overline{CLK}$	0.5 / –150			0.5 / –150			0.5 / –150			μA

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

6. V_{CC} = 3.3V ± 0.5V, V_{EE} = 0V, all other pins floating.
7. All loading with 50 ohms to V_{CC}–2.0 volts.
8. Single ended input operation is limited $V_{CC} \ge$ –3.0V in PECL mode.
9. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
10. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVEPECL (V_{CC} = 2.5V ± 0.125V, V_{EE} = 0V) (Note 14.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 11.)					70					mA
V_{OH}	Output HIGH Voltage (Note 12.)	1365	1440	1615	1430	1555	1680	1490	1615	1740	mV
V_{OL}	Output LOW Voltage (Note 12.)	565	690	815	630	755	880	690	815	940	mV
V_{IH}	Input HIGH Voltage Single Ended	1290		1615	1355		1680	1415		1740	mV
V_{IL}	Input LOW Voltage Single Ended	565		890	630		955	690		1015	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 13.)	1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

11. V_{CC} = 2.5V, V_{EE} = 0V, all other pins floating.
12. All loading with 50 ohms to V_{EE}.
13. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
14. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, HSTL (V_{CC} = 2.5(–0.125, +1.3)V, V_{EE} = 0V)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage				1200						mV
V_{IL}	Input LOW Voltage						400				mV
$V_{\mathfrak{X}}$	Input Crossover Voltage				680		900				mV
I_{CC}	Power Supply Current (Note 15.)		100			100			100		mA

15. V_{CC} = 2.375V to 3.8V, V_{EE} = 0V, all other pins floating.

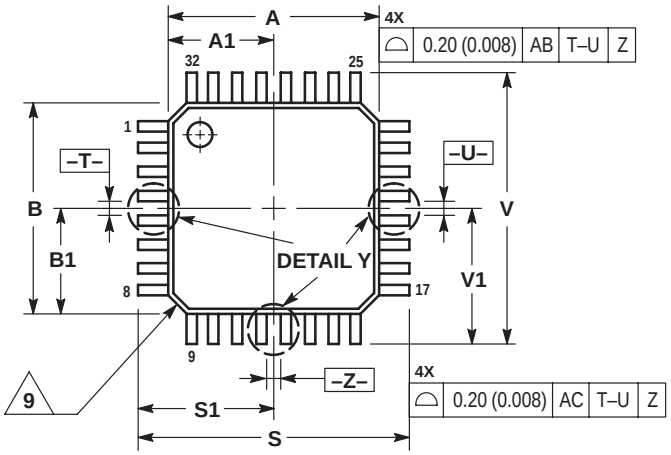
AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –2.5V to –3.8V) or (V_{CC} = 2.5V to 3.8V; V_{EE} = 0V)

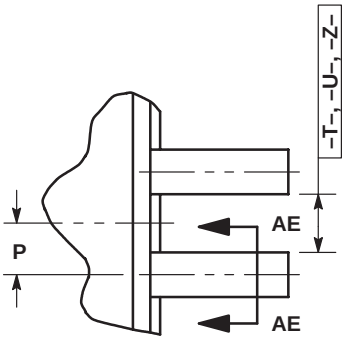
Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{maxLVPECL}$	Maximum Toggle Frequency for LVECL and LVPECL (Note 16.)					1.5					GHz
$f_{maxHSTL}$	Maximum Toggle Frequency for HSTL (Note 16.)					250					MHz
t_{PLH}, t_{PHL}	Propagation Delay Differential					475					ps
t_{SKEW}	Within Device Skew Duty Cycle Skew (Note 17.)		TBD TBD			35 100			TBD TBD		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)					180 180					ps

16. F_{max} guaranteed for functionality only.
17. Skew is measured between outputs under identical transitions of similar paths through a device. Duty cycle skew is defined only for differential operation when the delays are measured from the crosspoint of the inputs to the crosspoint of the outputs.

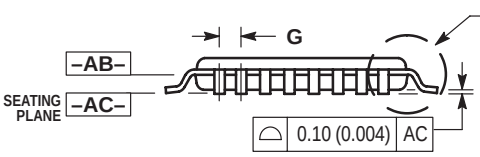
PACKAGE DIMENSIONS

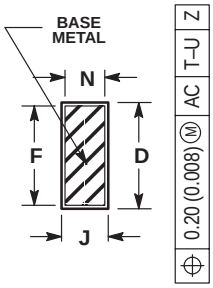
TQFP
FA SUFFIX
32–LEAD PLASTIC PACKAGE
CASE 873A–02
ISSUE A



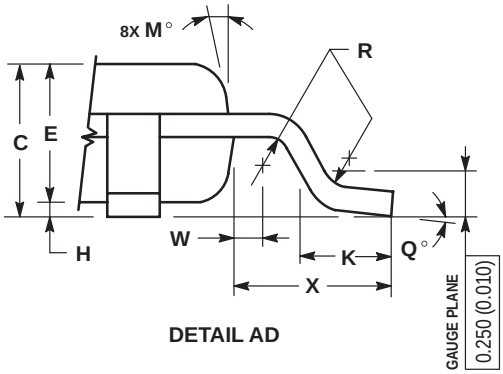


DETAIL Y





SECTION AE–AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

Notes

Notes

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