

MC10EP08



SO-8, D SUFFIX
8-LEAD PLASTIC SOIC PACKAGE
CASE 751

ORDERING INFORMATION

MC10EP08D SOIC

ECLPS Plus™

Product Preview

Differential 2-Input XOR/XNOR

- 230ps Typical Propagation Delay
- High Bandwidth Output Transistors to 3 Ghz Typical
- PECL mode: 3.0V to 5.5V V_{CC} with $V_{EE} = 0V$
- ECL mode: 0V V_{CC} with $V_{EE} = -3.0V$ to $-5.5V$
- Internal Input Resistors: Pulldown on D, Pulldown and Pullup on \overline{D}
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >4KV HBM, >200V MM
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count: 135 devices

The MC10EP08 is a differential XOR/XNOR gate. The EP08 is ideal for applications requiring the fastest AC performance available.

PIN DESCRIPTION

PIN	FUNCTION
D0, D1, $\overline{D0}$, $\overline{D1}$ Q, \overline{Q}	ECL Data Inputs ECL Data Outputs

XOR TRUTH TABLE

D0	$\overline{D0}$	D1	$\overline{D1}$	Q	\overline{Q}
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	H	L
H	L	H	L	L	H



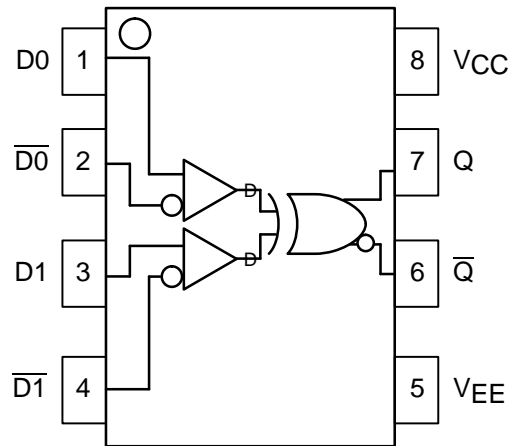


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply ($V_{CC} = 0V$)	-6.0 to 0	VDC
V_{CC}	Power Supply ($V_{EE} = 0V$)	6.0 to 0	VDC
V_I	Input Voltage ($V_{CC} = 0V$, V_I not more negative than V_{EE})	-6.0 to 0	VDC
V_I	Input Voltage ($V_{EE} = 0V$, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current	50 100	mA
	Continuous Surge		
T_A	Operating Temperature Range	-40 to +85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	190 130	°C/W
	Still Air 500lfpm		
θ_{JC}	Thermal Resistance (Junction-to-Case)	41 to 44 \pm 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

DC CHARACTERISTICS, ECL/LVECL ($V_{CC} = 0V$; $V_{EE} = -5.5V$ to $-3.0V$) (Note 4.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 1.)	20	28	36	20	30	38	20	32	38	mA
VOH	Output HIGH Voltage (Note 2.)	-1135	-1060	-885	-1070	-945	-820	-1010	-885	-760	mV
VOL	Output LOW Voltage (Note 2.)	-1935	-1810	-1685	-1870	-1745	-1620	-1810	-1685	-1560	mV
VIH	Input HIGH Voltage Single Ended	-1210		-885	-1145		-820	-1085		-760	mV
VIL	Input LOW Voltage Single Ended	-1935		-1610	-1870		-1545	-1810		-1485	mV
VIHCMR	Input HIGH Voltage Common Mode Range (Note 3.)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	$\frac{D}{\bar{D}}$ 0.5 -150			0.5 -150			0.5 -150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. $V_{CC} = 0V$, $V_{EE} = V_{EEmin}$ to V_{EEmax} , all other pins floating.
2. All loading with 50 ohms to $V_{CC}-2.0$ volts.
3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .
4. Input and output parameters vary 1:1 with V_{CC} .

DC CHARACTERISTICS, LVPECL ($V_{CC} = 3.3V \pm 0.3V$, $V_{EE} = 0V$) (Note 8.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 5.)	20	28	36	20	30	38	20	32	38	mA
VOH	Output HIGH Voltage (Note 6.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
VOL	Output LOW Voltage (Note 6.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
VIH	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
VIL	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
VIHCMR	Input HIGH Voltage Common Mode Range (Note 7.)	2.0		3.3	2.0		3.3	2.0		3.3	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	$\frac{D}{\bar{D}}$ 0.5 -150			0.5 -150			0.5 -150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. $V_{CC} = 3.3V$, $V_{EE} = 0V$, all other pins floating.
6. All loading with 50 ohms to $V_{CC}-2.0$ volts.
7. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .
8. Input and output parameters vary 1:1 with V_{CC} .

DC CHARACTERISTICS, PECL ($V_{CC} = 5.0V \pm 0.5V$, $V_{EE} = 0V$) (Note 12.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 9.)	20	28	36	20	30	38	20	32	38	mA
VOH	Output HIGH Voltage (Note 10.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
VOL	Output LOW Voltage (Note 10.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
VIH	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
VIL	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
VIHCMR	Input HIGH Voltage Common Mode Range (Note 11.)	2.0		5.0	2.0		5.0	2.0		5.0	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	D D̄ 0.5 -150			0.5 -150			0.5 -150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

9. $V_{CC} = 5.0V$, $V_{EE} = 0V$, all other pins floating.

10. All loading with 50 ohms to $V_{CC} - 2.0$ volts.

11. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

12. Input and output parameters vary 1:1 with V_{CC} .

AC CHARACTERISTICS ($V_{CC} = 0V$; $V_{EE} = -3.0V$ to $-5.5V$) or ($V_{CC} = 3.0V$ to $5.5V$; $V_{EE} = 0V$)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{max}	Maximum Toggle Frequency (Note 13.)	2.7	3.0		2.7	3.0		2.7	3.0		GHz
t _{PLH} , t _{PHL}	Propagation Delay D, D̄ → Q, Q̄	100	170	240	120	200	260	150	220	300	ps
t _{SKEW}	Device Skew Part-to-Part (Note 14.) Q, Q̄		TBD TBD			TBD TBD			TBD TBD		ps
t _{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
V _{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t _r , t _f	Output Rise and Fall Times (20% – 80%) Q, Q̄	70	120	170	80	130	180	100	150	200	ps

13. F_{max} guaranteed for functionality only. See Figure 2 for typical output swing. V_{OL} and V_{OH} levels are guaranteed at DC only.

14. Skew is measured between outputs under identical transitions.

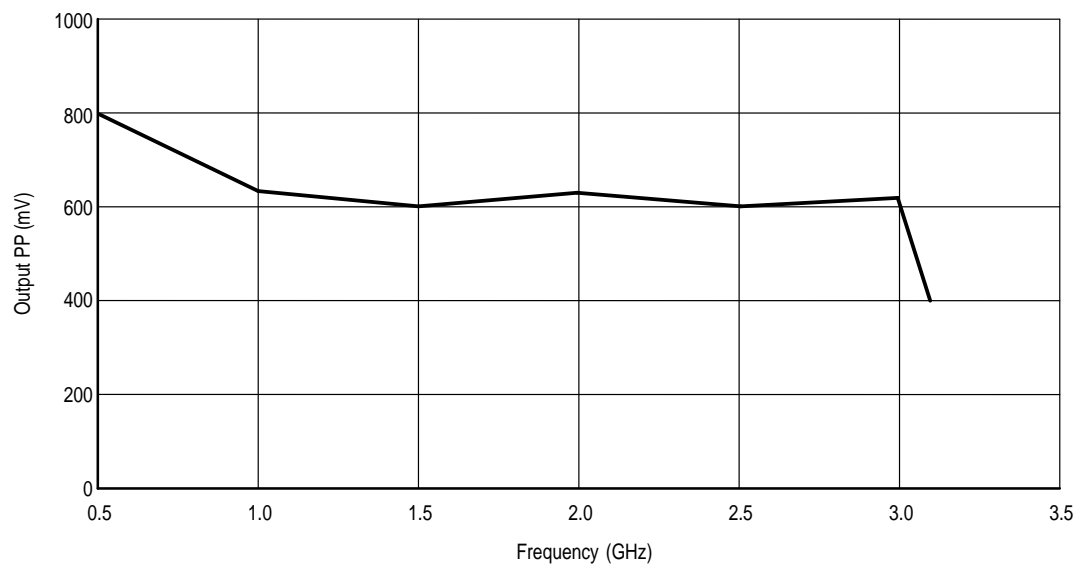
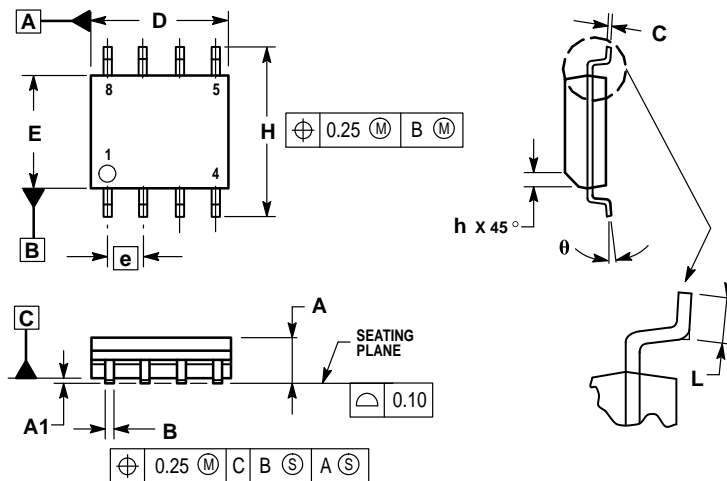


Figure 2. Typical Output V_{pp} vs. Frequency

OUTLINE DIMENSIONS


SO-8, D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-06
ISSUE T



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

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