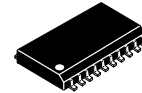


MC10EP14



SO-20, DW SUFFIX
PLASTIC WIDE SOIC PACKAGE
CASE 751D

ORDERING INFORMATION
MC10EP14DW SOIC

ECLPS Plus™

Product Preview

1:5 Clock Distribution Chip

- 475ps Typical Propagation Delay
- 50ps Output-to-Output Skew
- PECL mode: 3.0V to 5.5V V_{CC} with $V_{EE} = 0V$
- ECL mode: 0V V_{CC} with $V_{EE} = -3.0V$ to $-5.5V$
- Synchronous Enable/Disable
- Multiplexed Clock Input
- Internal Input Resistors: Pulldown on D, Pulldown and Pullup on $\overline{D}$
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >4KV HBM, >200V MM
- Maximum Frequency > 2.7GHz
- V_{BB} Output
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack
- Transistor Count = TBD devices
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34

The MC10EP14 is a low skew 1:5 clock distribution chip designed explicitly for low skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. The EP14 is functionally and pin compatible with the EL14 and LVEL14 but is designed to operate in ECL or PECL mode for a voltage supply range of $-3.0V$ to $-5.5V$ (or $3.0V$ to $5.5V$). If a single-ended input is to be used the V_{BB} output should be connected to the $\overline{CLK}$ input and bypassed to ground via a $0.01\mu F$ capacitor. The V_{BB} output is designed to act as the switching reference for the input of the EP14 under single-ended input conditions.

The EP14 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

The common enable ($\overline{EN}$) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip-flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

PIN DESCRIPTION

PIN	FUNCTION
CLK/ $\overline{CLK}$	ECL Diff Clock Inputs
SCLK	ECL Scan Clock Input
$\overline{EN}$	ECL Sync Enable
SEL	ECL Clock Select Input
V_{BB}	ECL Reference Output
Q0-Q4/ $\overline{Q0-Q4}$	ECL Diff Outputs

TRUTH TABLE

CLK	SCLK	SEL	$\overline{EN}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

* On next negative transition of CLK or SCLK



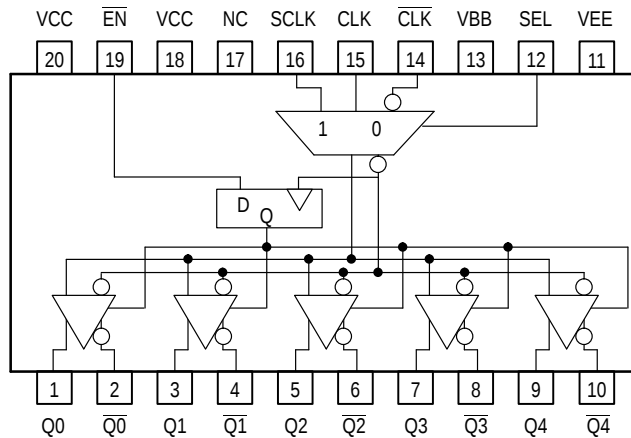


Figure 1. 20-Lead SOIC (Top View) and Logic Diagram

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply ($V_{CC} = 0V$)	-6.0 to 0	VDC
V_{CC}	Power Supply ($V_{EE} = 0V$)	6.0 to 0	VDC
V_I	Input Voltage ($V_{CC} = 0V$, V_I not more negative than V_{EE})	-6.0 to 0	VDC
V_I	Input Voltage ($V_{EE} = 0V$, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	-40 to +85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	90 60	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	30 to 35	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS, ECL/LVECL ($V_{CC} = 0V$; $V_{EE} = -5.5V$ to $-3.0V$) (Note 4.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 1.)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
V _{OH}	Output HIGH Voltage (Note 2.)	-1135	-1060	-885	-1070	-945	-820	-1010	-885	-760	mV
V _{OL}	Output LOW Voltage (Note 2.)	-1935	-1810	-1685	-1870	-1745	-1620	-1810	-1685	-1560	mV
V _{IH}	Input HIGH Voltage Single Ended	-1210		-885	-1145		-820	-1085		-760	mV
V _{IL}	Input LOW Voltage Single Ended	-1935		-1610	-1870		-1545	-1810		-1485	mV
V _{BB}	Output Voltage Reference	-1510	-1410	-1310	-1445	-1345	-1245	-1385	-1285	-1185	mV
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	V _{EE} +2.0		0.0	V _{EE} +2.0		0.0	V _{EE} +2.0		0.0	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current CLK CLK	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. $V_{CC} = 0V$, $V_{EE} = V_{EEmin}$ to V_{EEmax} , all other pins floating.
2. All loading with 50 ohms to $V_{CC}-2.0$ volts.
3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .
4. Input and output parameters vary 1:1 with V_{CC} .

DC CHARACTERISTICS, LVPECL ($V_{CC} = 3.3V \pm 0.3V$, $V_{EE} = 0V$) (Note 8.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 5.)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
V _{OH}	Output HIGH Voltage (Note 6.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V _{OL}	Output LOW Voltage (Note 6.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V _{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V _{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
V _{BB}	Output Voltage Reference	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7.)	2.0		3.3	2.0		3.3	2.0		3.3	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current CLK CLK	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. $V_{CC} = 3.3V$, $V_{EE} = 0V$, all other pins floating.
6. All loading with 50 ohms to $V_{CC}-2.0$ volts.
7. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .
8. Input and output parameters vary 1:1 with V_{CC} .

DC CHARACTERISTICS, PECL ($V_{CC} = 5.0V \pm 0.5V$, $V_{EE} = 0V$) (Note 12.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 9.)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
VOH	Output HIGH Voltage (Note 10.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
VOL	Output LOW Voltage (Note 10.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
VIH	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
VIL	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
VBB	Output Voltage Reference	3490	3590	3690	3555	3655	3755	3615	3715	3815	mV
VIHCMR	Input HIGH Voltage Common Mode Range (Note 11.)	2.0		5.0	2.0		5.0	2.0		5.0	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current CLK CLK	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

9. $V_{CC} = 5.0V$, $V_{EE} = 0V$, all other pins floating.

10. All loading with 50 ohms to V_{CC} -2.0 volts.

11. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

12. Input and output parameters vary 1:1 with V_{CC} .

AC CHARACTERISTICS ($V_{CC} = 0V$; $V_{EE} = -3.0V$ to $-5.5V$) or ($V_{CC} = 3.0V$ to $5.5V$; $V_{EE} = 0V$)

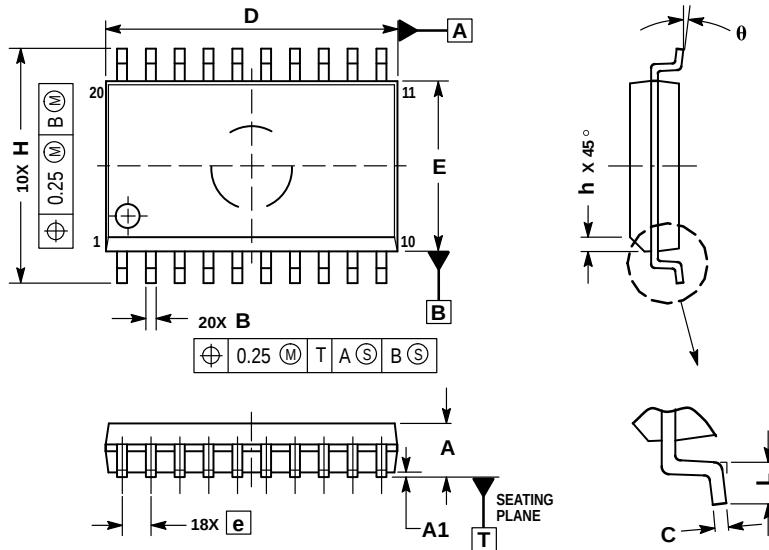
Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{max}	Maximum Toggle Frequency (Note 13.)		TBD			3.5			TBD		GHz
t _{PLH} , t _{PHL}	Propagation Delay Diff CLK to Q SE CLK to Q SCLK to Q		TBD TBD TBD			475 475 475			TBD TBD TBD		ps
t _S	Setup Time $\overline{EN}$		TBD			TBD			TBD		ps
t _H	Hold Time $\overline{EN}$		TBD			TBD			TBD		ps
t _{SKEW}	Within Device Skew Duty Cycle Skew (Note 14.)		TBD TBD			50 200			TBD TBD		ps
t _{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
V _{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t _r t _f	Output Rise/Fall Times Q (20% – 80%)		TBD TBD			120 110			TBD TBD		ps

13. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.

14. Skew is measured between outputs under identical transitions of similar paths through a device. Duty cycle skew is defined only for differential operation when the delays are measured from the crosspoint of the inputs to the crosspoint of the outputs.

OUTLINE DIMENSIONS

SO-20, DW SUFFIX
PLASTIC WIDE SOIC PACKAGE
CASE 751D-06
ISSUE F



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

MILLIMETERS		
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

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