MOTOROLA
Semiconductor Components

Order Number: MC10EP32/D
Rev. 0.2, 06/1999

MC10EP32

SO–8, D SUFFIX
8–LEAD PLASTIC SOIC PACKAGE
CASE 751

ORDERING INFORMATION
MC10EP32D SOIC

ECLinPS Plus™

Product Preview

÷2 Divider

- 355ps Propagation Delay
- >4 GHz Toggle Frequency
- High Bandwidth Output Transistors
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- Internal Input Resistors: Pulldown on D, $\overline{D}$
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >4KV HBM, >200V MM
- V_{BB} Output
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 78 devices

PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Clock Inputs
Reset	ECL Asynch Reset
V_{BB}	Ref Voltage Output
Q, $\overline{Q}$	ECL Data Outputs

TRUTH TABLE

CLK	$\overline{CLK}$	RESET	Q	$\overline{Q}$
X	X	Z	L	H
Z	$\overline{Z}$	L	F	F

Z = LOW to HIGH Transition
$\overline{Z}$ = HIGH to LOW Transition
F = Divide by 2 Function

The MC10EP32 is an integrated ÷2 divider. The differential clock inputs and the V_{BB} allow a differential, single–ended or AC coupled interface to the device. If used, the V_{BB} output should be bypassed to ground with a 0.01μF capacitor.

The reset pin is asynchronous and is asserted on the rising edge. Upon power–up, the internal flip–flops will attain a random state; the reset allows for the synchronization of multiple EP32’s in a system.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

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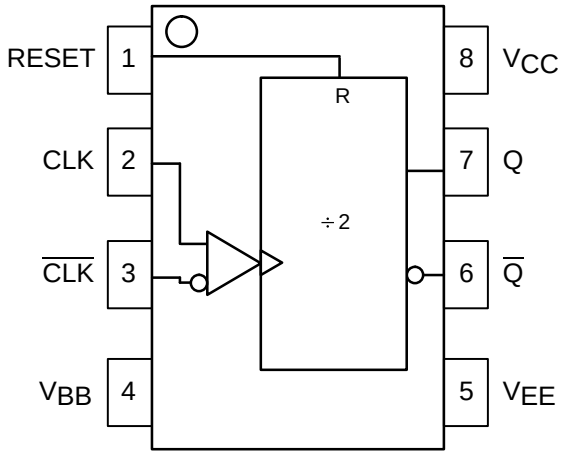


Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –5.5V to –3.0V) (Note 4.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
IEE	Power Supply Current (Note 1.)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
V_{BB}	Output Voltage Reference	–1510	–1410	–1310	–1445	–1345	–1245	–1385	–1285	–1185	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current CLK	0.5			0.5			0.5			µA
	$\overline{CLK}$	–150			–150			–150			

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
4. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 8.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
IEE	Power Supply Current (Note 5.)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
V_{OH}	Output HIGH Voltage (Note 6.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 6.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
V_{BB}	Output Voltage Reference	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7.)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current CLK	0.5			0.5			0.5			µA
	$\overline{CLK}$	–150			–150			–150			

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. V_{CC} = 3.3V, V_{EE} = 0V, all other pins floating.
6. All loading with 50 ohms to V_{CC}–2.0 volts.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
8. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 12.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current (Note 9.)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
V_{OH}	Output HIGH Voltage (Note 10.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 10.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
V_{BB}	Output Voltage Reference	3490	3590	3690	3555	3655	3755	3615	3715	3815	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 11.)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 –150			0.5 –150			0.5 –150			µA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

9. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
10. All loading with 50 ohms to V_{CC}–2.0 volts.
11. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
12. Input and output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V) or (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency (Note 13.)	TBD			TBD	4.0		TBD			GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential CLK–>Q, $\overline{Q}$ RESET–>Q, $\overline{Q}$	 TBD TBD			 TBD TBD	 300 300		 TBD TBD			ps
t_{RR}	Set/Reset Recovery		TBD			TBD			TBD		ps
t_{SKEW}	Duty Cycle Skew (Note 14.)		5.0			5.0	20		5.0	20	ps
t_{PW}	Minimum Pulse Width RESET		TBD			TBD			TBD		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times (20% – 80%) Q, $\overline{Q}$		TBD TBD			120 110			TBD TBD		ps

13. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
14. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

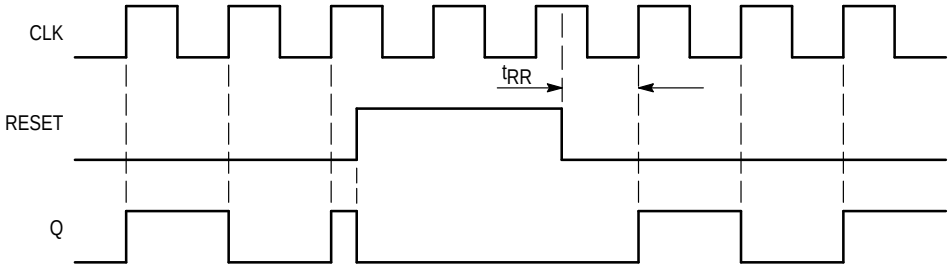
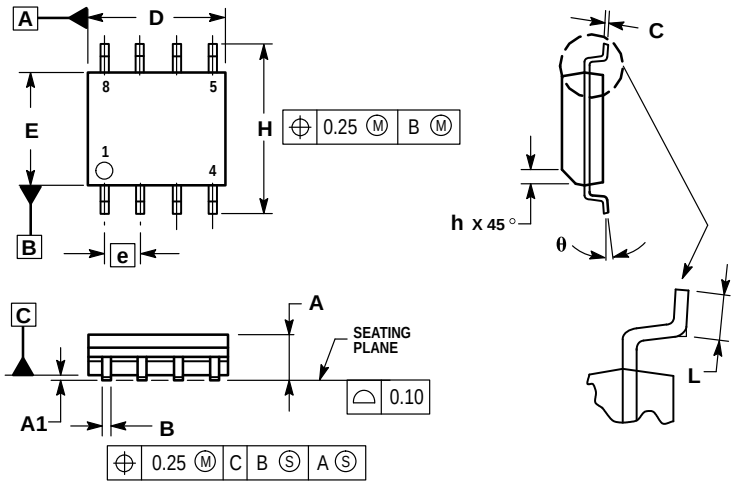


Figure 2. Timing Diagram

OUTLINE DIMENSIONS

SO–8, D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–06
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

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