

Product Preview

TMOS V™

SO-8 for Surface Mount

N-Channel Enhancement-Mode Silicon Gate

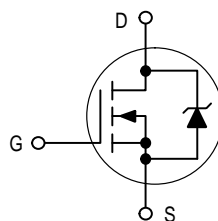
TMOS V is a new technology designed to achieve an on-resistance area product about one-half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E-FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

New Features of TMOS V

- On-resistance Area Product about One-half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E-FET Predecessors

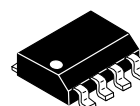
Features Common to TMOS V and TMOS E-FETs

- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E-FET
- Miniature SO-8 Surface Mount Package – Saves Board Space
- Mounting Information for SO-8 Package Provided

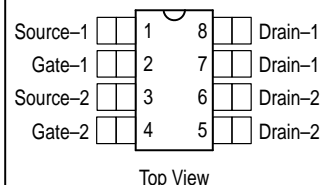


MMDF3N06VL

DUAL TMOS MOSFET
3.3 AMPERES
60 VOLTS
 $R_{DS(on)} = 0.130 \text{ OHM}$



CASE 751-06, Style 11
SO-8



MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	60	Vdc
Drain-to-Gate Voltage, ($R_{GS} = 1 \text{ M}\Omega$)	V_{DGR}	60	Vdc
Gate-to-Source Voltage — Continuous	V_{GS}	± 15	Vdc
Drain Current — Continuous @ $T_A = 25^\circ\text{C}$	I_D	3.3	Adc
— Continuous @ $T_A = 100^\circ\text{C}$	I_D	0.7	
— Single Pulse ($t_p \leq 10 \mu\text{s}$)	I_{DM}	10	Apk
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (1)	P_D	2.0	W
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy — Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 25 \text{ Vdc}$, $V_{GS} = 5.0 \text{ Vdc}$, Peak $I_L = 3.3 \text{ Apk}$, $L = 10 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	54	mJ
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 0.0625" from case for 10 seconds	T_L	260	$^\circ\text{C}$

DEVICE MARKING

2N6VL

(1) Mounted on G10/FR4 glass epoxy board using minimum recommended footprint.

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMDF3N06VLR2	13"	12mm embossed tape	2500

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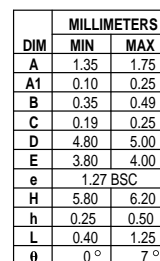
MMDF3N06VL

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 0.25 mAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	60 —	— 66	— —	Vdc mV/°C	
Zero Gate Voltage Drain Current (V _{DS} = 60 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 60 Vdc, V _{GS} = 0 Vdc, T _J = 150°C)	I _{DSS}	— —	— —	10 100	μAdc	
Gate-Body Leakage Current (V _{GS} = ± 15 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	100	nAdc	
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	1.0 —	1.5 3.0	2.0 —	Vdc mV/°C	
Static Drain-to-Source On-Resistance (V _{GS} = 5.0 Vdc, I _D = 3.3 Adc)	R _{DS(on)}	—	0.12	0.13	Ohm	
Drain-to-Source On-Voltage (V _{GS} = 5.0 Vdc, I _D = 3.3 Adc) (V _{GS} = 5.0 Vdc, I _D = 1.65 Adc, T _J = 150°C)	V _{DS(on)}	— —	— —	0.5 0.4	Vdc	
Forward Transconductance (V _{DS} = 15 Vdc, I _D = 1.65 Adc)	g _{FS}	1.0	3.0	—	Mhos	
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V _{DS} = 25 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	—	340	pF	
Output Capacitance		C _{oss}	—	110		
Transfer Capacitance		C _{rss}	—	27		
SWITCHING CHARACTERISTICS(2)						
Turn-On Delay Time	(V _{DD} = 30 Vdc, I _D = 3.3 Adc, V _{GS} = 5.0 Vdc, R _G = 9.1 Ω)	t _{d(on)}	—	10	ns	
Rise Time		t _r	—	30		
Turn-Off Delay Time		t _{d(off)}	—	32		
Fall Time		t _f	—	28		
Gate Charge	(V _{DS} = 48 Vdc, I _D = 3.3 Adc, V _{GS} = 5.0 Vdc)	Q _T	—	9.0	nC	
		Q ₁	—	1.5		
		Q ₂	—	4.3		
		Q ₃	—	3.5		
SOURCE-DrAIN DIODE CHARACTERISTICS						
Forward On-Voltage(1)	(I _S = 3.3 Adc, V _{GS} = 0 Vdc) (I _S = 3.3 Adc, V _{GS} = 0 Vdc, T _J = 150°C)	V _{SD}	— —	0.84 0.67	1.2 —	Vdc
Reverse Recovery Time	(I _S = 3.3 Adc, V _{GS} = 0 Vdc, dI _S /dt = 100 A/μs)	t _{rr}	—	58	ns	
		t _a	—	38		
		t _b	—	20		
Reverse Recovery Storage Charge		Q _{RR}	—	0.11	—	μC


(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.



PIN 1.	SOURCE 1
2.	GATE 1
3.	SOURCE 2
4.	GATE 2
5.	DRAIN 2
6.	DRAIN 2
7.	DRAIN 1
8.	DRAIN 1

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