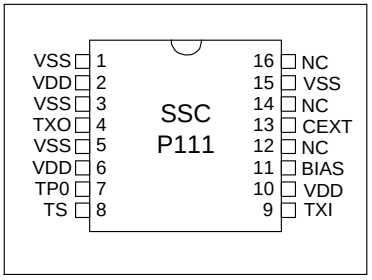
Intellon
CONNECTING THE FUTURE™

Technical Data Sheet **SSC P111 PL Media Interface IC**

Features

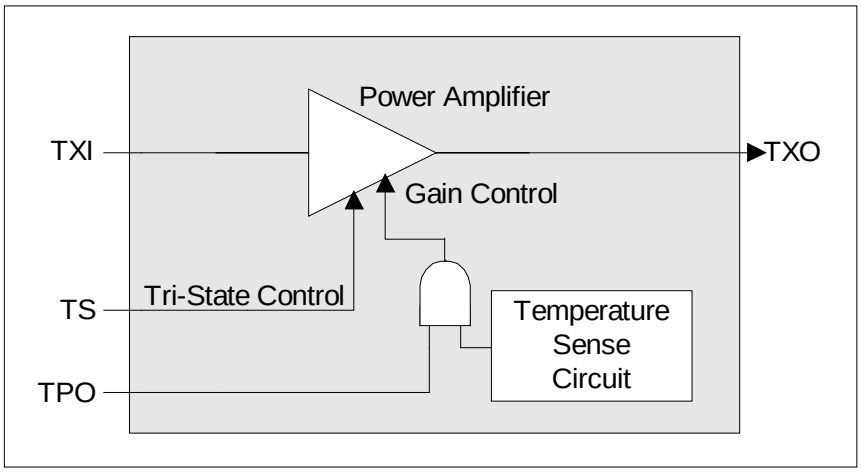


- Integrates Power Amplifier and Tri-state functions for CEBus Powerline (PL) Physical Interfaces
- Replaces approximately 30 discrete components to save board space and increase reliability
- Implements high-drive Output Amplifier (6 Vp-p into 10 ohm load) to increase performance under low impedance conditions
- Output Amplifier is a Class AB configuration for increased efficiency and lower power consumption
- Incorporates built-in over temperature protection circuit for improved system reliability
- Serves as companion IC to Intellon SSC P300 and P200 Network Controller IC's
- 16 Pin SOIC Package

Introduction

The SSC P111 PL Media Interface IC provides the functions of Output Power Amplifier and Output Tri-state Switch for power line transceiver products. The Output Power Amplifier meets the requirements specified by the EIA-600 (CEBus) Standard for output voltage levels into typical and low impedance power line loads and incorporates over-temperature protection for improved system reliability. The IC replaces approximately 30 of the discrete components normally used in support of PL transceivers and reduces required printed circuit board area by up to 50%.

SSC P111 IC Block Diagram



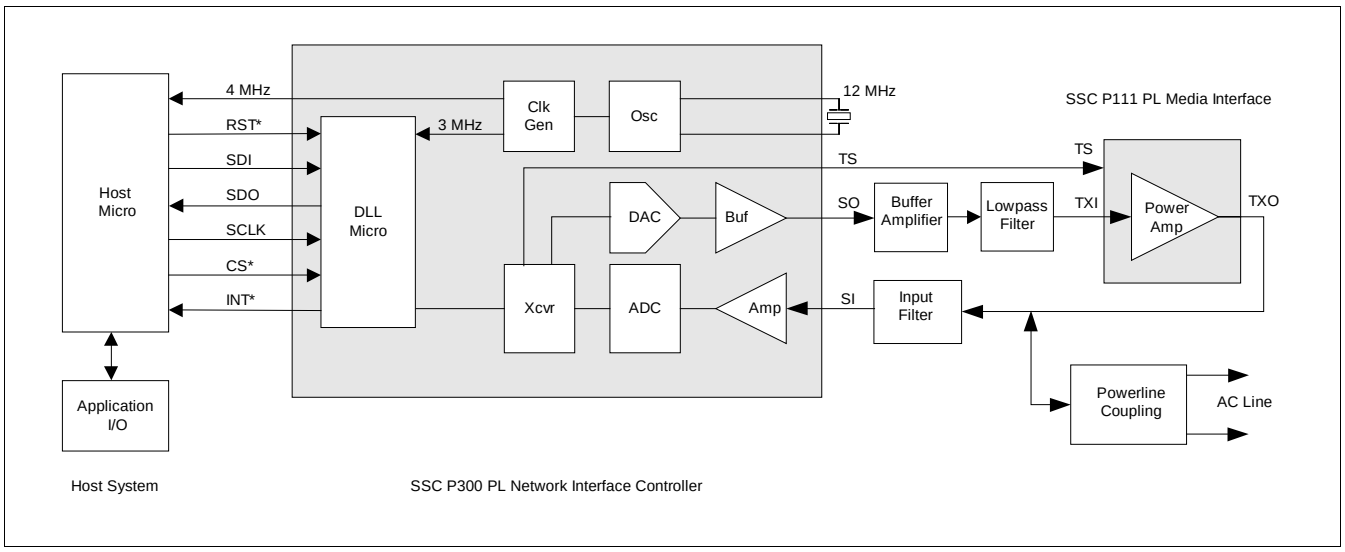
CEBus Power line “Node” Overview

As illustrated in the node block diagram below, the Host microprocessor interprets commands and data for the User Application and provides the upper layers (Application and high-level Network) of the CEBus communication protocol. Low-level Network, Data Link, and Physical layer services of the protocol are provided by the Intellon SSC P300 Network IC. Output signal amplification is provided by the SSC P111 PL Media Interface IC. The Buffer Amplifier, Low-pass Pre-filter and Input Filter functions are performed using external discrete components. Likewise, discrete components are also utilized to couple the Node to the power line.

SSC P111 Functionality

When transmitting, the output “chirp” waveform from the SSC P300 SO pin is buffered by an external unity gain Buffer Amplifier before being filtered by an external low-pass filter. Once the signal passes through the filter, the output waveform is applied to the SSC P111 TXI pin for amplification by the Power Amplifier and then applied to the external Power line Coupling/Filter network. The Tri-State (TS) signal from the SSC P300 disconnects the SSC P111 power amplifier from the coupling network when the system is in the receive mode and places the SSC P111 power amplifier in a power-down state. Under output overload conditions, temperature sense circuitry inside the SSC P111 reduces the power amplifier fixed gain from 2 to 1, which will lower the output transistor power dissipation.

Application Block Diagram Using the SSC P111 and SSC P300



SSC P111 Transient Protection

Since the SSC P111 drives the AC power line, voltage transients present on the line will conduct back through the coupling circuitry and onto the SSC P111 output pin. Under certain conditions, transients with high amplitudes and/or fast rise times can cause the SSC P111 IC to become damaged. Transient suppression circuitry is required to ensure proper operation of the SSC P111 IC. The recommended protection circuitry includes a MOV/Zener Diode combination at the AC Power Line Coupler, and a Transient Voltage Suppressor (TVS)/Schottky Diode combination at the SSC P111 IC output pin. Refer to Application Note #0071, “Surge Protection Techniques for Power Line Communications”, and the Hardware Design Reference document for the SSC P300 and P200.

Keep in mind that these recommendations may not be sufficient for all applications and that environments with high voltage transient activity may require additional protection elements.

Absolute Maximum Ratings(1)

Symbol	Parameter	Value	Unit
V_{DDMAX}	DC Supply Voltage	0 to +11.0	V
V_{IN}	Input Voltage (any pin)	V_{SS} - 0.3 to V_{DD}	V
T_{STG}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (Soldering, 10 Sec.)	300	°C
ESD	ESD Tolerance (2)	2	kV

Notes: 1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.
2) ESD uses MIL-STD-833C Method 3015 as a guideline to testing.

Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit
V_{DD}	DC Supply Voltage	9.0	10.0	11.0	V
T_A	Operating Temperature	-40	+25	+85	°C
	Humidity		non-condensing		

Electrical Characteristics

Symbol	Parameter	Min	Typical	Max	Unit	Notes
Z_{IN}(PA)	Power Amplifier Input Resistance	1.4	2	2.7	KΩ	
A_V(PA)	Power Amplifier Voltage Gain	1.8	2	2.2	V/V	
V_{IN}(PA)	Input Voltage range of Power Amplifier		3	3.5	Vac	
PM(PA)	Phase Margin of Power Amplifier		78		Deg	
G_{BW}(PA)	Gain Bandwidth of Power Amplifier	1.1		2.1	MHz	
V_{IH}	Minimum High-level Input Voltage	4.0			V	(1)
V_{IL}	Maximum Low-level Input Voltage			0.5	V	(1)
I_{IL}	Maximum Input Leakage Current			+/-10	μA	(1)
Hys	Minimum Input Hysteresis	350			mV	(1)
T_{enbl}	TS to Power Amp output signal valid			500	ns	
T_{disabl}	TS to Power Amp output tristate			50	ns	
I_{DD} (TX)	Supply Current (Transmit)		140	250	mA	(2)
I_{DD} (RX)	Supply Current (Receive)		10	20	mA	
	Latchup	150			mA	(3)

Notes: 1) Input Signal TS
2) Typical value for driving 10 Ohm, AC coupled load
3) JEDEC JC-40.2

SSC P111 Pin Assignments

Pin	Mnemonic	Name	Description
1	VSS	Analog Ground	Ground Reference.
2	VDD	Analog Supply	Power Amplifier +10 VDC +/- 10% analog supply voltage with respect to VSS.
3	VSS	Analog Ground	Power Amplifier Ground Reference.
4	TXO	PowerAmp Output	Power Amplifier signal output. Transmit enabled with TS = Logic 1.
5	VSS	Analog Ground	Power Amplifier Ground Reference.
6	VDD	Analog Supply	Power Amplifier +10 VDC +/- 10% analog supply voltage with respect to VSS.
7	TP0	Test Pin 0	Reserved pin for testing. Connect pin to VDD supply
8	TS	Tristate In	TTL-level digital input signal driven from the transceiver. Logic 0 places Power Amplifier in tri-state mode.
9	TXI	PowerAmp Input	Power Amplifier signal input.
10	VDD	Analog Supply	+10 VDC +/- 10% analog supply voltage with respect to VSS.
11	BIAS	Bias Input	Connection for external 75Kohm, 1% bias resistor to ground.
12	NC	No Connect	Do not connect to this pin.
13	CEXT	External Capacitor	Connection for external 1 uF capacitor to ground.
14	NC	No Connect	Do not connect to this pin.
15	VSS	Analog Ground	Ground Reference.
16	NC	No Connect	Do not connect to this pin.

Typical Performance Characteristics

V_{DD} = 9 VDC, V_{ss} = 0 VDC, T_A = 25° C unless otherwise indicated.

Input signal is at a constant 100% transmit rate with Spread Spectrum Carrier Chirps.

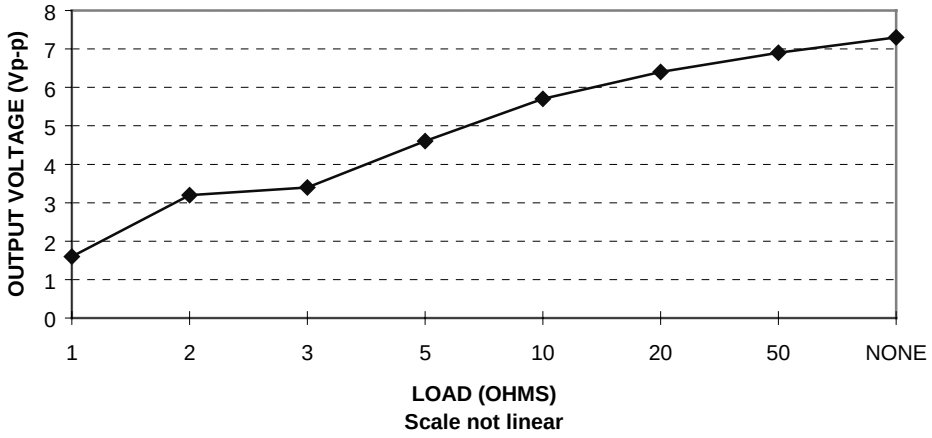


Figure 2. P111 Output Voltage VS. Load (Transmit Mode)

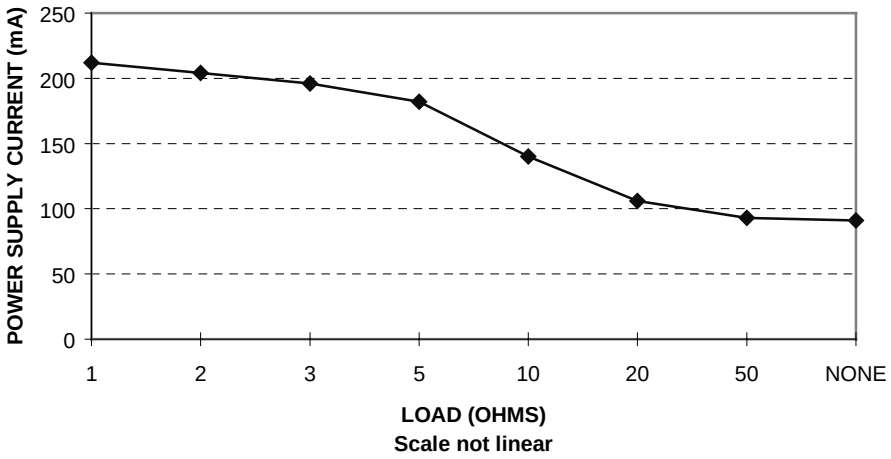


Figure 3. P111 Power Supply Current VS. Load (Transmit Mode)

SSC P111 Mechanical Specifications

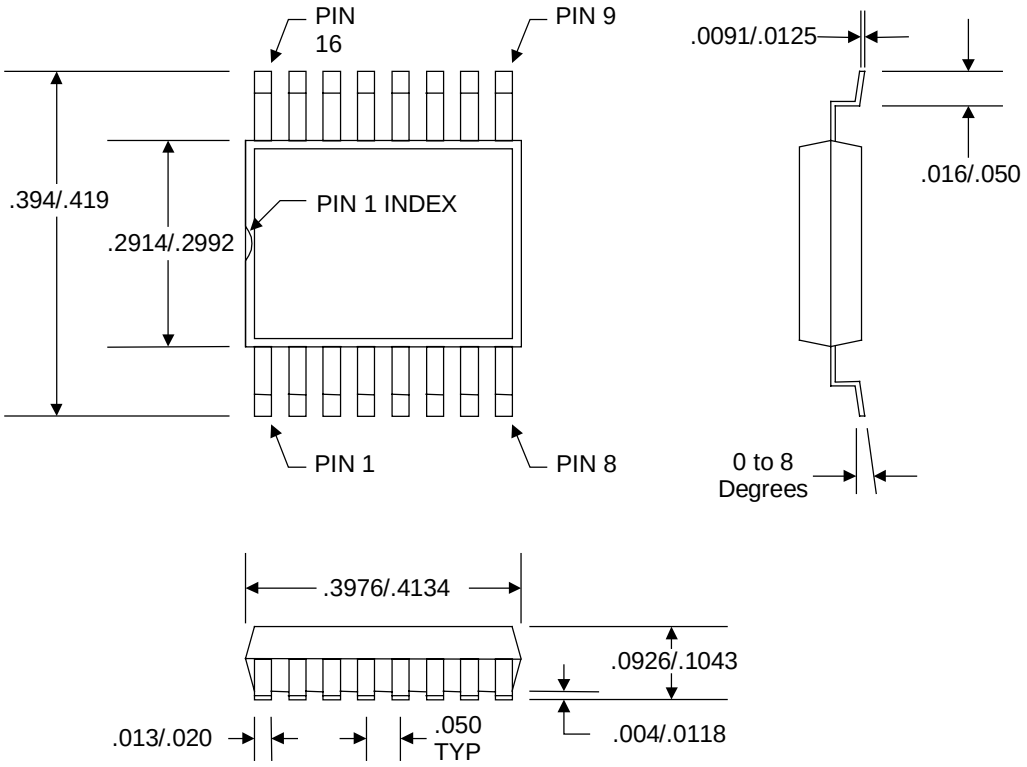


Figure 4. 16 Pin SOIC Package Outline in inches

Ordering Information

SSC P111 PL Media Interface IC

Intellon
CONNECTING THE FUTURE™

5100 West Silver Springs Boulevard
Ocala, Florida 34482

Phone: (352) 237-7416
Fax: (352) 237-7616

Internet
http://www.intellon.com
ftp://ftp.intellon.com