CONTENTS

Remote 16-bit I/O expander for I²C-bus PCF8575

1 FEATURES

- Operating supply voltage 2.5 to 5.5 V
- Low standby current consumption of 10 μA maximum
- I²C-bus to parallel port expander
- 400 kbits/s FAST I²C-bus
- Open-drain interrupt output
- 16-bit remote I/O port for the I²C-bus
- Compatible with most microcontrollers
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices
- SSOP24 package.

2 GENERAL DESCRIPTION

The PCF8575 is a silicon CMOS circuit. It provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I²C-bus).

The device consists of a 16-bit quasi-bidirectional port and an I²C-bus interface. The PCF8575 has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line ($\overline{INT}$) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. This means that the PCF8575 is an I²C-bus slave transmitter/receiver.

Every data transmission from the PCF8575 must consist of an even number of bytes, the first byte will be referred to as P07 to P00 and the second byte as P17 to P10. The third will be referred to as P07 to P00 and so on.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8575TS	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

4 BLOCK DIAGRAM

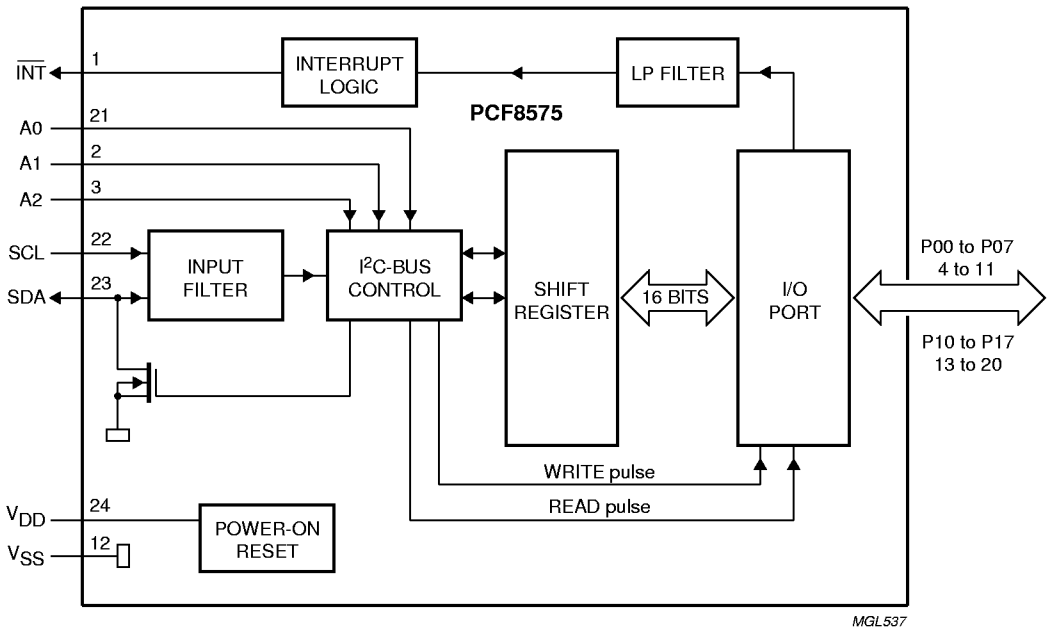


Fig.1 Block diagram.

5 PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{INT}$	1	interrupt output (active LOW)
A1	2	address input 1
A2	3	address input 2
P00	4	quasi-bidirectional I/O 00
P01	5	quasi-bidirectional I/O 01
P02	6	quasi-bidirectional I/O 02
P03	7	quasi-bidirectional I/O 03
P04	8	quasi-bidirectional I/O 04
P05	9	quasi-bidirectional I/O 05
P06	10	quasi-bidirectional I/O 06
P07	11	quasi-bidirectional I/O 07
V_{SS}	12	supply ground
P10	13	quasi-bidirectional I/O 10
P11	14	quasi-bidirectional I/O 11
P12	15	quasi-bidirectional I/O 12
P13	16	quasi-bidirectional I/O 13
P14	17	quasi-bidirectional I/O 14
P15	18	quasi-bidirectional I/O 15
P16	19	quasi-bidirectional I/O 16
P17	20	quasi-bidirectional I/O 17
A0	21	address input 0
SCL	22	serial clock line input
SDA	23	serial data line input/output
V_{DD}	24	supply voltage

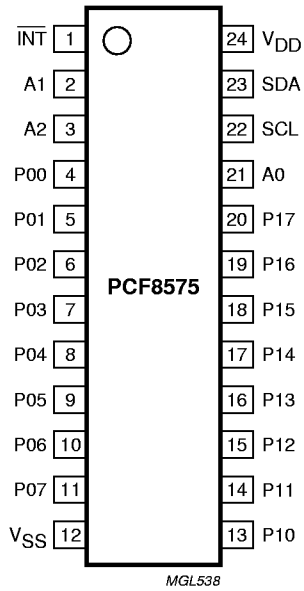


Fig.2 Pin configuration.

6 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

6.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Fig.3).

6.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S).

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition P (see Fig.4).

6.3 System configuration

A device generating a message is a 'transmitter', a device receiving the message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Fig.5).

6.4 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The transmitter must release the SDA line before the receiver can send an acknowledge bit.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge after the last byte that has been clocked out of the slave. This is done by the master receiver by holding the SDA line HIGH. In this event the transmitter must release the data line to enable the master to generate a STOP condition.

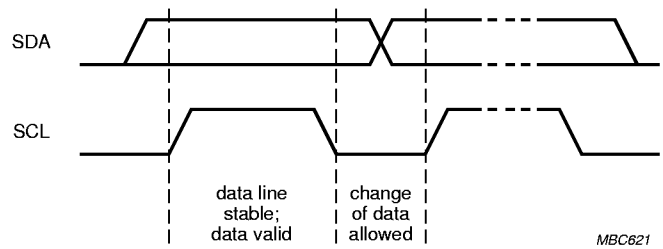


Fig.3 Bit transfer.

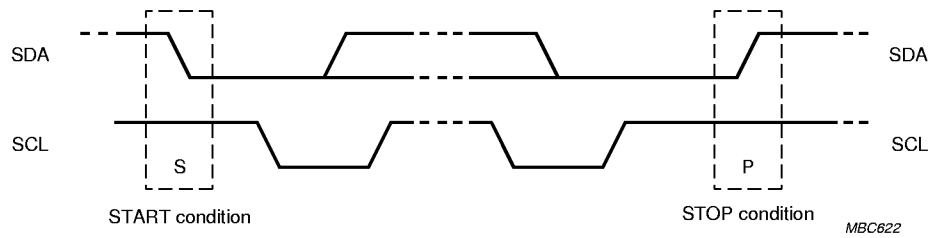


Fig.4 Definition of START and STOP conditions.

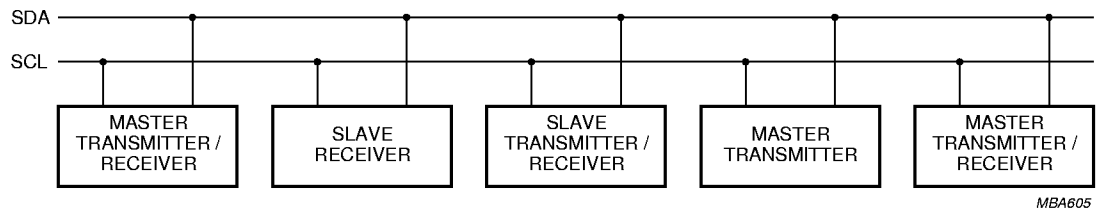


Fig.5 System configuration.

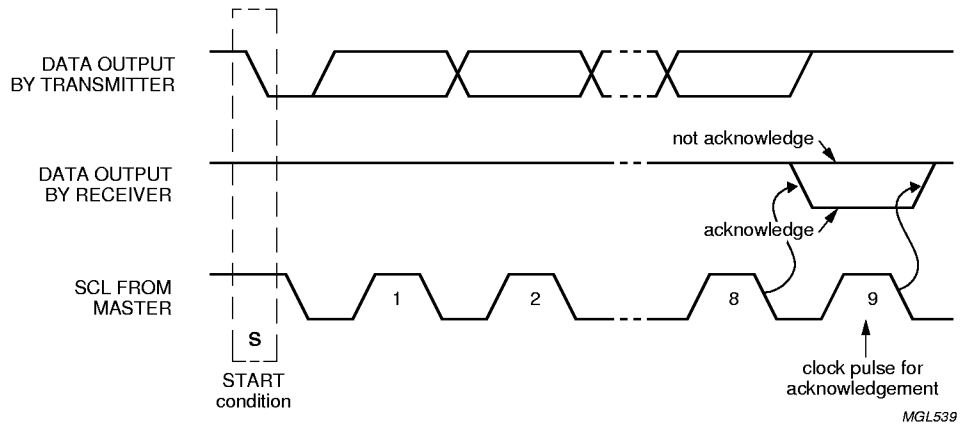


Fig.6 Acknowledgment on the I²C-bus.

7 FUNCTIONAL DESCRIPTION

7.1 Quasi-bidirectional I/Os

The PCF8575's 16 ports (see Fig.7) are entirely independent and can be used either as input or output ports. Input data is transferred from the ports to the microcontroller in the READ mode (see Fig.10). Output data is transmitted to the ports in the WRITE mode (see Fig.9).

This quasi-bidirectional I/O can be used as an input or output without the use of a control signal for data direction. At power-on the I/Os are HIGH. In this mode only a current source (I_{OH}) to V_{DD} is active. An additional strong pull-up to V_{DD} (I_{OHt}) allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The I/Os should be HIGH before being used as inputs. After power-on as all the I/Os are set HIGH all of them can be used as input. Any change in setting of the I/Os as either inputs or outputs can be done with the write mode. Warning: If a HIGH is applied to an I/O which has been written earlier to LOW, a large current (I_{OL}) will flow to V_{SS}. (see Characteristics note 3).

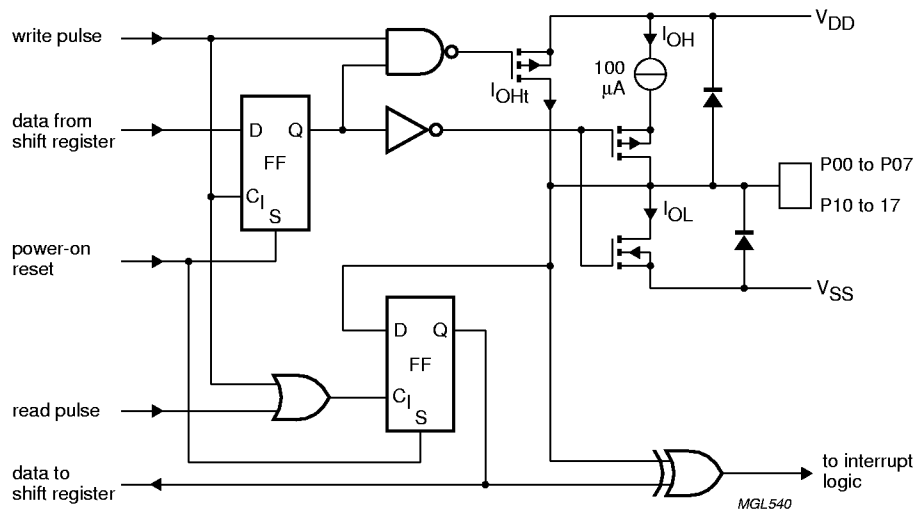


Fig.7 Simplified schematic diagram of each I/O.

7.2 Addressing

Figures 8, 9 and 10 show the address and timing diagrams. Before any data is transmitted or received the master must send the address of the receiver via the SDA line. The first byte transmitted after the START condition carries the address of the slave device and the read/write bit. The address of the slave device must not be changed between the START and the STOP conditions. The PCF8575 acts as a slave receiver or a slave transmitter.

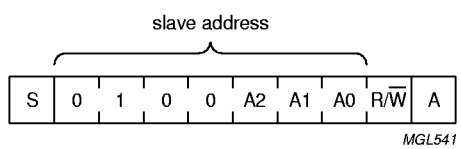


Fig.8 Byte containing the slave address and the R/$\overline{W}$ bits.

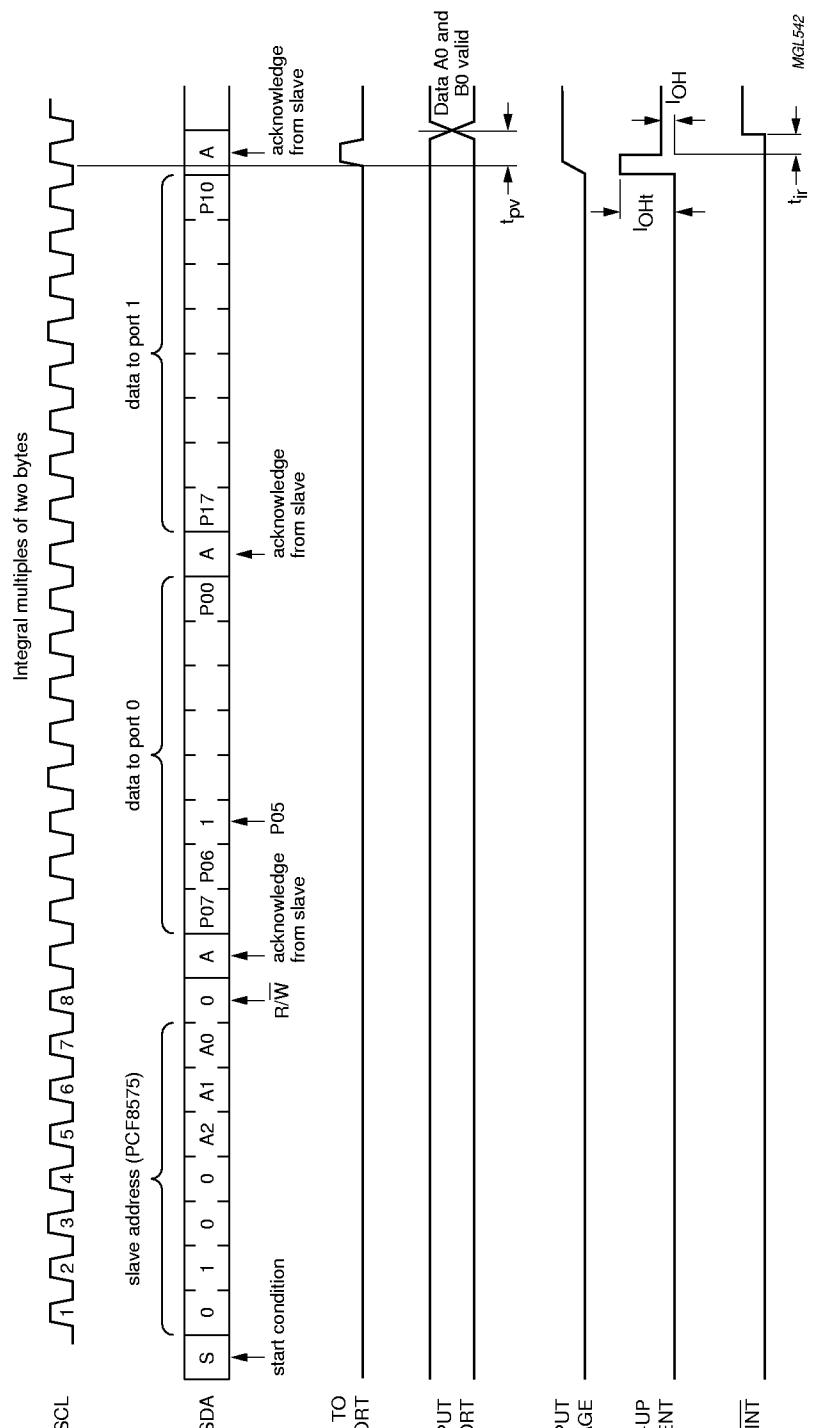
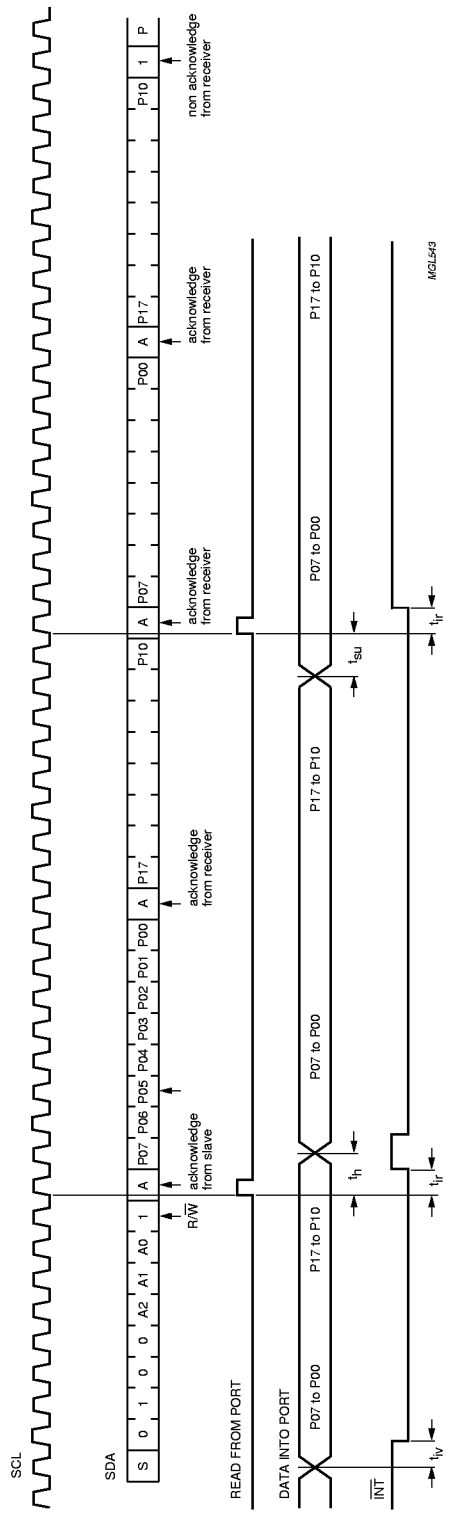


Fig.9 WRITE mode (output).



A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the STOP condition (P). Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). Input data is lost.

Fig.10 READ mode (input).

7.3 Reading from a port (input mode)

All ports programmed as input should be set to logic 1. To read, the master (microcontroller) first addresses the slave device after it receives the interrupt. By setting the last bit of the byte containing the slave address to logic 1 the read mode is entered. The data bytes that follow on the SDA are the values on the ports.

If the data on the input port changes faster than the master can read, this data may be lost.

7.4 Writing to the port (output mode)

To write, the master (microcontroller) first addresses the slave device. By setting the last bit of the byte containing the slave address to logic 0 the write mode is entered. The PCF8575 acknowledges and the master sends the first data byte for P07 to P00. After the first data byte is acknowledged by the PCF8575, the second data byte P17 to P10 is sent by the master. Once again the PCF8575 acknowledges the receipt of the data after which this 16-bit data is presented on the port lines.

The number of data bytes that can be sent successively is not limited. After every two bytes the previous data is overwritten.

The first data byte in every pair refers to Port 0 (P07 to P00), whereas the second data byte in every pair refers to Port 1 (P17 to P10), see Fig.11.

7.5 Interrupt

The PCF8575 provides an open-drain interrupt ($\overline{INT}$) which can be fed to a corresponding input of the microcontroller (see Figs 9, 10 and 12). This gives these chips a kind of a master function which can initiate an action elsewhere in the system.

An interrupt is generated by any rising or falling edge of the port inputs. After time t_{iv} the signal $\overline{INT}$ is valid.

The interrupt disappears when data on the port is changed to the original setting or data is read from or written to the device which has generated the interrupt.

In the write mode the interrupt may become deactivated (HIGH) on the rising edge of the write to port pulse. On the falling edge of the write to port pulse the interrupt is definitely deactivated (HIGH).

The interrupt is reset in the read mode on the rising edge of the read from port pulse.

During the resetting of the interrupt itself any changes on the I/Os may not generate an interrupt. After the interrupt is reset any change in I/Os will be detected and transmitted as an $\overline{INT}$.

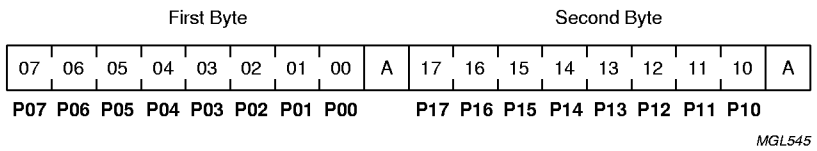


Fig.11 Correlation between bits and ports.

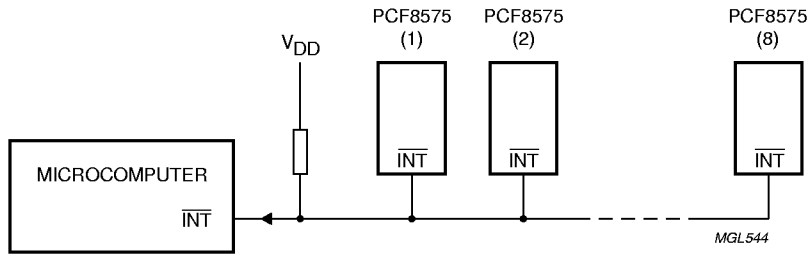


Fig.12 Application of multiple PCF8575s with interrupt.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); note 1.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
I_{DD}	supply current	−	±100	mA
I_{SS}	supply current	−	±100	mA
V_I	input voltage	V_{SS} − 0.5	V_{DD} + 0.5	V
I_I	DC input current	−	±20	mA
I_O	DC output current	−	±25	mA
P_{tot}	total power dissipation	−	400	mW
P_O	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−40	+85	°C

Note

1. Stress above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC12 under *"Handling MOS Devices"*.

10 CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2.5	−	5.5	V
I_{DD}	supply current	operating mode; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 400 kHz	−	100	200	µA
$I_{DD(stb)}$	standby current	standby mode; no load; $V_I = V_{DD}$ or V_{SS}	−	2.5	10	µA
V_{POR}	power-on reset voltage	note 1	−	1.2	1.8	V
V_{IL1}	LOW-level input voltage pins A0, A1 and A2		0.0	−	$0.2V_{DD}$	V
V_{IL2}	LOW-level input voltage on all other signal pins		0.0	−	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	−	V_{DD}	V
I_{L1}	leakage current at pins A0, A1 and A2	$V_I = V_{DD}$ or V_{SS}	−1	−	+1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{L2}	leakage current on all other signal pins	$V_I = V_{DD}$ or V_{SS}	−10	–	+10	μA
Input SCL; input/output SDA						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; note 3	3	–	–	mA
C_I	input capacitance	$V_I = V_{SS}$; note 2	–	–	7	pF
I/Os; P00 to P07 and P10 to P17						
I_{OL}	LOW-level output current	V_{OL} = 1 V; note 3	10	25	–	mA
I_{OH}	HIGH-level output current	$V_{OH} = V_{SS}$	−30	–	−300	μA
I_{OHt}	transient pull-up current	$V_{OH} = V_{SS}$; see Fig.9	−0.5	−1.0	–	mA
C_I	input capacitance	note 2	–	–	10	pF
C_O	output capacitance	note 2	–	–	10	pF
Port timing; $C_L \leq$ 100 pF (see Figs 9 and 10)						
t_{pv}	output data valid		–	–	4	μs
t_{su}	input data set-up time		0	–	–	μs
t_h	input data hold time		4	–	–	μs
Interrupt $\overline{INT}$ (see Fig.13)						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	1.6	–	–	mA
TIMING; $C_L \leq$ 100 pF (see Figs 9 and 10)						
t_{iv}	input data valid time		–	–	4	μs
t_{ir}	reset delay time		–	–	4	μs

Notes

1. The power-on reset circuit resets the I²C-bus logic with $V_{DD} < V_{POR}$ and sets all I/Os to logic 1 (with current source to V_{DD}).
2. The value is not tested, but verified on sampling basis.
3. A single LOW-level output current (I_{OL}) must not exceed 20 mA for an extended time. The sum of all I_{OL}s at any point in time must not exceed 100 mA.

11 I²C-BUS TIMING CHARACTERISTICS

See Fig.13 and note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{SCL}	SCL clock frequency		–	400	kHz
t_{SW}	tolerable spike width on bus	note 2	–	50	ns
t_{BUF}	BUS free time between a STOP and START condition		1.3	–	µs
$t_{SU;STA}$	START condition set-up time		0.6	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	µs
t_{LOW}	SCL LOW time		1.3	–	µs
t_{HIGH}	SCL HIGH time		0.6	–	µs
t_r	SCL and SDA rise time	note 3	$20 + 0.1C_b$	300	ns
t_f	SCL and SDA fall time	note 3	$20 + 0.1C_b$	300	ns
$t_{SU;DAT}$	data set-up time		100	–	ns
$t_{HD;DAT}$	data hold time		0	–	ns
$t_{SU;STO}$	STOP condition set-up time		0.6	–	µs
C_b	capacitive load represented by each bus line		–	400	pF

Notes

1. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
2. The device inputs SDA and SCL are filtered and will reject spikes on the bus lines of widths less than $t_{SW(max)}$.
3. The rise and fall times specified here refer to the driver device (PCF8575) and are part of the general fast I²C-bus specification when PCF8575 asserts an acknowledge on SDA, the minimum fall time is 20 ns + $0.1C_b$.

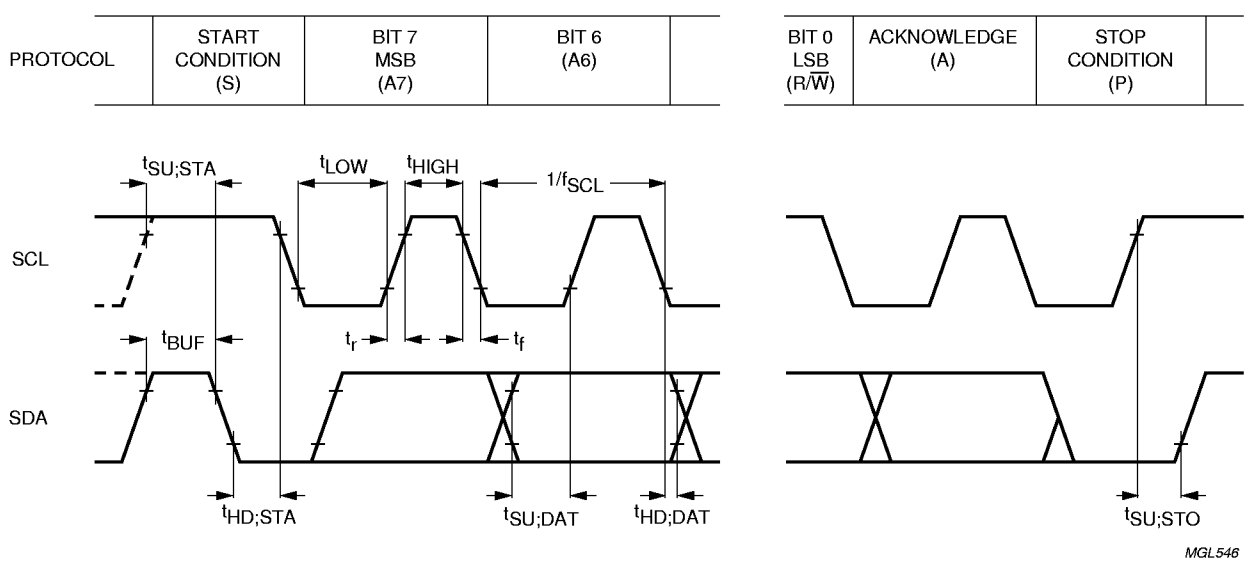


Fig.13 I²C-bus timing diagram.

12 DEVICE PROTECTION

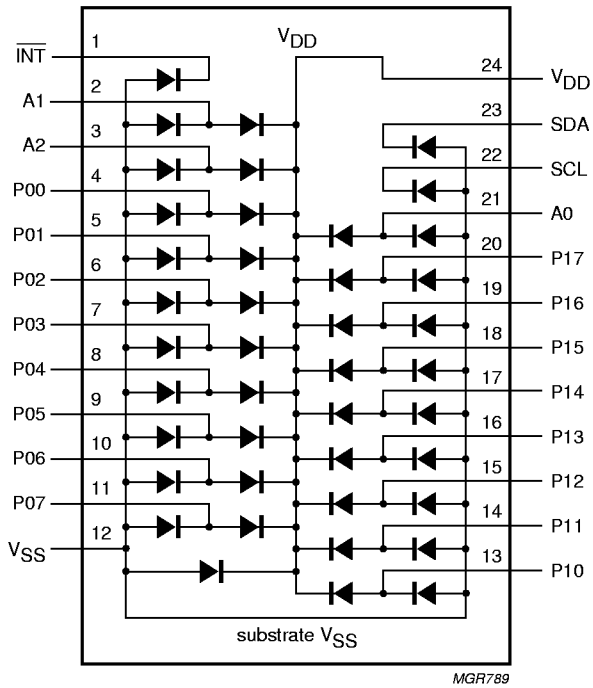
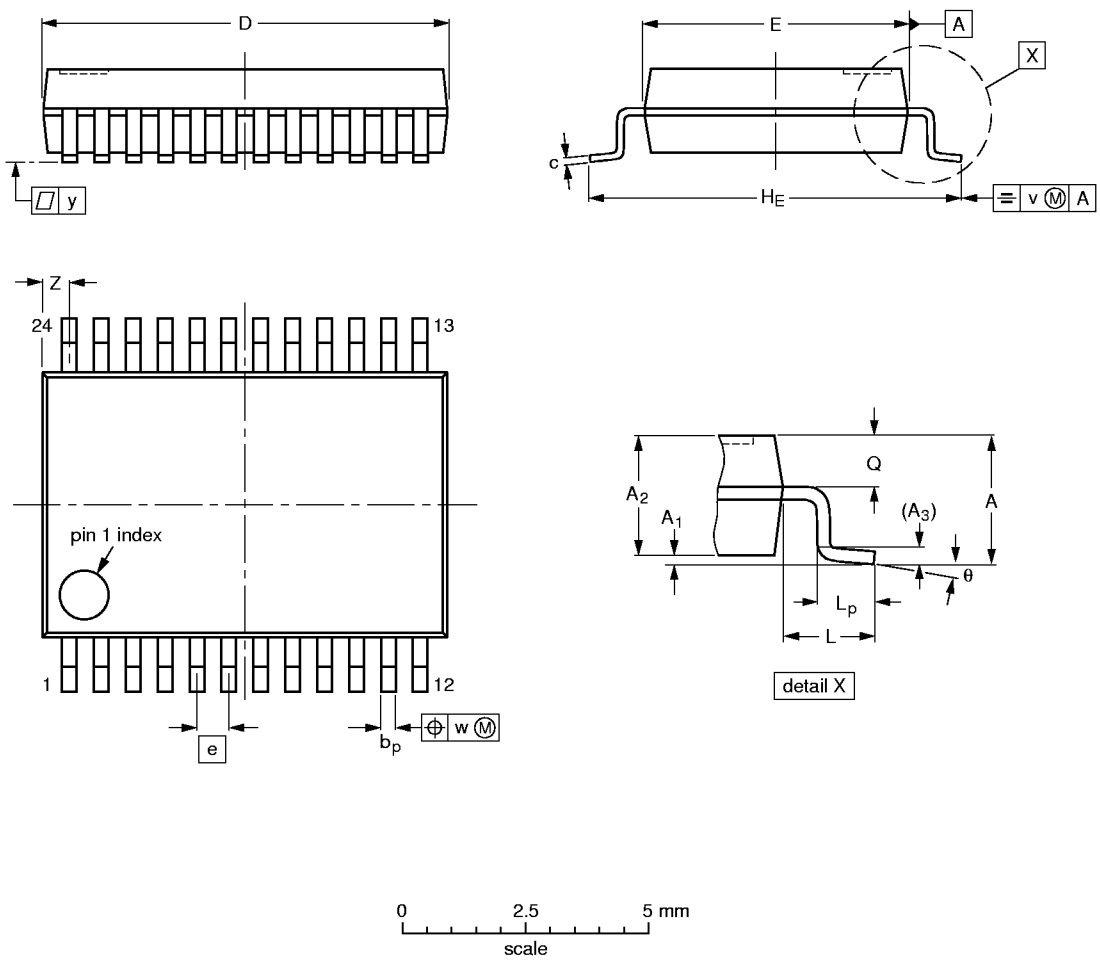


Fig.14 Device protection diagram.

13 PACKAGE OUTLINE

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

14 SOLDERING

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

14.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
HLQFP, HSQFP, HSOP, SMS	not suitable[2]	suitable
PLCC[3], SO	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SQFP	not suitable	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

15 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

16 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

17 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.