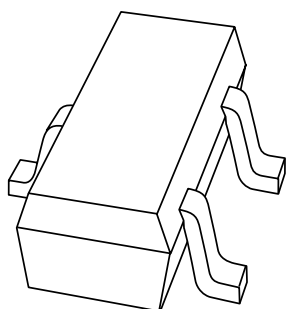


DATA SHEET



PUTC115EE

NPN resistor-equipped transistor;
 $R1 = 100\text{ k}\Omega$, $R2 = 100\text{ k}\Omega$

Product specification

2002 May 08

NPN resistor-equipped transistor;
R1 = 100 kΩ, R2 = 100 kΩ

PDTC115EE

FEATURES

- Built-in bias resistors R1 and R2 (typically 100 kΩ each)
- Simplification of circuit design
- Reduces number of components and required PCB area.

APPLICATIONS

- Especially suitable for space reduction in interface and driver circuits
- Inverter circuit configuration without use of external resistors.

DESCRIPTION

NPN resistor-equipped transistor in a SOT416 (SC-75) plastic package.

MARKING

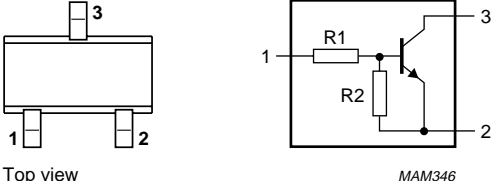
TYPE NUMBER	MARKING CODE
PDTC115EE	46

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V _{CEO}	collector-emitter voltage	50	V
I _O	output current (DC)	20	mA
R1	bias resistor	100	kΩ
R2	bias resistor	100	kΩ

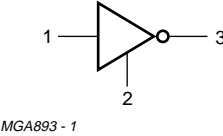
PINNING

PIN	DESCRIPTION
1	base/input
2	emitter/ground
3	collector/output



The figure shows two representations of the PDTC115EE transistor. On the left is a 'Top view' of the SOT416 (SC-75) plastic package, a small rectangular component with three pins labeled 1, 2, and 3. On the right is the circuit symbol, which depicts an NPN transistor with a base (pin 1), emitter (pin 2), and collector (pin 3). Two resistors, R1 and R2, are shown connected to the base and emitter respectively. The symbol is labeled 'MAM346'.

Fig.1 Simplified outline (SOT416) and symbol.



The figure shows the equivalent inverter symbol for the PDTC115EE transistor. It consists of a triangle with an input pin 1, an output pin 3, and a feedback pin 2. The symbol is labeled 'MGA893 - 1'.

Fig.2 Equivalent inverter symbol.

NPN resistor-equipped transistor; R1 = 100 k Ω , R2 = 100 k Ω

PDTC115EE

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	–	50	V
V _{CEO}	collector-emitter voltage	open base	–	50	V
V _{EBO}	emitter-base voltage	open collector	–	10	V
V _i	input voltage				
	positive		–	+40	V
	negative		–	–10	V
I _O	output current (DC)		–	20	mA
I _{CM}	peak collector current		–	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; note 1	–	150	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C

Note

1. Refer to standard SOT416 (SC-75) mounting conditions.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient	in free air; note 1	833	K/W

Note

1. Refer to standard SOT416 (SC-75) mounting conditions.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{CBO}	collector-base cut-off current	V _{CB} = 50 V; I _E = 0	–	–	100	nA
I _{CEO}	collector-emitter cut-off current	V _{CE} = 30 V; I _B = 0	–	–	1	μA
		V _{CE} = 30 V; I _B = 0; T _j = 150 °C	–	–	50	μA
I _{EBO}	emitter-base cut-off current	V _{EB} = 5 V; I _C = 0	–	–	50	μA
h _{FE}	DC current gain	V _{CE} = 5 V; I _C = 5 mA	80	–	–	
V _{CEsat}	collector-emitter saturation voltage	I _C = 300 mA; I _B = 10 mA	–	–	150	mV
V _{i(off)}	input off voltage	V _{CE} = 5 V; I _C = 100 μA	–	–	0.5	V
V _{i(on)}	input on voltage	V _{CE} = 0.3 V; I _C = 1 mA	3	–	–	V
R1	input resistor		70	100	130	k Ω
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	
C _c	collector capacitance	I _E = I _e = 0; V _{CB} = 10 V; f = 1 MHz	–	–	2.5	pF

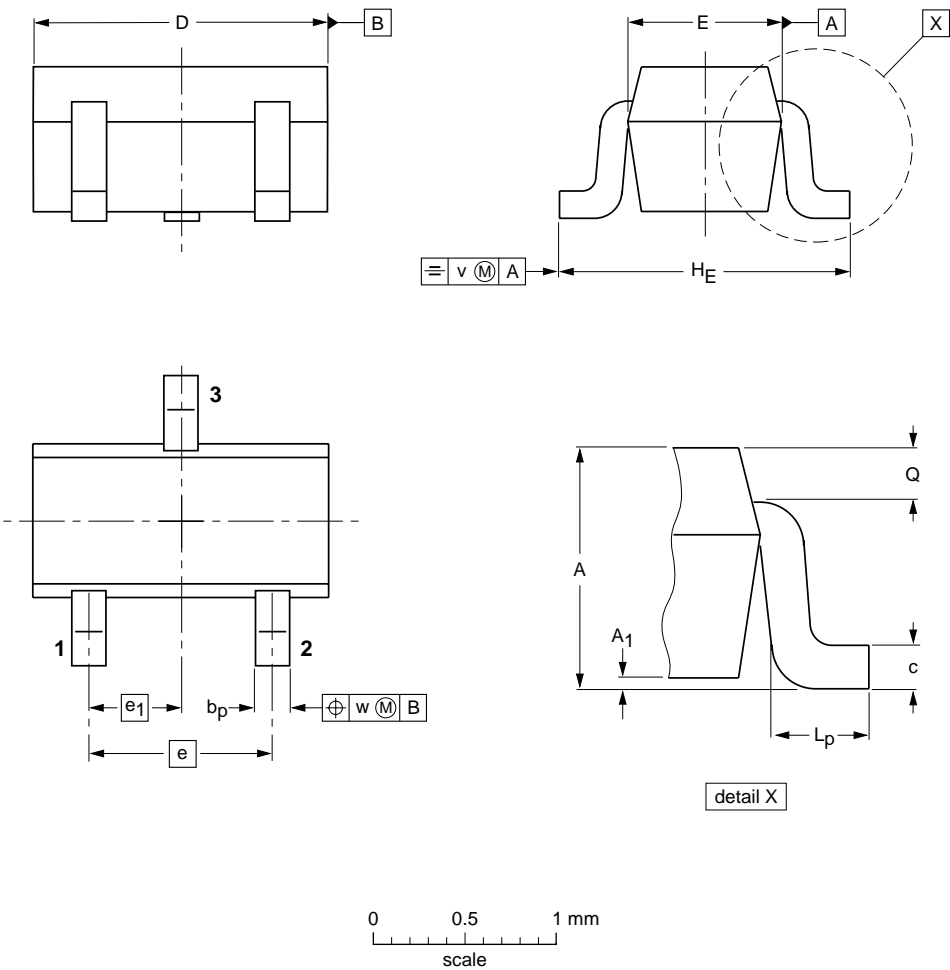
NPN resistor-equipped transistor;
R1 = 100 kΩ, R2 = 100 kΩ

PDTC115EE

PACKAGE OUTLINE

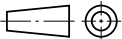
Plastic surface mounted package; 3 leads

SOT416



DIMENSIONS (mm are the original dimensions)

UNIT	A	A1 max	bp	c	D	E	e	e1	HE	Lp	Q	v	w
mm	0.95 0.60	0.1	0.30 0.15	0.25 0.10	1.8 1.4	0.9 0.7	1	0.5	1.75 1.45	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT416			SC-75			97-02-28

NPN resistor-equipped transistor;
R1 = 100 k Ω , R2 = 100 k Ω

PDTC115EE

DATA SHEET STATUS

DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
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PDTC115EE

NOTES

NPN resistor-equipped transistor;
R1 = 100 k Ω , R2 = 100 k Ω

PDTC115EE

NOTES

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