DATA SHEET

CX77301: PA Module Dual-band EGSM900 DCS1800 / GPRS

APPLICATIONS

- Dual-band cellular handsets encompassing
  - Class 4 EGSM900,
  - Class 1 DCS1800
  - up to Class 10 GPRS multi-slot operation.

FEATURES

- High efficiency
  - EGSM 55%
  - DCS 50%
- Input/output matching
  - 50 Ω internal
- Small outline 9.1 mm x 11.6 mm
- Low profile 1.5 mm maximum
- Low APC current 10 µA typical

The CX77301 is a dual-band Power Amplifier Module (PAM) designed in a compact form factor for Class 4 EGSM900 and Class 1 DCS1800 operation that also supports multi-slot transmission for Class 10 General Packet Radio Service (GPRS) operation.

The module consists of an EGSM900 PA block, a DCS1800 PA block, impedance matching circuitry for 50 Ω input and output impedances, and bias control circuitry. Two separate Heterojunction Bipolar Transistor (HBT) PA blocks are fabricated on a single Gallium Arsenide (GaAs) die. One PA block operates in the EGSM900 band and the other PA block supports the DCS1800 band. Optimized for lithium ion battery operation, both PA blocks share common power supply pins to distribute current. A custom CMOS integrated circuit provides the internal interface circuitry, including a current amplifier that minimizes the required power control current (I_{APC}) to 10 µA, typical. The GaAs die, the Silicon (Si) die, and passive components are mounted on a multi-layer laminate substrate. The assembly is encapsulated with plastic overmold.

The RF input and output ports are internally matched to 50 Ω to reduce the number of external components for a dual-band design. Extremely low leakage current (2 µA, typical) of the dual PA module maximizes handset standby time. The CX77301 also contains band-select switching circuitry to select EGSM (logic 0) or DCS (logic 1) as determined from the Band Select (BS) signal. In the Functional Block Diagram shown below, the BS pin selects the PA output (DCS OUT or EGSM OUT) while the Analog Power Control (APC) controls the level of output power.

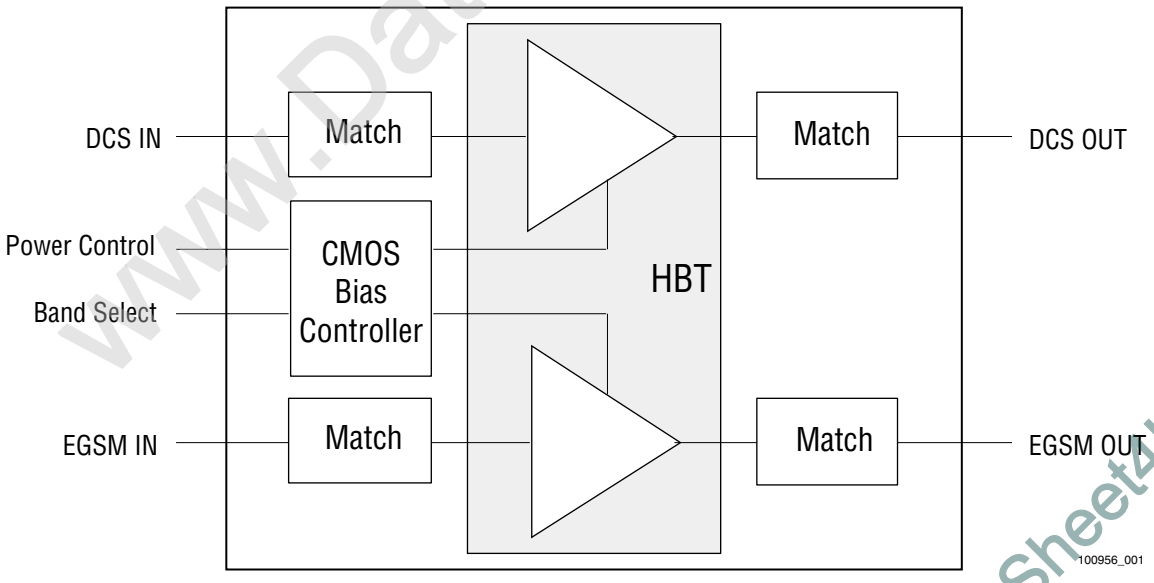


Figure 1. Functional Block Diagram

ELECTRICAL SPECIFICATIONS

The following tables list the electrical characteristics of the CX77301 Power Amplifier. Table 1 lists the absolute maximum ratings and Table 2 shows the recommended operating conditions. Table 3 shows the electrical characteristics of the CX77301 for EGSM and DSC modes. A typical CX77301 application diagram appears in Figure 2.

The CX77301 is a static-sensitive electronic device and should not be stored or operated near strong electrostatic fields. Detailed ESD precautions along with information on device dimensions, pin descriptions, packaging and handling can be found in later sections of this data sheet.

Table 1. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Input power (P_{IN})	—	15	dBm
Supply voltage (V_{CC}), standby, $V_{APC} \leq 0.3$ V	—	7	V
Control voltage (V_{APC})	–0.5	V_{CC_MAX} – 0.2 (See Table 3)	V
Storage Temperature	–55	+100	°C

Table 2. CX77301 Recommended Operating Conditions

Parameter	Minimum	Typical	Maximum	Unit
Supply Voltage (V_{CC})	2.9	3.5	4.8 V[1]	V
Supply Current (I_{CC})	0	—	2.5[1]	A
Operating Case Temperature (T_{CASE})				
1-Slot (12.5% duty cycle)	–20	—	100	°C
2-Slot (25% duty cycle)	–20	—	90	
3-Slot (37.5% duty cycle)	–20	—	75	
4-Slot (50% duty cycle)	–20	—	60	

[1] For charging conditions with $V_{CC} > 4.8$ V, derate I_{CC} linearly down to 0.5 A max at $V_{CC} = 5.5$ V

Table 3. CX77301 Electrical Specifications(1) (1 of 3)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
General						
Supply Voltage	V_{CC}	—	2.9	3.5	4.8V	V
Power Control Current	I_{APC}	—	—	10	100	µA
Leakage Current	I_Q	V_{CC} = 4.5 V V_{APC} = 0.3 V T_{CASE} = +25 °C $P_{IN} \leq$ –60 dBm	—	—	5	µA
APC Enable Threshold	V_{APCTH}	—	200	—	600	mV
APC Enable Switching Delay	τ_{SW}	Time from $V_{APC} \geq V_{APCTH}$ until $P_{OUT} \leq (P_{OUT\_FINAL}$ –3 dB)	5		8	µs
EGSM Mode (f = 880 to 915 MHz and P_{IN} = 6 to 12 dBm)						
Frequency Range	f	—	880	—	915	MHz
Input Power	P_{IN}	—	6	—	12	dBm
Analog Power Control Voltage	V_{APC}	P_{OUT} = 32 dBm	1.2	1.7	2.1	V
Power Added Efficiency	PAE	V_{CC} = 3.5 V $P_{OUT} \geq$ 34.5 dBm $V_{APC} \approx$ 2.0 V pulse width = 577 µs duty cycle = 1:8 T_{CASE} = +25 °C	50	55	—	%
2nd to 13th Harmonics	2f0 to 13f0	BW = 3 MHz 5 dBm $\leq P_{OUT} \leq$ 35 dBm	—	—	–7	dBm
Output Power	P_{OUT}	V_{CC} = 3.5 V $V_{APC} \approx$ 2.0 V T_{CASE} = +25 °C	34.5	35.0	—	dBm
	$P_{OUT\ MAX}$	V_{CC} = 2.9 V $V_{APC} \leq$ 2.6 V T_{CASE} = –20 °C to +100 °C (See Table 2 for multi-slot) P_{IN} = 6 dBm	32	33	—	
	$P_{OUT\ MAX}$	V_{CC} = 4.8 V $V_{APC} \leq$ 2.6 V T_{CASE} = –20 °C to +100 °C (See Table 2 for multi-slot) P_{IN} = 6 dBm	32	33	—	
Input VSWR	Γ_{IN}	P_{OUT} = 5 to 35 dBm, controlled by V_{APC}	—	1.5:1	2:1	—
Forward Isolation	$P_{OUT\ STANDBY}$	P_{IN} = 12 dBm V_{APC} = 0.3 V	—	–35	–30	dBm
Switching Time	τ_{RISE}, τ_{FALL}	Time from P_{OUT} = –10 dBm to P_{OUT} = +5 dBm, $\tau \approx$ 90%	—	5	8	µs
		Time from P_{OUT} = –10 dBm to P_{OUT} = +20 dBm, $\tau \approx$ 90%	—	5	8	
		Time from P_{OUT} = –10 dBm to P_{OUT} = +34.5 dBm, $\tau \approx$ 90%	—	2	4	

Table 3. CX77301 Electrical Specifications(1) (2 of 3)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Spurious	Spur	All combinations of the following parameters: V_{APC} = Controlled (2) P_{IN} = Min. to Max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 8:1, all phase angles	No parasitic oscillation > –36 dBm			
Load Mismatch	Load	All combinations of the following parameters: V_{APC} = Controlled (2) P_{IN} = Min. to Max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 10:1, all phase angles	No module damage or permanent degradation			
Noise Power	P_{NOISE}	At f0 + 20 MHz: RBW = 100 kHz V_{CC} = 3.5 V 5 dBm ≤ P_{OUT} ≤ 34.5 dBm	—	—	–82	dBm
		At f0 + 10 MHz: RBW = 100 kHz V_{CC} = 3.5 V 5 dBm ≤ P_{OUT} ≤ 34.5 dBm	—	—	–76	
		At 1805 to 1880 MHz: RBW = 100 kHz V_{CC} = 3.5 V 5 dBm ≤ P_{OUT} ≤ 34.5 dBm	—	—	–90	
Coupling of 2nd and 3rd Harmonic from the EGSM Band into the DCS Band	2f0, 3f0	Measured at the DCS output, –15 dBm ≤ P_{OUT} ≤ 34 dBm	—	–25	–20	dBm
DCS Mode (f = 1710 to 1785 MHz and P_{IN} = 5 to 11 dBm)						
Frequency Range	f	—	1710	—	1785	MHz
Input Power	P_{IN}	—	5	—	11	dBm
Analog Power Control Voltage	V_{APC}	P_{OUT} = 29.5 dBm	1.35	1.7	2.1	V
Power Added Efficiency	PAE	V_{CC} = 3.5 V P_{OUT} ≥ 31.5 dBm V_{APC} ≈ 2.0 V pulse width = 577 µs duty cycle = 1:8 T_{CASE} = +25 °C	45	50	—	%
2nd to 7th Harmonics	2f0 to 7f0	BW = 3 MHz 0 dBm ≤ P_{OUT} ≤ 32 dBm	—	—	–7	DBm
Output Power	P_{OUT}	V_{CC} = 3.5 V V_{APC} ≈ 2.0 V T_{CASE} = +25 °C	31.5	32.0	—	DBm
	$P_{OUT\ MAX}$	V_{CC} = 2.9 V V_{APC} ≤ 2.6 V T_{CASE} = –20 °C to +100 °C (See Table 2 for multi-slot) P_{IN} = 5 dBm	29.5	30.5	—	
	$P_{OUT\ MAX}$	V_{CC} = 4.8 V V_{APC} ≤ 2.6 V T_{CASE} = –20 °C to +100 °C (See Table 2 for multi-slot) P_{IN} = 5 dBm	29.5	30.5	—	

Table 3. CX77301 Electrical Specifications(1) (3 of 3)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Input VSWR	Γ_{IN}	P_{OUT} = 0 to 32 dBm, controlled by V_{APC}	—	—	2:1	—
Forward Isolation	$P_{OUT\ STANDBY}$	P_{IN} = 10.5 dBm V_{APC} = 0.3 V	—	–40	–35	dBm
Switching Time	τ_{RISE}, τ_{FALL}	Time from P_{OUT} = –10 dBm to P_{OUT} = 0 dBm, $\tau \approx$ 90%	—	10	12	µs
		Time from P_{OUT} = –10 dBm to P_{OUT} = +20 dBm, $\tau \approx$ 90%	—	5	8	
		Time from P_{OUT} = –10 dBm to P_{OUT} = +31.5 dBm, $\tau \approx$ 90%	—	2	5	
Spurious	Spur	All combinations of the following parameters: V_{APC} = Controlled (3) P_{IN} = min. to max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 8:1, all phase angles	No parasitic oscillation > –36 dBm			
Load Mismatch	Load	All combinations of the following parameters: V_{APC} = Controlled (3) P_{IN} = Min. to Max. V_{CC} = 2.9 V to 4.8 V Load VSWR = 10:1, all phase angles	No module damage or permanent degradation			
Noise Power	P_{NOISE}	At f0 + 20 MHz: RBW = 100 kHz V_{CC} = 3.5 V 0 dBm ≤ P_{OUT} ≤ 31.5 dBm	—	—	–80	dBm
		At 925 to 960 MHz: RBW = 100 kHz V_{CC} = 3.5 V 0 dBm ≤ P_{OUT} ≤ 31.5 dBm	—	—	–95	

(1) Unless specified otherwise: T_{CASE} = –20 °C to maximum operating temperature (see Table 2), RL = 50 Ω, pulsed operation with pulse width ≤ 2308 µs, duty cycle ≤ 4:8, V_{CC} = 2.9 V to 4.8 V

(2) I_C = 0A to xA, where x = current at P_{OUT} = 34.5 dBm, 50 Ω load, and V_{CC} = 3.5 V.

(3) I_C = 0A to xA, where x = current at P_{OUT} = 32.0 dBm, 50 Ω load, and V_{CC} = 3.5 V.

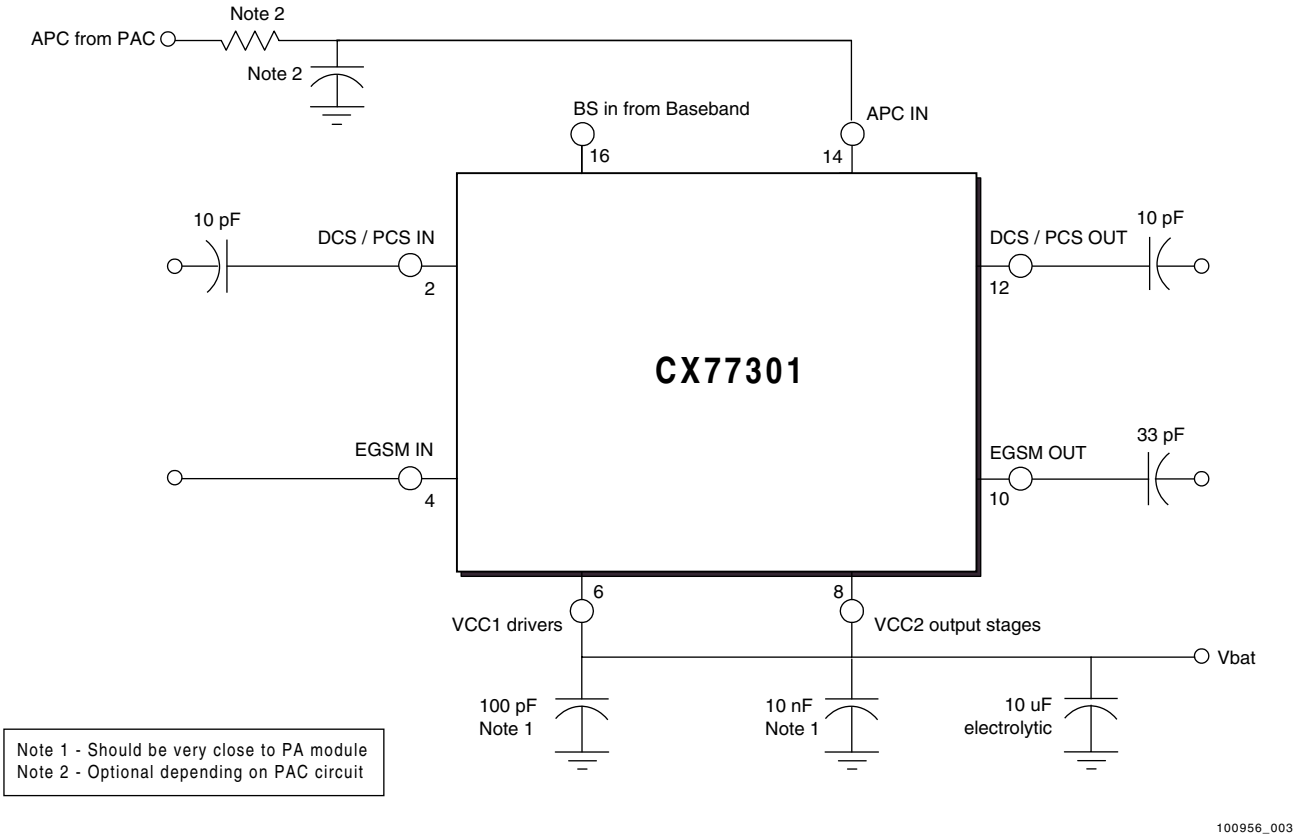
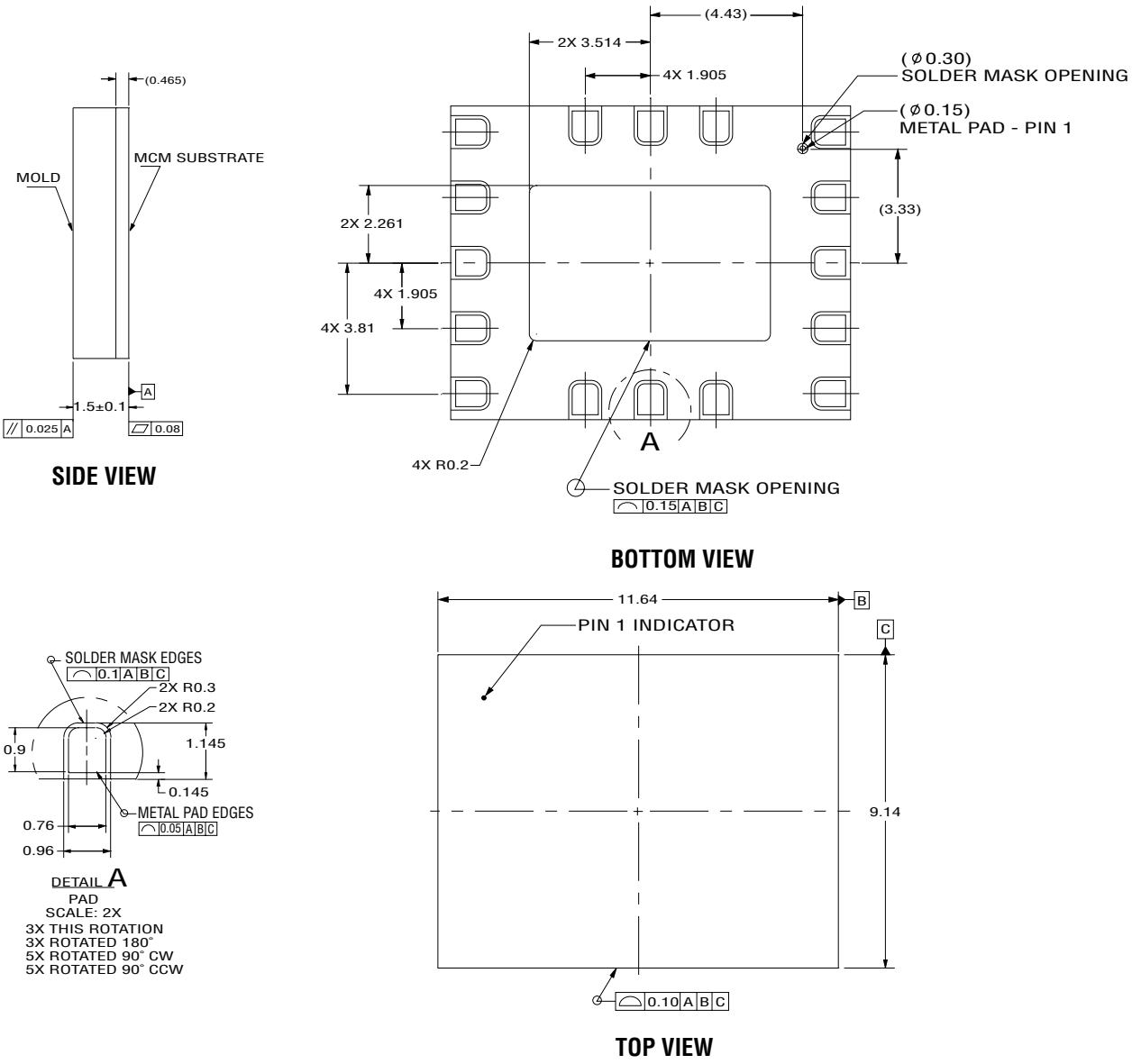


Figure 2. Typical CX77301 Application

PACKAGE DIMENSIONS AND PIN DESCRIPTIONS

Figure 3 displays the dimensions of the 16-pin leadless CX77301 dual-band PAM. Figure 4 provides a recommended phone board layout footprint for the PAM to help the designer attain optimum thermal conductivity, good grounding, and minimum RF discontinuity for the 50 ohm terminals. Figure 5 shows the device pin configuration, and Table 4 describes the pin names and signals.



NOTES: unless otherwise specified
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING IN ACCORDANCE WITH ASME Y14.5M–1994
3. SEE APPLICABLE BONDING DIAGRAM AND DEVICE ASSEMBLY DRAWING FOR DIE AND COMPONENT PLACEMENT.
4. PADS ARE METAL DEFINED. THE CENTER PAD IS SOLDER MASK DEFINED.

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Figure 3. CX77301 Package Dimensions–16-pin Module (All Views)

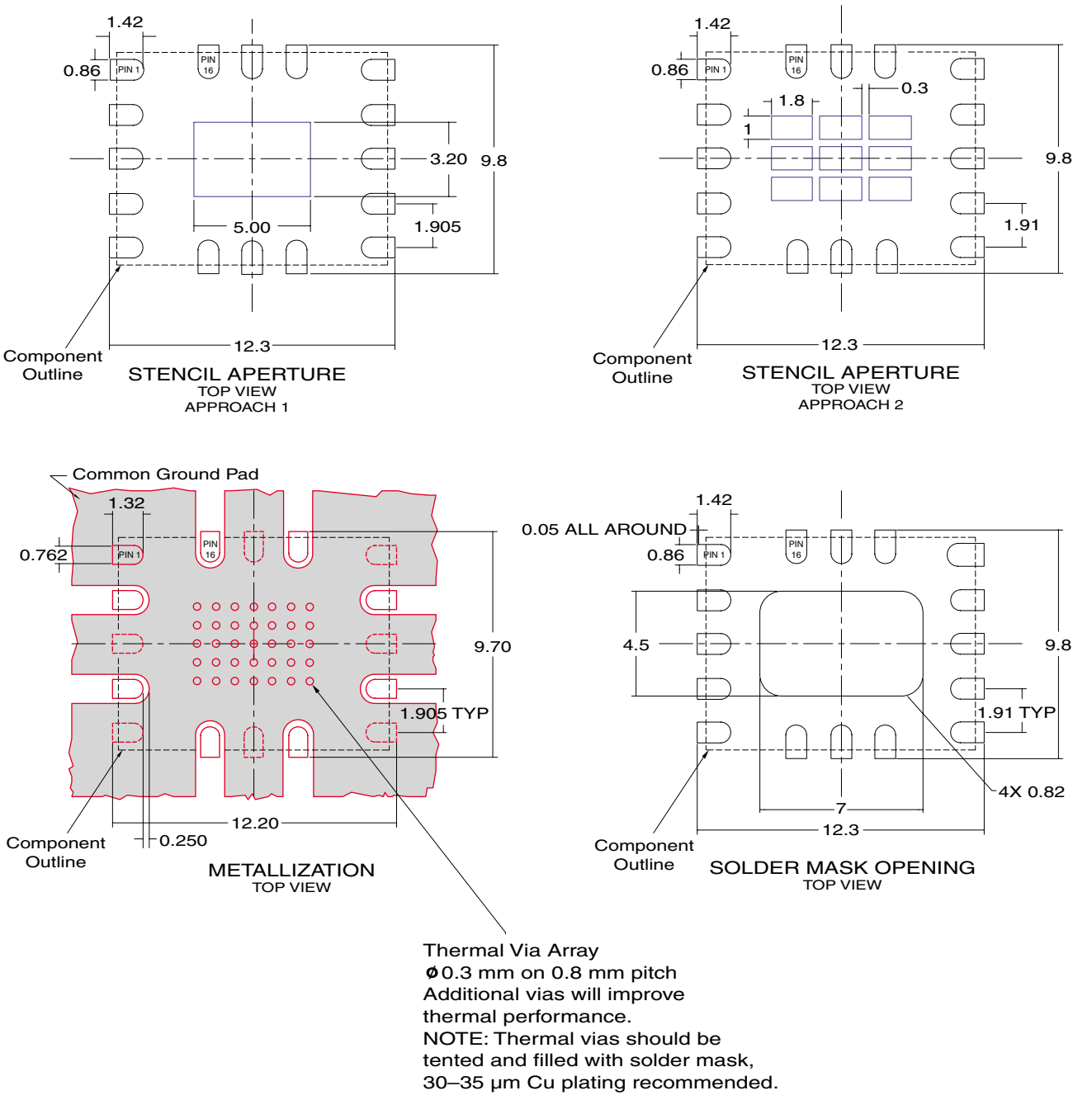

Figure 4. Phone Board Layout Footprint for 9.1 mm x 11.6 mm Package

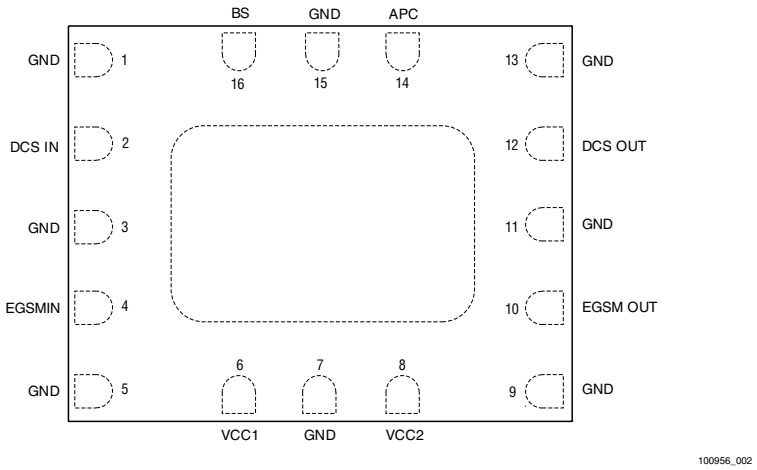

Figure 5. CX77301 Package and Pin Configuration (Top View)

Table 4. CX77301 Pin Names and Signal Descriptions

Pin	Name	Description
1	GND	Ground
2	DCS IN	RF input to DCS PA (DC coupled)
3	GND	Ground
4	EGSM IN	RF input to EGSM PA
5	GND	Ground
6	VCC1	Power supply for PA driver stages
7	GND	Ground
8	VCC2	Power supply for PA output stages
9	GND	Ground
10	EGSM OUT	EGSM RF output (DC coupled)
11	GND	Ground
12	DCS OUT	DCS RF output (DC coupled)
13	GND	Ground
14	APC	Analog Power Control
15	GND	Ground
16	BS	Band select

PACKAGE AND HANDLING INFORMATION

Because of its sensitivity to moisture absorption, this device package is baked and vacuum packed prior to shipment. Instructions on the shipping container label must be followed regarding exposure to moisture after the container seal is broken, otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY77301 is capable of withstanding an MSL 3/240 °C solder reflow. Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. If the part is attached in a reflow oven, the temperature ramp rate should not exceed 5 °C per second; maximum temperature should not exceed 240 °C. If the part is manually attached, precaution should be taken to insure that the part is not subjected to temperatures exceeding 240 °C for more than 10 seconds. For details on attachment techniques, precautions, and handling procedures recommended by Skyworks, please refer to *Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752*. Additional information on standard SMT reflow profiles can also be found in the *JEDEC Standard J–STD–020B*.

Production quantities of this product are shipped in the standard tape-and-reel format. For packaging details, refer to *Application Note: Tape and Reel, Document Number 101568.*

ELECTROSTATIC DISCHARGE SENSITIVITY

The CX77301 is a Class I device. Figure 6 lists the Electrostatic Discharge (ESD) immunity level for each pin of the CX77301 product. The numbers for each pin in Figure 6 specify the ESD threshold level where the I-V curve between the pin and ground starts to show degradation. If ESD damage threshold magnitude is found to consistently exceed 2000 volts on a given pin, this so is indicated. If ESD damage threshold below 2000 volts is measured for either polarity, numbers are indicated that represent worst case values observed in product characterization.

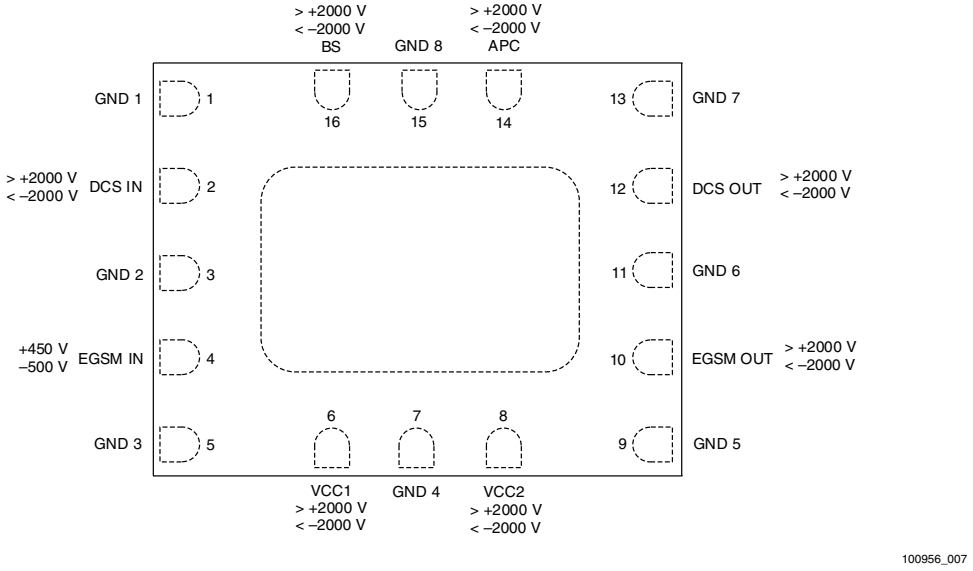

Figure 6. ESD Sensitivity Areas (Top View)

Various failure criteria can be utilized when performing ESD testing. Many vendors employ relaxed ESD failure standards which fail devices only after “the pin fails the electrical specification limits” or “the pin becomes completely non-functional”. Skyworks employs most stringent criteria, fails devices as soon as the pin begins to show any degradation on a curve tracer.

To avoid ESD damage, both latent and visible, it is very important that the product assembly and test areas follow the Class-1 ESD handling precautions listed in

Table 5.

Table 5. Precautions for Handling GaAs IC-based Products to Avoid Induced Damage

Personnel Grounding	Facility
Wrist Straps Conductive Smocks, Gloves and Finger Cots Antistatic ID Badges	Relative Humidity Control and Air Ionizers Dissipative Floors (less than 10^9 Ω to GND)
Protective Workstation	**Protective Packaging & Transportation**
Dissipative Table Tops Protective Test Equipment (Properly Grounded) Grounded Tip Soldering Irons Conductive Solder Suckers Static Sensors	Bags and Pouches (Faraday Shield) Protective Tote Boxes (Conductive Static Shielding) Protective Trays Grounded Carts Protective Work Order Holders

TECHNICAL INFORMATION

CMOS Bias Controller Characteristics

The CMOS die within the PAM performs several functions that are important to the overall module performance. Some of these functions must be considered for development of the power ramping features in a 3GPP compliant transmitter power control loop.

Please refer to 3GPP TS 05.05, Digital Cellular Communications System (Phase 2+); Radio Transmission and Reception. All GSM specifications are now the responsibility of 3GPP.

The standards are available at http://www.3GPP.org/specs/specs.htm.

Power ramping considerations will be discussed later in this section. The four main functions that will be described in this section are Standby Mode Control, Band Select, Voltage Clamp, and Current Buffer. The functional block diagram is shown in Figure 7.

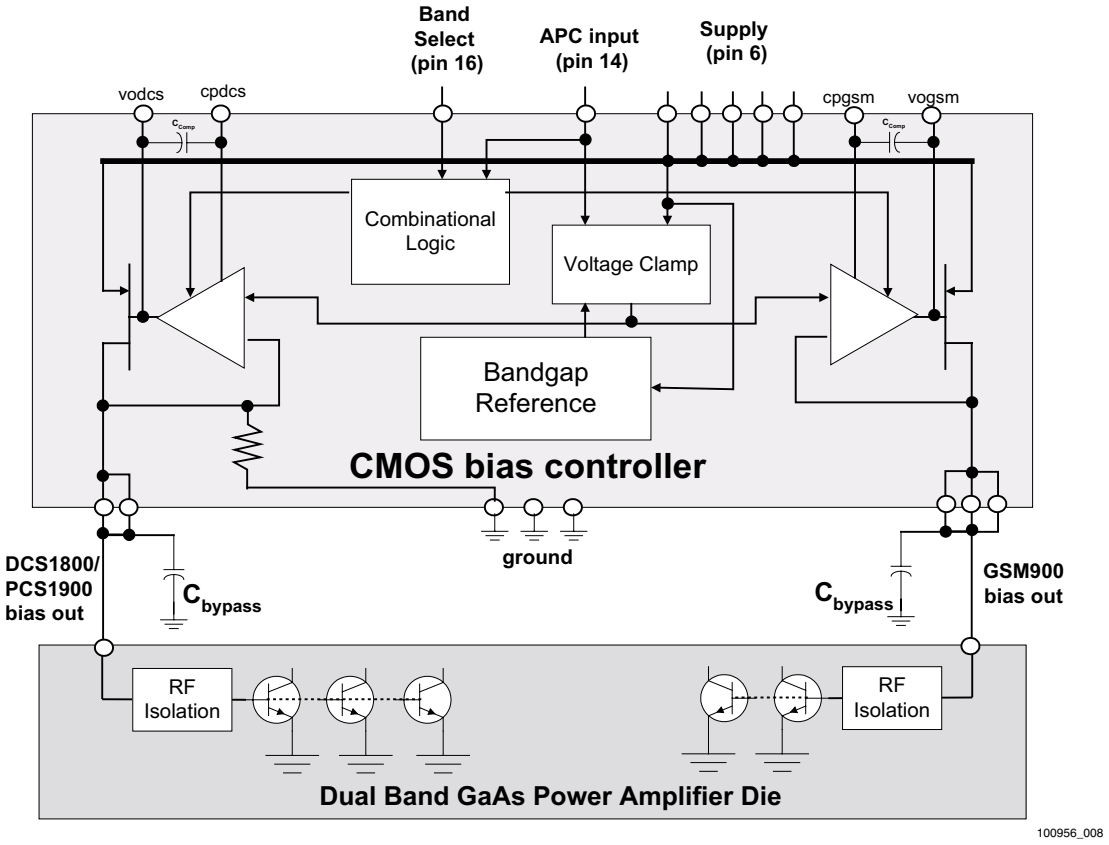

Figure 7. Functional Block Diagram

Standby Mode Control

The Combinational Logic cell includes enable circuitry that monitors the APC ramping voltage from the power amplifier controller (PAC) circuit in the GSM transmitter. Typical handset designs directly connect the PA V_{CC} to the battery at all times, and for some PA manufacturers this requires a control signal to set the device in or out of standby mode. The Skyworks PAM does not require a Transmit Enable input because it contains a standby detection circuit that senses the V_{APC} to enable or disable the PA. This feature helps minimize battery discharge when the PA is in standby mode. When V_{APC} is below the enable threshold voltage, the PA goes into a standby mode, which reduces battery current (I_{CC}) to 6 µA, typical, under nominal conditions.

For voltages less than 700 mV at the APC input (pin 14), the PA bias is held at ground. As the APC input exceeds the enable threshold, the bias will activate. After an 8 µs delay, the amplifier internal bias will ramp quickly to match the ramp voltage applied to the APC input. In order for the internal bias to precisely follow the APC ramping voltage, it is critical that a ramp pedestal is set to the APC input at or above the enable threshold level with a timing at least 8 µs prior to ramp-up. This will be discussed in more detail in the following section, “Power Ramping Considerations for 3GPP Compliance”.

Band Select

The Combinational Logic cell also includes a simple gate arrangement that selects the desired operational band by activating the appropriate current buffer. The voltage threshold level at the Band Select input (pin 16) will determine the active path of the bias output to the GaAs die.

Voltage Clamp

The Voltage Clamp circuit will limit the maximum bias voltage output applied to the bases of the HBT devices on the GaAs die. This provides protection against electrical overstress (EOS) of the active devices during high voltage and/or load mismatch conditions. Figure 8 shows the typical transfer function of the APC input to buffer output under resistively loaded conditions. Notice the enable function near 600 mV, and the clamp acting at 2.15 V, corresponding to a supply voltage of 4.0 V.

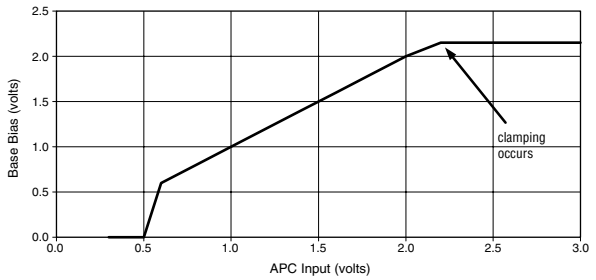

Figure 8. Base Bias Voltage vs. APC Input, V_{CC} = 4.0 V

Due to output impedance effects, the bias of the GaAs devices increases as the supply voltage increases. The Voltage Clamp is designed to gradually decrease in level as the battery voltage increases. The performance of the clamp circuit is enhanced by the band gap reference that provides a supply-, process-, and temperature-independent reference voltage. The transfer function relative to V_{BAT} is shown in Figure 9. For battery voltages below 3.4 V, the base bias voltage is limited by the common mode range of the buffer amplifier. For battery voltages above 3.4 V, the clamp limits the base bias.

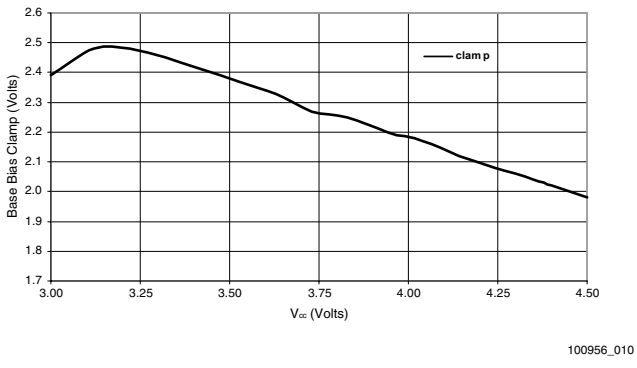

Figure 9. Base Bias Clamp vs. Supply Voltage

Current Buffer

The output buffer amplifier performs a vital function in the CMOS device by transferring the APC input voltage ramp to the base of the GaAs power devices. This allows the APC input to be a high impedance port, sinking only 10 µA, typical, assuring no loading effects on the PAC circuit. The buffers are designed to source the high GaAs base currents required, while allowing a settling time of less than 8 µs for a 1.5 V ramp.

POWER RAMPING CONSIDERATIONS FOR 3GPP COMPLIANCE

These are the primary variables in the power control loop that the system designer must control:

- software control of the DSP / DAC
- software control of the transmitter timing signals
- ramp profile attributes - pedestal, number of steps, duration of steps
- layout of circuit / parasitics
- RC time constants within the PAC circuit design

All of these variables will directly influence the ability of a GSM transmitter power control loop to comply with 3GPP specifications.

Although there is a specific time mask template in which the transmitter power is allowed to ramp up, the method is very critical. The 3GPP system specification for switching transients results in a requirement to limit the edge rate of output power transitions of the mobile. Switching transients are caused by the transition from minimum output power to the desired output power, and vice versa. The spectrum generated by this transition is due to the ramping waveform amplitude modulation imposed on the carrier. Sharper transitions tend to produce more spectral "splatter" than smooth transitions. If the transmit output power is ramped up too slowly, the radio will violate the time mask specification. In this condition, the radio may not successfully initiate or maintain a phone call. If the transmit output power is ramped up too quickly, this will cause RF "splatter" at certain frequency offsets from the carrier as dictated by the 3GPP specification. This splatter, known as Output RF Spectrum (ORFS) due to Switching Transients, will increase the system noise level, which may knock out other users on the system. The main difficulty with TDMA power control is allowing the transmitter to ramp the output power up and down gradually so switching transients are not compromised while meeting the time mask template at all output power levels in all operational bands. The transmitter has 28 µs to ramp up power from an off state to the desired power level.

The GSM transmitter power control loop generally involves feedback around the GaAs PA, which limits the bandwidth of signals that can be applied to the PA bias input. Since the PA is within the feedback loop, its own small-signal frequency response must exhibit a bandwidth 5 to 10 times that of the power control loop. As discussed in the previous section, the PA bias is held at ground for inputs less than 700 mV. As the APC input exceeds the enable threshold, the bias will activate. After

an 8 µs delay, the amplifier internal bias will quickly ramp to match the ramp voltage applied to the VAPC input. Since the bias must be wide band relative to the power control loop, the ramp will exhibit a fast edge rate. If the APC input increases beyond 1 volt before the 8 µs switching delay is allowed to occur after the bias is enabled, the PA will have significant RF output as the internal bias approaches the applied bias. During this ramp, the internal power control is running "open loop" and the edge rates are defined by the frequency response of the PA bias rather than that of the power control loop. This open loop condition will result in switching transients that are directly correlated to the PA bias bandwidth.

Application of an initial APC voltage, which enables the bias at least 8 µs before the VAPC voltage is ramped, will ensure that the internal bias of the PAM will directly follow the applied VAPC. As a result, the power control loop will define all edge transitions rather than the PA internal bandwidth defining the transition. Figure 10 and Figure 11 show the relationship of the internal bias relative to the applied APC in two cases. One case has ramping starting from ground; the other case has ramping starting with an initial enable pedestal of 700 mV. It is evident that the pedestal level is critical to ensure a predictable and well behaved power control loop.

To enable the CMOS driver in the PAM prior to ramp-up, a PAC output pedestal level to the APC input of the PAM (pin 14) should be set to about 700 mV. This pedestal level should have a duration of at least 8 µs directly prior to the start of ramp up.

Figure 12 shows typical signals and timings measured in a GSM transmitter power control loop. This particular example is at GSM Power Level 5, Channel 62. The oscilloscope traces are TxVCO_enable, PAC_enable, DAC Ramp, and VAPC (pin 14).

NOTE: When the TxVCO is enabled, the pedestal becomes set at the APC input of the PAM, then the PAC is enabled, and finally the DAC ramp begins.

The device specifications for enable threshold level and switching delay are shown in Table 3.

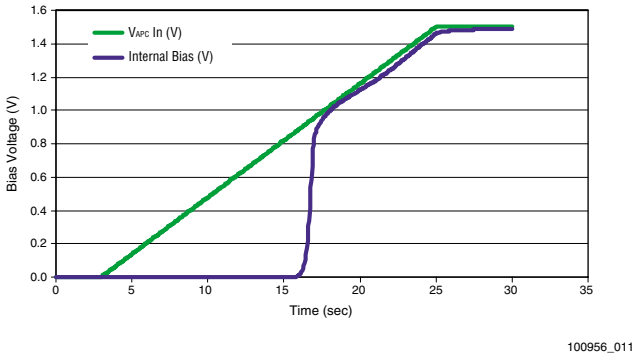

Figure 10. PAM Internal Bias Performance – No Pedestal Applied

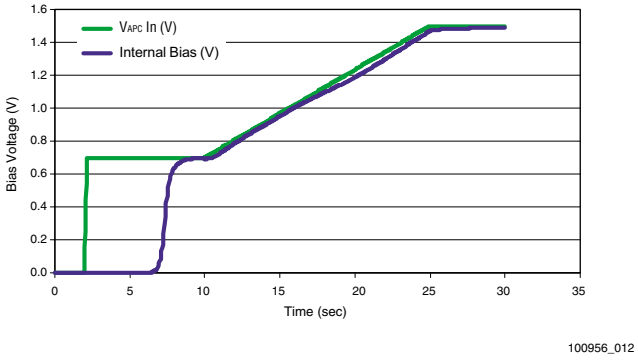

Figure 11. PAM Internal Bias Performance – Pedestal Applied

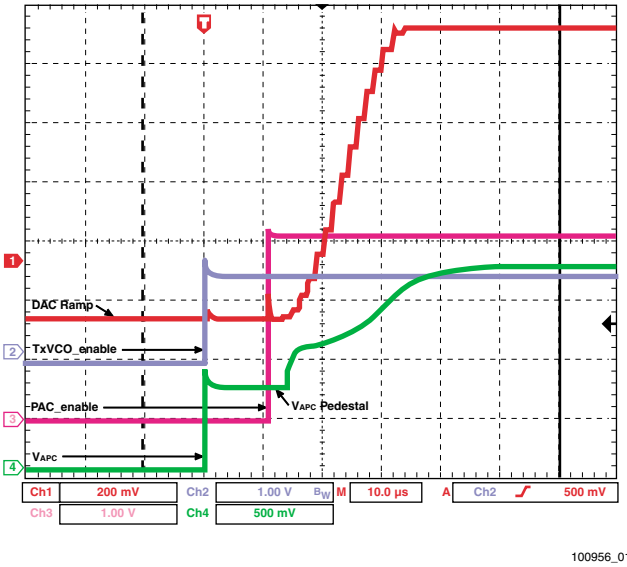

Figure 12. GSM Transmitter – Typical Ramp-up Signals

ORDERING INFORMATION

Model Number	Manufacturing Part Number	Product Revision	Package	Operating Temperature
CX77301	CX77301	–13	9.1 x 11.6 x 1.5 mm	–20 ×C to +100 ×C

REVISION HISTORY

Revision	Level	Date	Description
A		June 2000	Initial Release
B		January 2001	Add: Tables 3,4 Revise: Figure 4.
C		March 2001	Add: ESD data, revised format to add chapter headings
D		January 2, 2002	Add: Technical Information Section Revise: Functional Block Diagram; ESD data (+/– thresholds), Figure 10.
E		September 19, 2003	New format Add: Figure 4 Revise: Figures 3, 5, 6

REFERENCES

Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752
Application Note: Tape and Reel, Document Number 101568
JEDEC Standard J–STD–020B

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