LOW SKEW TTL PLL CLOCK DRIVER WITH INTEGRATED LOOP FILTER

QS5931T

FEATURES:

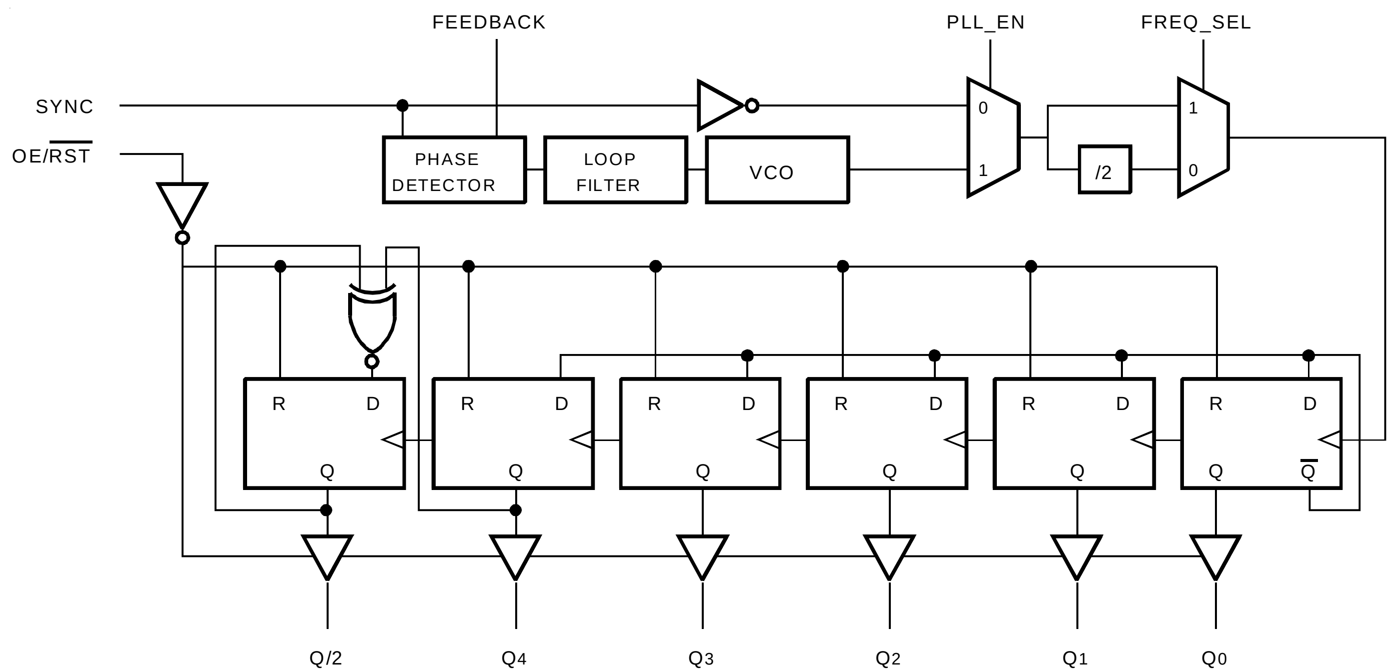
- **5V operation**
- **Six low noise TTL level outputs**
- **Q outputs, Q/2 output**
- **<250ps output skew, Q0–Q4**
- **Outputs 3-state and reset while OE/$\overline{\text{RST}}$ low**
- **PLL disable feature for low frequency testing**
- **Internal loop filter RC network**
- **Internal VCO/2 option**
- **Balanced drive outputs ±24mA**
- **ESD >2000V**
- **80MHz maximum frequency**
- **Available in QSOP package**

DESCRIPTION:

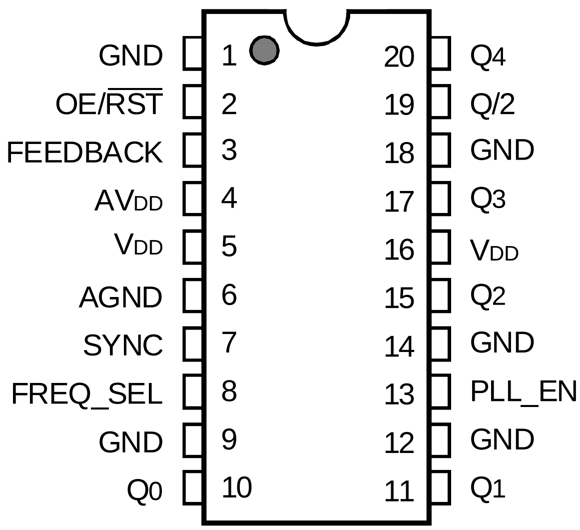
The QS5931T Clock Driver uses an internal phase locked loop (PLL) to lock low skew outputs to a reference clock input. Six outputs are available: Q0–Q4, Q/2. Careful layout and design ensure <250ps skew between the Q0–Q4, and Q/2 outputs. The QS5931T includes an internal RC filter which provides excellent jitter characteristics and eliminates the need for external components. Various combinations of feedback and a divide-by-2 in the VCO path allow applications to be customized for linear VCO operation over a wide range of input SYNC frequencies. The PLL can also be disabled by the PLL_EN signal to allow low frequency or DC testing. The QS5931T is designed for use in cost sensitive high-performance computing systems, workstations, multi-board computers, networking hardware, and mainframe systems. Several can be used in parallel or scattered throughout a system for guaranteed low skew, system-wide clock distribution networks. In the QSOP package, the QS5931T clock driver represents the best value in small form factor, high-performance clock management products.

For more information on PLL clock driver products, see Application Note AN-227.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
AV_{DD}/V_{DD}	Supply Voltage to Ground	–0.5 to +7	V
	DC Input Voltage V_{IN}	–0.5 to V_{DD}+0.5	V
	Maximum Power Dissipation (T_A = 85°C)	0.5	W
T_{STG}	Storage Temperature Range	–65 to +150	°C

NOTE:
1. Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

CAPACITANCE (T_A = +25°C, f = 1MHz, V_{IN} = 0V)

Pins	Typ.	Max.	Unit
C_{IN}	3	4	pF
C_{OUT}	4	5	pF

PIN DESCRIPTION

Pin Name	I/O	Description
SYNC	I	Reference clock input
FREQ_SEL	I	VCO frequency select. For choosing optimal VCO operating frequency depending on input frequency. HIGH is for higher frequencies, LOW is for lower frequencies.
FEEDBACK	I	PLL feedback input which is connected to either a Q or a Q/2 output. External feedback provides flexibility for different output frequency relationships. See the Frequency Selection Table for more information.
Q_0 - Q_4	O	Clock outputs
Q/2	O	Clock output. Matched in phase, but frequency is half the Q frequency.
OE/$\overline{RST}$	I	Output enable/asynchronous reset. Resets all output registers. When 0, all outputs are held in a tri-stated condition. When 1, outputs are enabled.
PLL_EN	I	PLL enable. Enables and disables the PLL. Allows the SYNC input to be single-stepped for system debug.
V_{DD}	—	Power supply for output buffers
AV_{DD}	—	Power supply for phase lock loop and other internal circuitries
GND	—	Ground supply for output buffers
AGND	—	Ground supply for phase lock loop and other internal circuitries

OUTPUT FREQUENCY SPECIFICATIONS

Industrial: T_A = –40°C to +85°C, AV_{DD}/V_{DD} = 5.0V ± 10%

Symbol	Description	–50	–66	–80	Units
F_{MAX_Q}	Max Frequency, Q_0 - Q_4,	50	66	80	MHz
$F_{MAX\_Q/2}$	Max Frequency, Q/2	25	33	40	MHz
F_{MIN_Q}	Min Frequency, Q_0 - Q_4	10	10	10	MHz
$F_{MIN\_Q/2}$	Min Frequency, Q/2	5	5	5	MHz

FREQUENCY SELECTION TABLE

FREQ_SEL	Output Used for Feedback	SYNC (MHz) (allowable range)(1)		Output Frequency Relationships	
		Min.	Max	Q/2	Q0 - Q4
HIGH	Q/2	$F_{MIN\_Q/2}$	$F_{MAX\_Q/2}$	SYNC	SYNC X 2
HIGH	Q0 -Q4	F_{MIN_Q}	F_{MAX_Q}	SYNC / 2	SYNC
LOW	Q/2	$F_{MIN\_Q/2}/2$	$F_{MAX\_Q/2}/2$	SYNC	SYNC X 2
LOW	Q0 -Q4	$F_{MIN\_Q}/2$	$F_{MAX\_Q}/2$	SYNC / 2	SYNC

NOTE:
1. Operation in the specified SYNC frequency range guarantees that the VCO will operate in its optimal range of 20MHz to F_{MAX_Q} x2. Operation with Sync inputs outside specified frequency ranges may result in out-of-lock outputs. FREQ_SEL only affects VCO frequency and does not affect output frequencies.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, AV_{DD}/V_{DD} = 5.0V ± 10%

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	—	—	0.8	V
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = −24mA	2.4	—	—	V
		V_{DD} = Min., I_{OH} = −100µA	3	—	—	
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 24mA	—	—	0.45	V
		V_{DD} = Min., I_{OL} = 100µA	—	—	0.2	
V_H	Input Hysteresis	—	—	100	—	mV
I_{OZ}	Output Leakage Current	V_{OUT} = V_{DD} or GND, V_{DD} = Max., Outputs Disabled	—	—	5	µA
I_{IN}	Input Leakage Current	V_{IN} = AV_{DD} or GND, AV_{DD} = Max.	—	—	5	µA

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions	Typ.	Max.	Unit
I_{DDQ}	Quiescent Power Supply Current	V_{DD} = Max., OE/$\overline{RST}$ = LOW, SYNC = LOW, All outputs unloaded	—	1	mA
ΔI_{DD}	Power Supply Current per Input HIGH	V_{DD} = Max., V_{IN} = 3.4V	0.7	1.5	mA
I_{DDD}	Dynamic Power Supply Current per Output	V_{DD} = Max., C_L = 0pF	—	0.1	µA/MHz

INPUT TIMING REQUIREMENTS

Symbol	Description(1)	Min.	Max.	Unit
t_R, t_F	Maximum input rise and fall times, 0.8V to 2V	—	3	ns
F_I	Input Clock Frequency, SYNC (1)	2.5	F_{MAX_Q}	MHz
t_{PWC}	Input clock pulse, HIGH or LOW (2)	2	—	ns
D_H	Duty Cycle, SYNC (2)	25	75	%

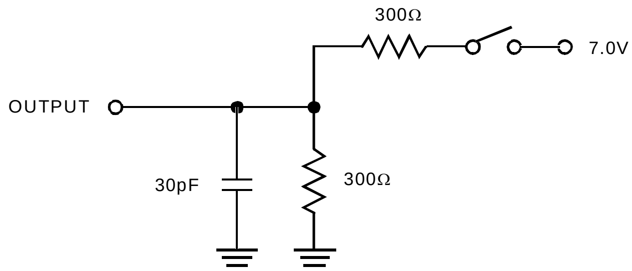
NOTES:
1. See Output Frequency and Frequency Selection tables for more detail on allowable SYNC input frequencies for different speed grades with different FEEDBACK and FREQ_SEL combinations.
2. Where pulse witdh implied by D_H is less than t_{WPC} limit, t_{WPC} limit applies

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

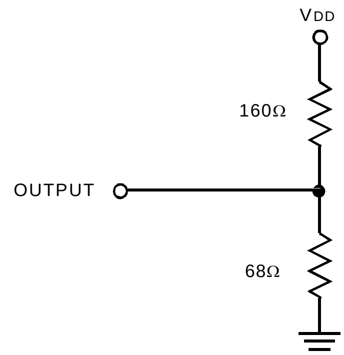
Symbol	Parameter [1]	Min.	Max.	Unit
t_{SKR}	Output Skew Between Rising Edges, Q_0-Q_4 and Q/2 [2]	—	250	ps
t_{SKF}	Output Skew Between Falling Edges, Q_0-Q_4 and Q/2 [2]	—	350	ps
t_{PW}	Pulse Width, Q_0-Q_4, Q/2 outputs, 80MHz	$T_{CY}/2 - 0.4$	$T_{CY}/2 + 0.4$	ns
t_J	Cycle-to-Cycle Jitter [4]	—	0.25	ns
t_{PD}	SYNC Input to Feedback Delay [5]	−100	400	ps
t_{LOCK}	SYNC to Phase Lock	—	10	ms
t_{PZH} t_{PZL}	Output Enable Time, OE/$\overline{RST}$ LOW to HIGH [3]	0	7	ns
t_{PHZ} t_{PLZ}	Output Disable Time, OE/$\overline{RST}$ HIGH to LOW [3]	0	6	ns
t_R, t_F	Output Rise/Fall Times, 0.8V to 2V	0.3	1.5	ns

NOTES:
1. See Test Loads and Waveforms for test load and termination.
2. Skew specifications apply under identical environments (loading, temperature, V_{DD}, device speed grade).
3. Measured in open loop mode PLL_EN = 0.
4. Jitter is characterized with Q output at 20MHz. See Frequency Selection Table for information on proper FREQ_SEL level for specified input frequencies.
5. t_{PD} measured at device inputs at 1.5V, Q output at 80MHz.

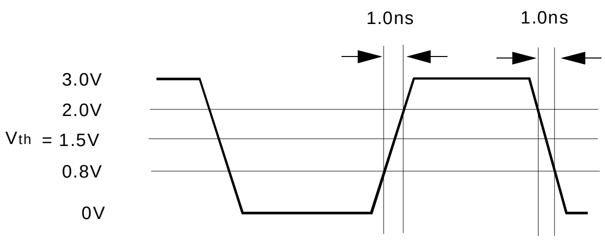
AC TEST LOADS AND WAVEFORMS



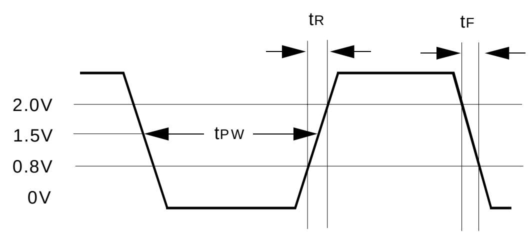
Test Circuit 1



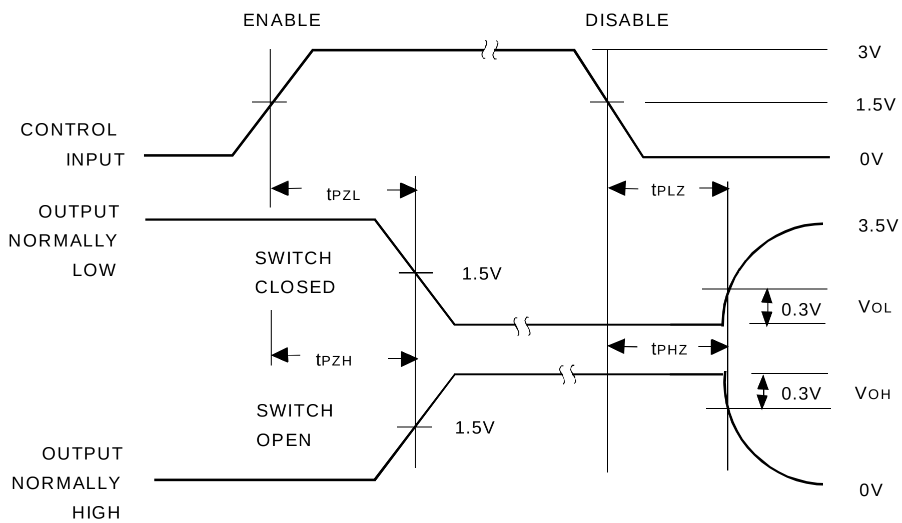
Test Circuit 2



TTL Input Test Waveform



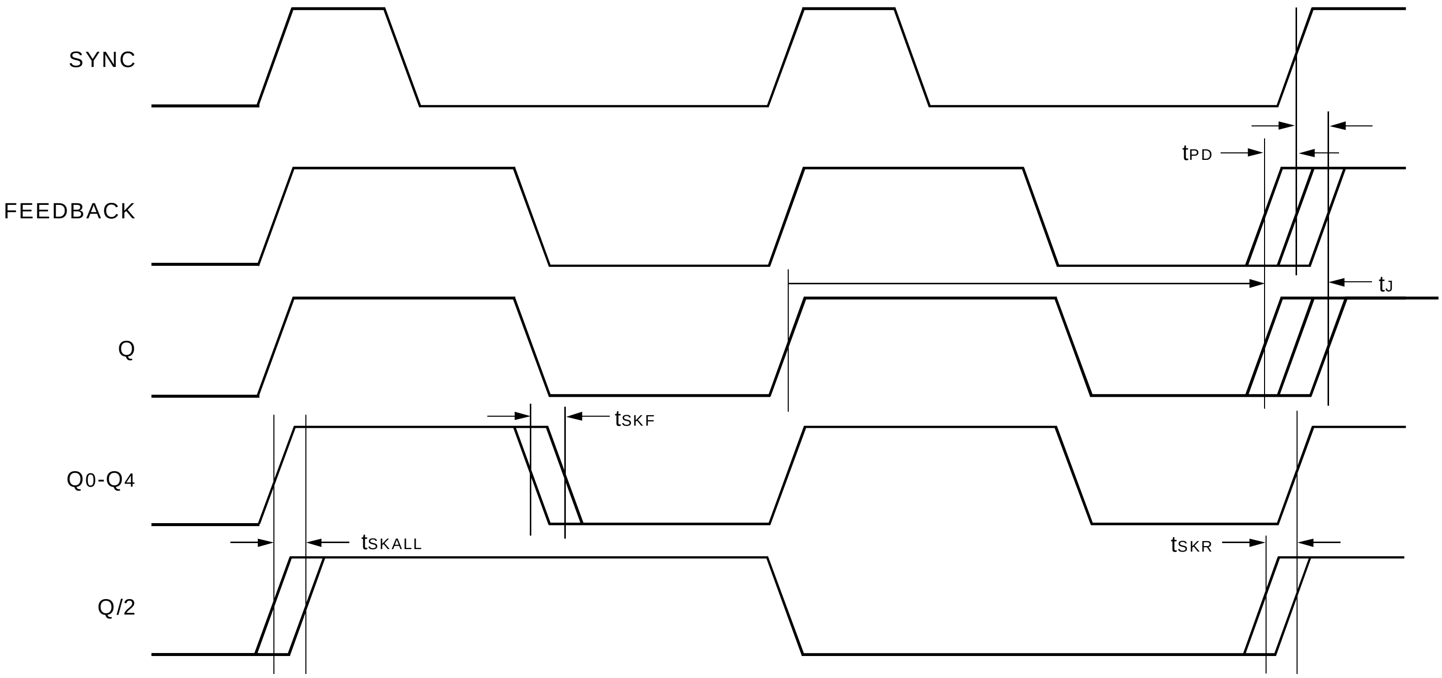
TTL Output Waveform



Enable and Disable Times

TEST CIRCUIT 1 is used for output enable/disable parameters.
TEST CIRCUIT 2 is used for all other timing parameters.

AC TIMING DIAGRAM

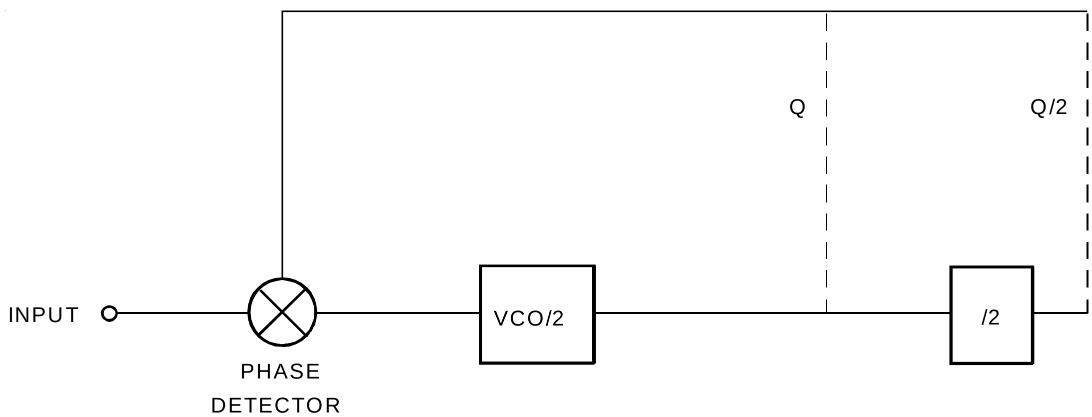


NOTES:
1. AC Timing Diagram applies to Q output connected to FEEDBACK.
2. All parameters are measured at 1.5V.

PLL OPERATION

The Phase Locked Loop (PLL) circuit included in the QS5931T provides for replication of incoming SYNC clock signals. Any manipulation of that signal, such as frequency multiplying, is performed by digital logic following the PLL (see the block diagram). The key advantage of the PLL circuit is to provide an effective zero propagation delay between the output and input signals. In fact, adding delay circuits in the feedback path, 'propagation delay' can even be negative! A simplified schematic of the QS5931T PLL circuit is shown below:

SIMPLIFIED DIAGRAM OF QS5931T FEEDBACK



The phase difference between the output and the input frequencies feeds the VCO which drives the outputs. Whichever output is fed back, it will stabilize at the same frequency as the input. Hence, this is a true negative feedback closed loop system. In most applications, the output will optimally have zero phase shift with respect to the input. In fact, the internal loop filter on the QS5931T typically provides within 150ps of phase shift between input and output.

If the user wishes to vary the phase difference (typically to compensate for backplane delays), this is most easily accomplished by adding delay circuits to the feedback path. The respective output used for feedback will be advanced by the amount of delay in the feedback path. All other outputs will retain their proper relationships to that output.

ORDERING INFORMATION

QS XXXX X X X

Device Type — Speed — Package — Process

Process	Blank	Industrial (-40°C to +85°C)
Package	Q	Quarter Size Outline Package
Speed	-50	50 MHz. max. frequency
	-66	66 MHz. max. frequency
	-80	80 MHz. max. frequency
Device Type	5931T	Low Skew TTL PLL Clock Driver with Integrated Loop Filter

IDT

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
logichelp@idt.com
(408) 654-6459