

DESCRIPTION

The SC1537 is designed to maintain a glitch-free 3.3V output when at least one of two inputs, 5V (VIN) and 3.3V (VAUX), is present.

Whenever VIN exceeds a predetermined threshold value, the internal 3.3V linear regulator is enabled, and DR is pulled high.

When VIN falls below a lower threshold value, DR is pulled low and the internal linear regulator is turned off. DR has been designed to drive the gate of an external low threshold P-channel MOSFET, which can be used to connect the 3.3V supply directly to the regulator output. This ensures an uninterrupted 3.3V output even if VIN falls out of specification. A maximum $R_{DS(ON)}$ of 100mΩ is recommended.

When both supplies are simultaneously available, the drive pin (DR) will be pulled High, turning off the external PMOS switch.

The internal 5V detector has its upper threshold (for VIN rising) set to 4.22V (typical) while the lower threshold (for VIN falling) is at 4.05V (typical) giving a hysteresis of approximately 170mV.

The SC1537 is available in the popular SO-8 and 5-lead TO-263 surface mount packages.

FEATURES

- Glitch-free transition between input sources
- Internal logic selects input source
- Gate drive for external PMOS bypass switch
- 5V detector with hysteresis
- 1% regulated output voltage accuracy
- 700mA load current capability
- SO-8 and TO-263 packages

APPLICATIONS

- Desktop Computers
- Network Interface Cards (NICs)
- PCMCIA/PCI Interface Cards
- Cardbus™ Technology
- Power supplies with multiple input sources

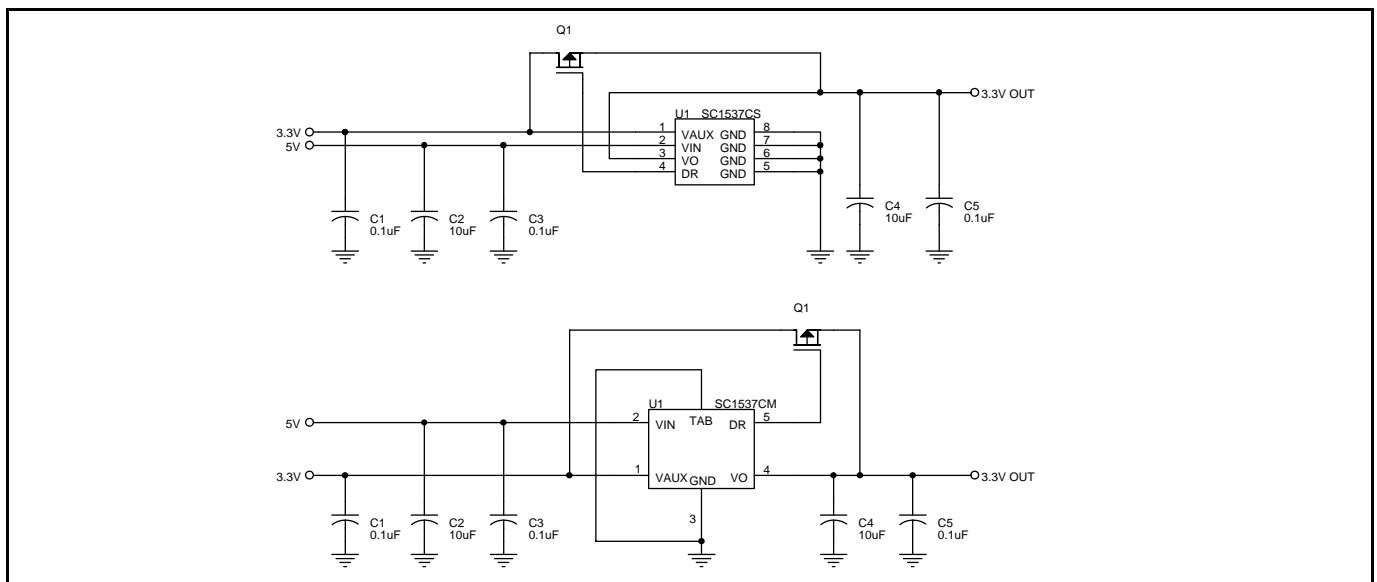
ORDERING INFORMATION

Part Number ⁽¹⁾	Package
SC1537CSTR	SO-8
SC1537CMTR	TO-263-5L

Note:

(1) Only available in tape and reel packaging. A reel contains 2500 devices for SO-8 and 800 devices for TO-263.

APPLICATION CIRCUIT



NOTE:

(1) External switch (Q1): use a low threshold P-channel MOSFET such as Vishay Si2305DS ($R_{DS(ON)} < 71\text{m}\Omega$ at $V_{GS} = 2.5\text{V}$) or International Rectifier IRLML6401 ($R_{DS(ON)} < 85\text{m}\Omega$ at $V_{GS} = 2.5\text{V}$), or equivalent.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Maximum	Units
Input Supply Voltage	V _{IN}	-0.5 to +7	V
Auxiliary Supply Voltage	VAUX	-0.5 to +7	V
LDO Output Current	I _O	10 to 700	mA
Operating Ambient Temperature Range	T _A	0 to +70	°C
Operating Junction Temperature Range	T _J	0 to +125	°C
Storage Temperature Range	T _{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec	T _{LEAD}	300	°C
Thermal Impedance Junction to Ambient SO-8 ⁽¹⁾ TO-263	θ _{JA}	65 60	°C/W
Thermal Impedance Junction to Case SO-8 TO-263	θ _{JC}	39 3	°C/W
ESD Rating (Human Body Model)	ESD	2	kV

Note:

(1) 1 inch square of 1/16" FR-4, double sided, 1 oz. minimum copper weight.

ELECTRICAL CHARACTERISTICS

 Unless specified, T_A = 25°C, V_{IN} = 5V, VAUX = 3.3V, I_O = 700mA, C_O = 10µF. Values in **bold** apply over full operating temperature range.

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
VIN						
Supply Voltage	V _{IN}	VAUX = 0V	4.75	5.00	5.25	V
Quiescent Current	I _Q	VIN = 5V, VAUX = 0V, I _O = 0mA		9.0	14.0	mA
				16.0		
Reverse Leakage From VAUX	I _{VIN}	VAUX = 3.6V, VIN = 0V, I _O = 0mA		13.0	17.0	mA
					18.0	
VAUX						
Supply Voltage	VAUX		3.0	3.3	3.6	V
Quiescent Current	I _{Q(AUX)}	VAUX = 3.3V, VIN = 0V, I _O = 0mA		8.0	11.0	mA
				13.0		
		VAUX = 3.3V, VIN = 5V, I _O = 0mA		1.5	2.5	mA
					3.0	

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ELECTRICAL CHARACTERISTICS

 Unless specified, $T_A = 25^\circ\text{C}$, $V_{IN} = 5\text{V}$, $V_{AUX} = 3.3\text{V}$, $I_O = 700\text{mA}$, $C_O = 10\mu\text{F}$. Values in **bold** apply over full operating temperature range.

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Unit
VAUX (Cont.)						
Reverse Leakage From VIN	I_{VAUX}	$V_{IN} = 5.5\text{V}$, $V_{AUX} = 0\text{V}$, $I_O = 0\text{mA}$		-5.0	-50.0	μA
					-100.0	
5V Detect⁽¹⁾⁽²⁾⁽³⁾						
Low Threshold Voltage	$V_{TH(LO)}$	VIN Falling, $I_O = 20\text{mA}$	3.92	4.05	4.18	V
			3.90		4.20	
Hysteresis	V_{HYST}		90	170		mV
			80			
High Threshold Voltage	$V_{TH(HI)}$	VIN Rising, $I_O = 20\text{mA}$			4.35	V
VO						
LDO Output Voltage	V_O	$I_O = 20\text{mA}$	3.267	3.300	3.333	V
		$4.75\text{V} \leq V_{IN} \leq 5.25\text{V}$, $0\text{mA} \leq I_O \leq 700\text{mA}$	3.234		3.366	
Output Current	I_O				400	mA
Line Regulation	$REG_{(LINE)}$	$V_{IN} = 4.75\text{V}$ to 5.25V		0.20	0.60	%
					0.80	
Load Regulation	$REG_{(LOAD)}$	$I_O = 10\text{mA}$ to 700mA		0.6	1.0	%
					1.2	
Drive Output						
Drive Voltage	V_{DR}	$4.75\text{V} \leq V_{IN} \leq 5.25\text{V}$, $I_{DR} = 200\mu\text{A}$	3.4	$V_{IN} - 0.8$		V
			3.3			
		$V_{IN} < V_{TH(LO)}$, $I_{DR} = -200\mu\text{A}$		35	150	mV
					250	
Peak Drive Current	$I_{DR(PK)}$	Sinking: $V_{IN} = 3.9\text{V}$, $V_{DR} = 1\text{V}$; Sourcing: $V_{IN} = 4.35\text{V}$, $V_{IN} - V_{DR} = 2.5\text{V}$	7			mA
			6			
Drive High Delay ⁽¹⁾⁽⁴⁾	t_{DH}	$C_{DR} = 1.2\text{nF}$, VIN ramping up, measured from $V_{IN} = V_{TH(HI)}$ to $V_{DR} = 2\text{V}$		0.5	1.0	μs
					2.0	
Drive Low Delay ⁽¹⁾⁽⁴⁾	t_{DL}	$C_{DR} = 1.2\text{nF}$, VIN ramping down, measured from $V_{IN} = V_{TH(LO)}$ to $V_{DR} = 2\text{V}$		0.5	1.0	μs
					2.0	

NOTES:

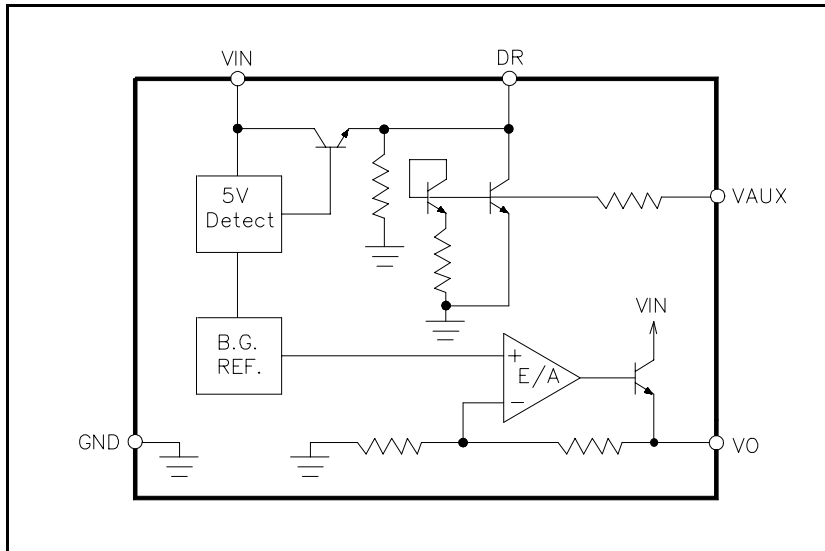
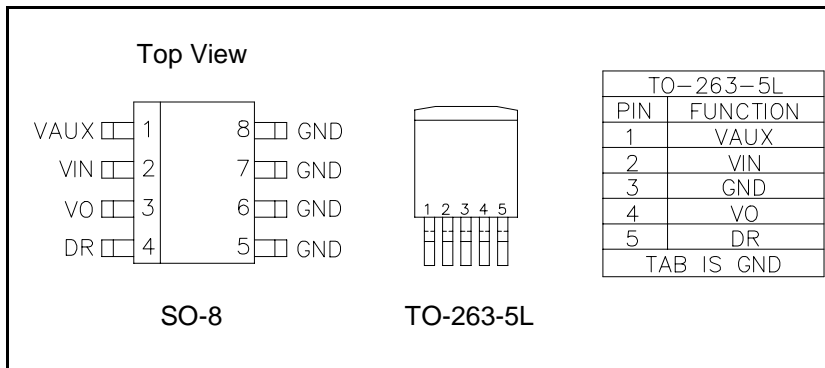
(1) Guaranteed by design.

(2) See 5V Detect Thresholds on page 5.

 (3) Recommended source impedance for 5V supply: $\leq 0.07\Omega$. This will ensure that $I_O \times R_{SOURCE} < V_{HYST}$, thus avoiding DR toggling during 5V detect threshold transitions.

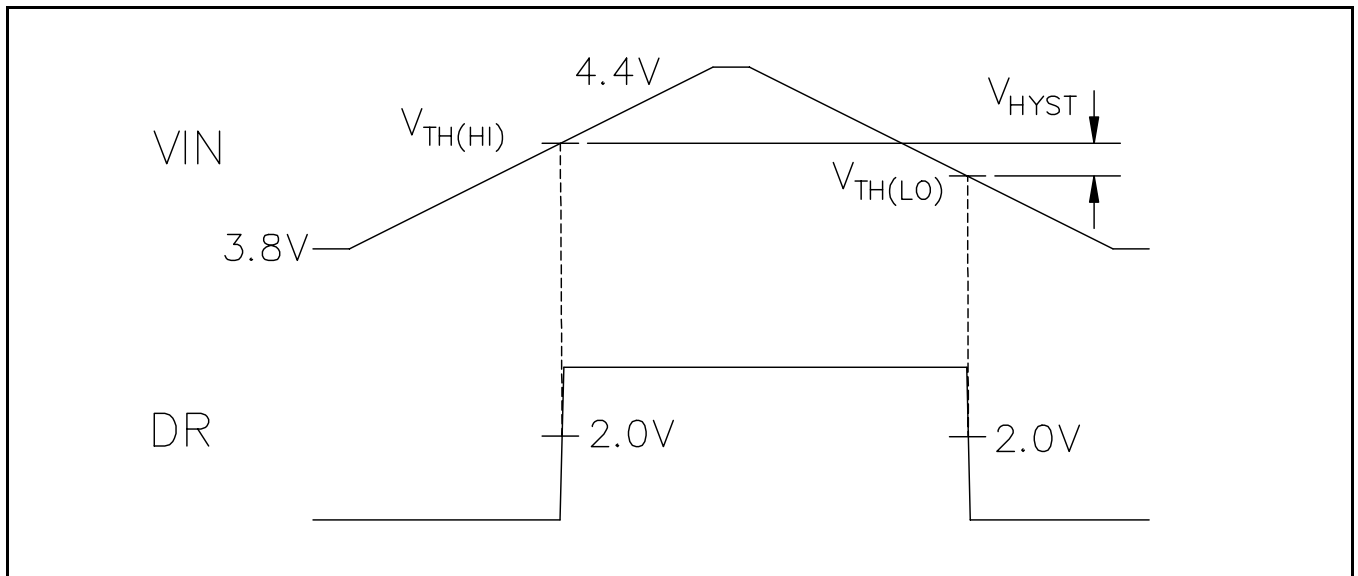
(4) See Timing Diagram on page 5.

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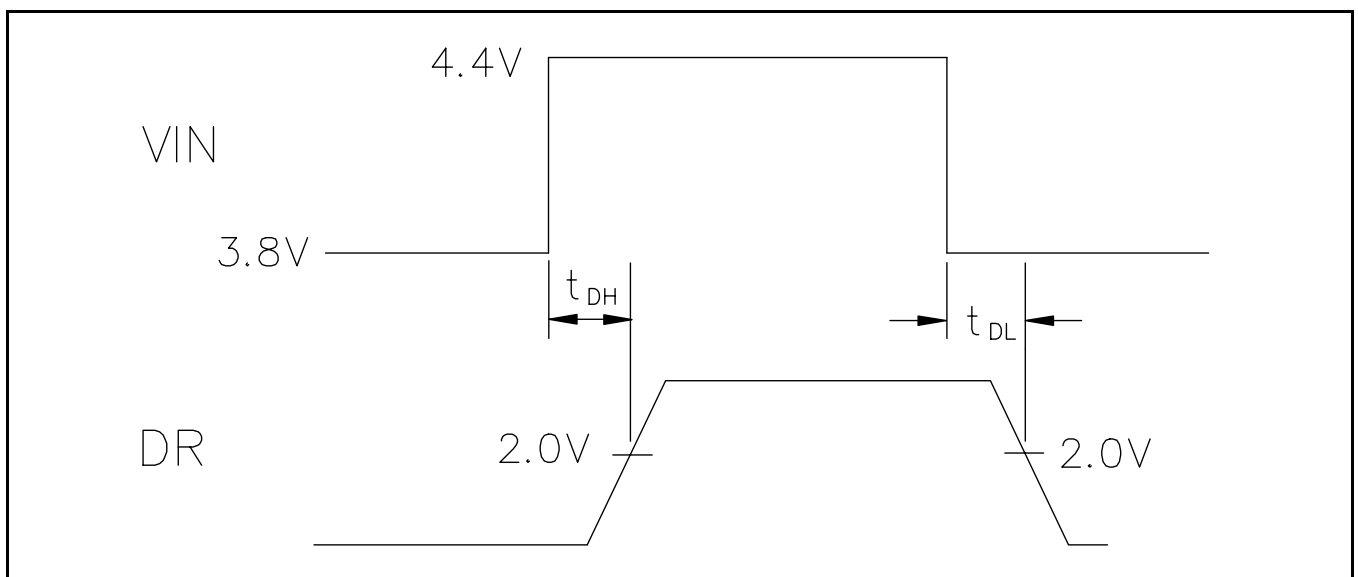
BLOCK DIAGRAM

PIN CONFIGURATION

PIN DESCRIPTION

Pin Name	SO-8 Pin #	TO-263-5L Pin #	Pin Function
DR	4	5	Driver output for external P-channel MOSFET pass element.
GND	5,6,7,8	3/TAB	Logic and power ground.
VAUX	1	1	This is the auxiliary input supply, nominally 3.3V.
VIN	2	2	This is the main input supply for the IC, nominally 5V.
VO	3	4	LDO 3.3V output.

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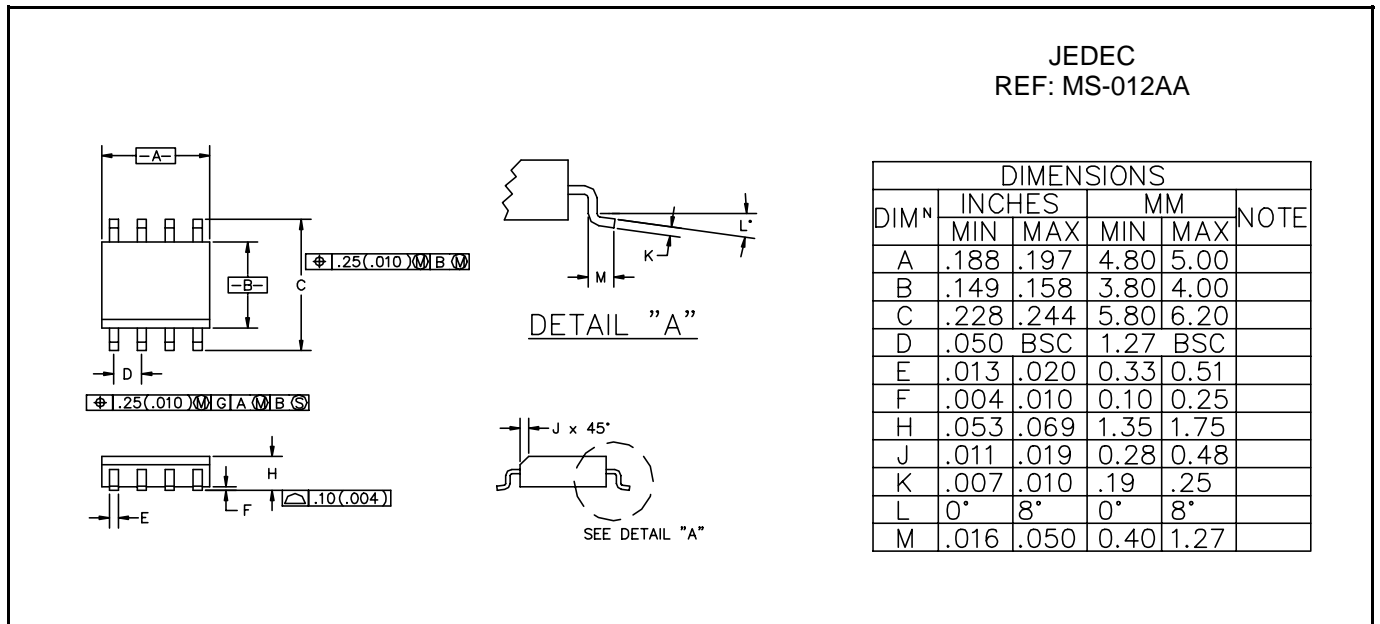
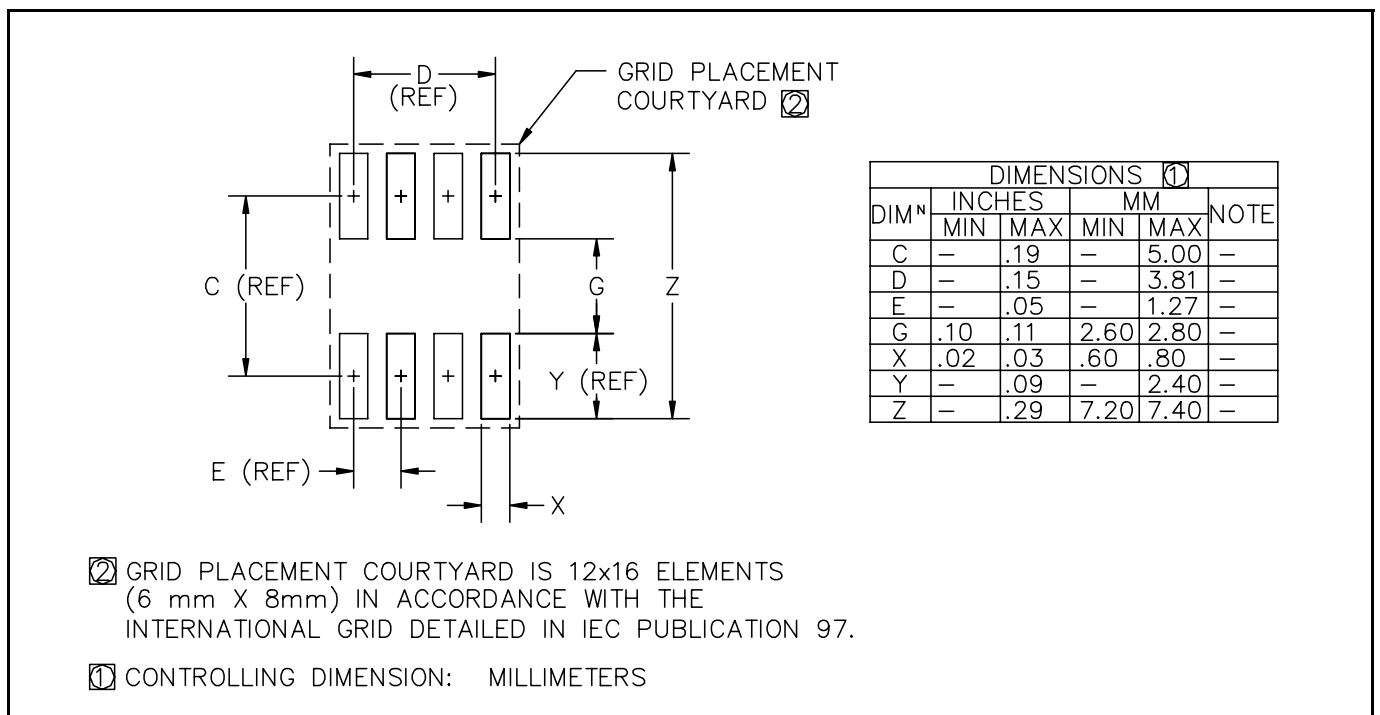
5V DETECT THRESHOLDS

NOTE:

 (1) VIN rise and fall times (10% to 90%) to be $\geq 100\mu s$.

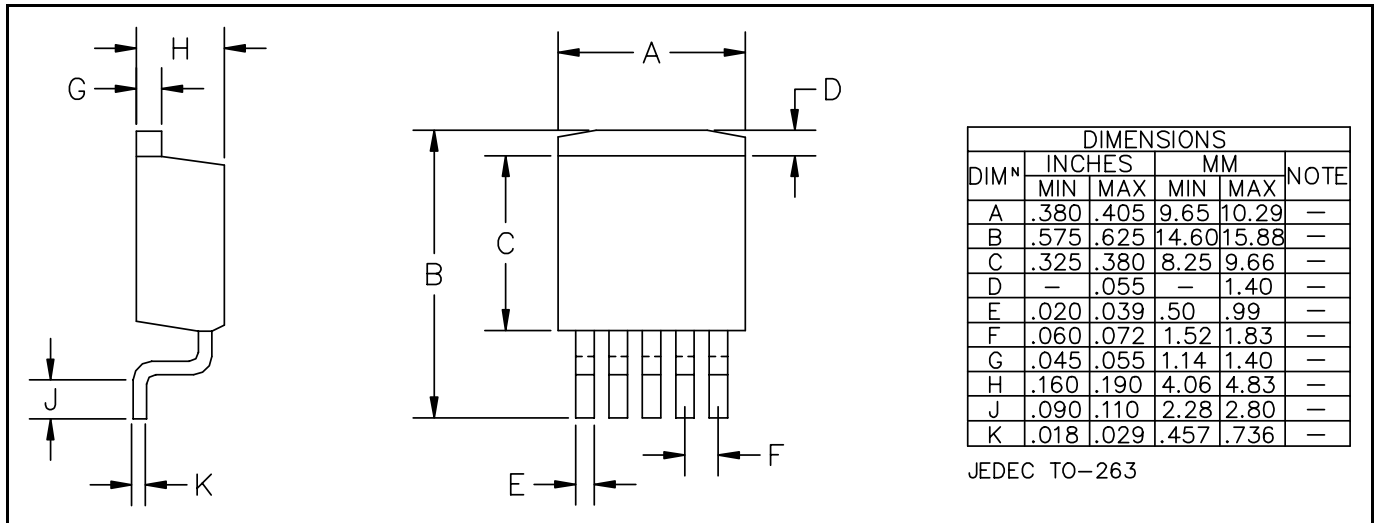
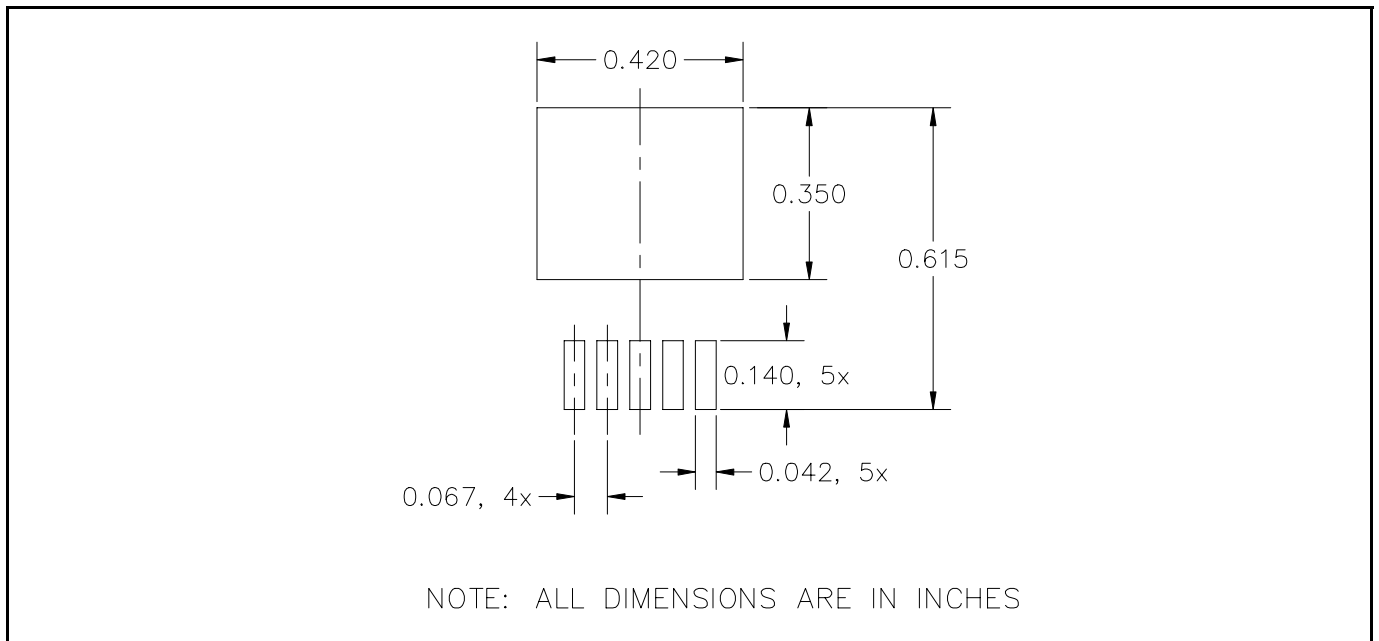
TIMING DIAGRAM

NOTE:

 (1) VIN rise and fall times (10% to 90%) to be $\leq 100ns$.

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OUTLINE DRAWING - SO-8

MINIMUM LAND PATTERN - SO-8


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DEVICE OUTLINE - TO-263, 5 PIN

MINIMUM LAND PATTERN - TO-263, 5 PIN


ECN00-1177