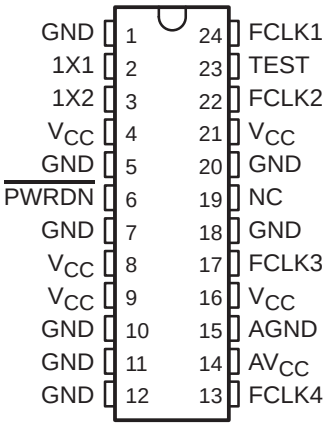
- **Two Integrated PLLs Provide All Digital Video Disk (DVD) System Frequencies**
- **Two 27-MHz Reference Clock Outputs**
- **One 18.432-MHz Reference Clock Output**
- **One 33.875-MHz Reference Clock Output**
- **Output Clock Frequencies Derived From an 18.432-MHz Crystal Input**
- **3.3-V CMOS Outputs**
- **Separate Analog Core and Output Supply Voltage**
- **Internal Loop Filters for Phase-Lock Loops Eliminate the Need for External Components**

DB PACKAGE
(TOP VIEW)



NC – No internal connection

description

The CDC9171 is a high-performance clock synthesizer that generates the required clock signals needed for a DVD system.

The CDC9171 generates all output frequencies from an 18.432-MHz crystal. The 18.432-MHz (FCLK1) reference clock output is buffered from the integrated oscillators. Two integrated phase-lock loops (PLL) synthesize the 27-MHz (FCLK2, FCLK3) and the 33.868-MHz (FCLK4) reference clock outputs from the 18.4320-MHz crystal. The oscillator and PLLs can be bypassed in the TEST mode. When TEST is high, input 1X1 is buffered to all outputs.

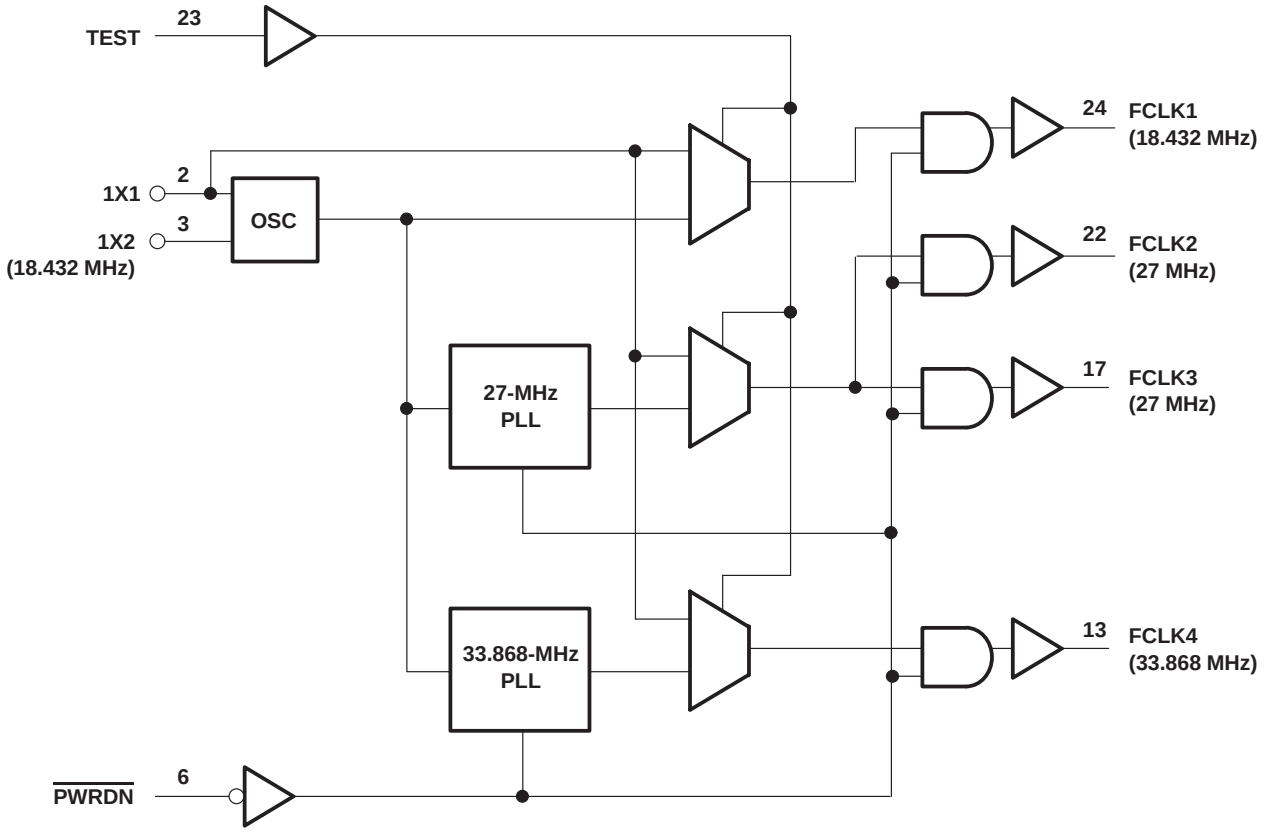
All clock outputs provide low-jitter clock signals for reliable clock operation. $\overline{\text{PWRDN}}$ is used to disable the PLLs and output buffers. When low, $\overline{\text{PWRDN}}$ disables the integrated PLLs and forces all outputs to a logic-low state.

Because the CDC9171 is based on PLL circuitry, it requires a stabilization time to achieve phase lock of the PLL. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at the 1X1 input and upon activation, following the transition of $\overline{\text{PWRDN}}$ to a logic-high state.

FUNCTION TABLE

INPUTS			OUTPUTS		
$\overline{\text{PWRDN}}$	TEST	1X1	FCLK1	FCLK(2–3)	FLCK4
L	X	X	L	L	L
H	L	18.432 MHz	18.432 MHz	27 MHz	33.868 MHz
H	H	L	L	L	L
H	H	H	H	H	H

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 6.5 V
Voltage range applied to any output in the high state or power-off state, V_O) . . . . . –0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O . . . . . ±35 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_I < 0) . . . . . ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) . . . . . 0.65 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_I	Input voltage ($\overline{PWRDN}$ only)	0	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{IK}	V_{CC} = 3 V,	I_I = –18 mA				–1.2		–1.2	V
V_{OH}	V_{CC} = 3 V,	I_{OH} = –8 mA		2.4			2.4		V
V_{OL}	V_{CC} = 3 V,	I_{OL} = 8 mA				0.4		0.4	V
I_I†	V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±1		±1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0	Outputs active ($\overline{PWRDN}$ = H)		20	35		35	mA
			Outputs low ($\overline{PWRDN}$ = L)		5	10		10	
C_i†	V_I = 3 V or 0				7				pF
C_o	V_O = 3 V or 0				8				pF

† Except for crystal input (1X1)

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
Stabilization time‡	After $\overline{PWRDN}$ ↑		5	ms
	After power up		5	

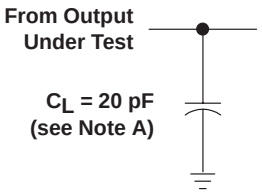
‡ Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at 1X1.

switching characteristics over recommended free-air temperature range for 3-V outputs (see Figure 1)§

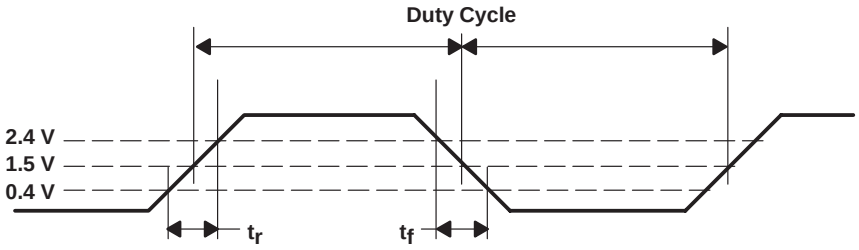
PARAMETER		V_{CC} = 3.3 V, T_A = 25°C		V_{CC} = 3 V to 3.6 V, T_A = 0°C to 70°C		UNIT
		MIN	MAX	MIN	MAX	
Jitter	FCLK1				±200	ps
	All other outputs				±250	
Duty cycle	Any output			45%	55%	
t_r¶	Any output (C_L = 20 pF)				2.5	ns
t_f¶	Any output (C_L = 20 pF)				2.5	ns

§ Specifications are applicable only after the PLL stabilization time has elapsed.
¶ Rise and fall times are characterized using the test circuit shown in Figure 1.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



NOTES: A. C_L inlcudes probe and jig capacitance.
B. The outputs are measured one at a time with one transition per measurement.

Figure 1. Voltage Waveform and Load Circuit

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