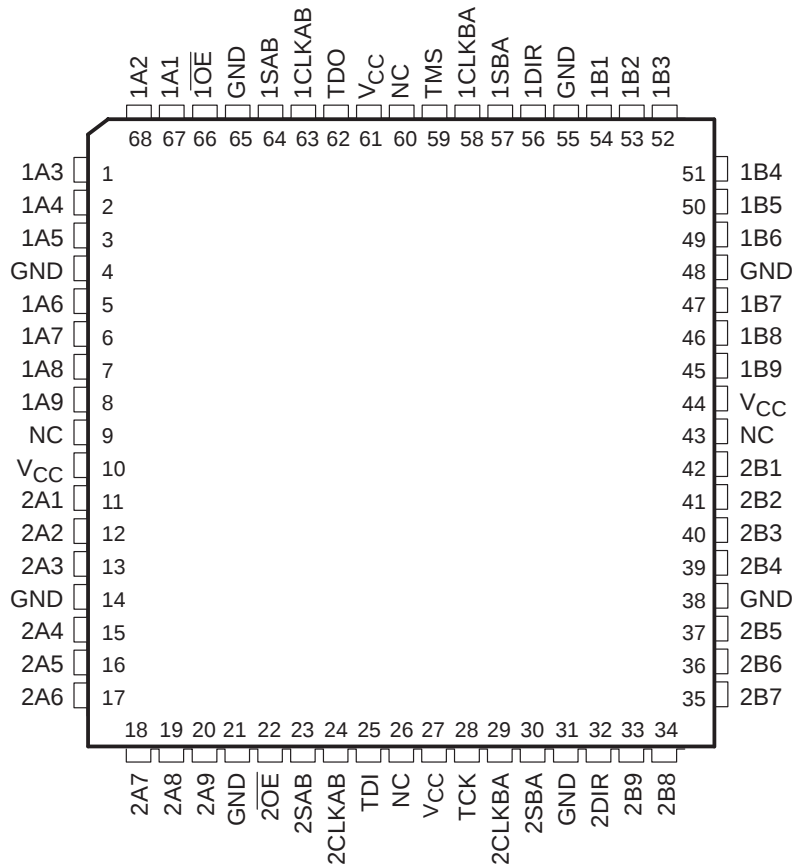


# SN54ABT18646, SN74ABT18646 SCAN TEST DEVICES WITH 18-BIT TRANSCEIVERS AND REGISTERS

SCBS131–AUGUST 1992–REVISED OCTOBER 1992

- Members of the Texas Instruments **SCOPE™** Family of Testability Products
- Members of the Texas Instruments **Widebus™** Family
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Include D-Type Flip-Flops and Control Circuitry to Provide Multiplexed Transmission of Stored and Real-Time Data
- Two Boundary-Scan Cells per I/O for Greater Flexibility
- State-of-the-Art **EPIC-II B™** BiCMOS Design Significantly Reduces Power Dissipation
- **SCOPE™** Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs With Masking Option
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Shrink Quad Flat Pack (PM) and 68-Pin Ceramic Quad Flat Pack (HV)

SN54ABT18646 . . . HV PACKAGE  
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

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## description (continued)

In the test mode, the normal operation of the SCOPE™ bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Additional flexibility is provided in the test mode through the use of two boundary scan cells (BSCs) for each I/O pin. This allows independent test data to be captured and forced at either bus (A or B). A PSA/COUNT instruction is also included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

The SN54ABT18646 is characterized over the full military temperature range of –55°C to 125°C. The SN74ABT18646 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**  
(normal mode, each 9-bit section)

| INPUTS |     |       |       |     |     | DATA I/O       |                | OPERATION OR FUNCTION     |
|--------|-----|-------|-------|-----|-----|----------------|----------------|---------------------------|
| OE     | DIR | CLKAB | CLKBA | SAB | SBA | A1 THRU A9     | B1 THRU B9     |                           |
| X      | X   | ↑     | X     | X   | X   | Input          | Unspecified†   | Store A, B unspecified†   |
| X      | X   | X     | ↑     | X   | X   | Unspecified†   | Input          | Store B, A unspecified†   |
| H      | X   | ↑     | ↑     | X   | X   | Input          | Input          | Store A and B data        |
| H      | X   | L     | L     | X   | X   | Input disabled | Input disabled | Isolation, hold storage   |
| L      | L   | X     | X     | X   | L   | Output         | Input          | Real-time B data to A bus |
| L      | L   | X     | L     | X   | H   | Output         | Input disabled | Stored B data to A bus    |
| L      | H   | X     | X     | L   | X   | Input          | Output         | Real-time A data to B bus |
| L      | H   | L     | X     | H   | X   | Input disabled | Output         | Stored A data to B bus    |

† The data output functions can be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

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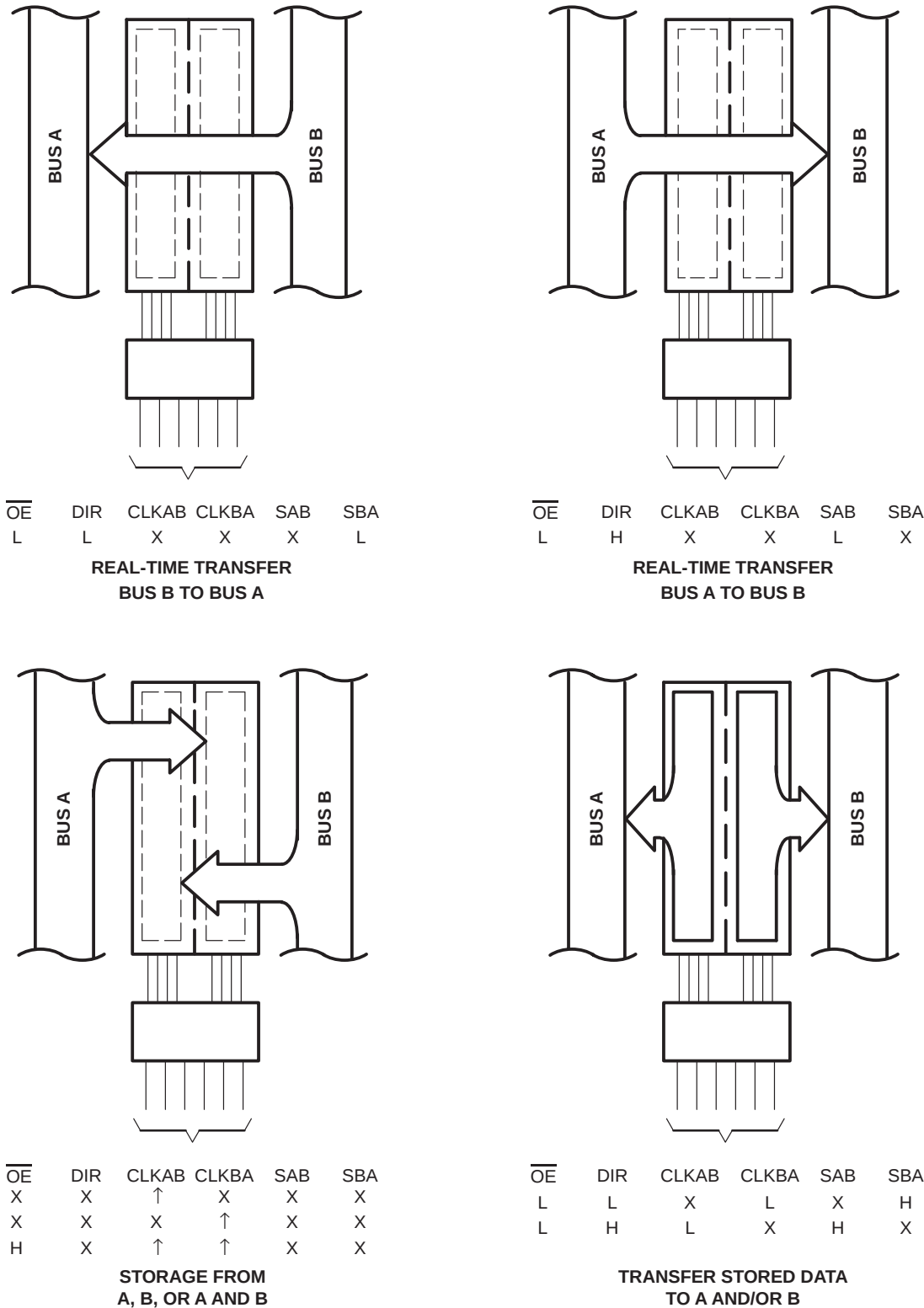
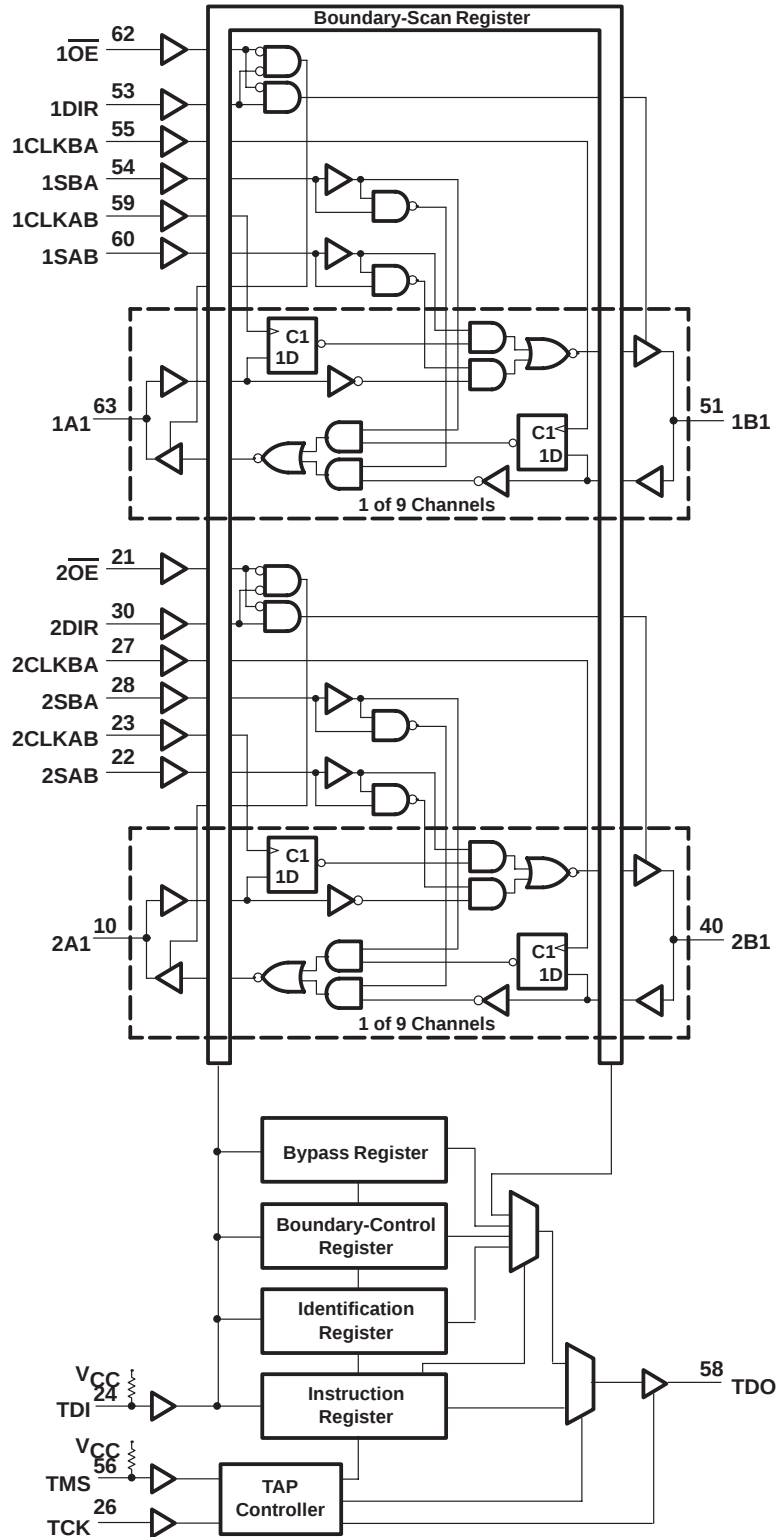


Figure 1. Bus-Management Functions

functional block diagram



Pin numbers shown are for the PM package.

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# SN54ABT18646, SN74ABT18646

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                                           |                 |
|-------------------------------------------------------------------------------------------|-----------------|
| Supply voltage range, $V_{CC}$                                                            | –0.5 V to 7 V   |
| Input voltage range, $V_I$ (except I/O ports) (see Note NO TAG)                           | –0.5 V to 7 V   |
| Input voltage range, $V_I$ (I/O ports) (see Note NO TAG)                                  | –0.5 V to 5.5 V |
| Voltage range applied to any output in the high state or power-off state, $V_O$           | –0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$ : SN54ABT18646                            | 96 mA           |
| SN74ABT18646                                                                              | 128 mA          |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                                               | –18 mA          |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ )                                              | –50 mA          |
| Maximum package power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2) | 885 mW          |
| Storage temperature range                                                                 | –65°C to 150°C  |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. For the SN74ABT18646 (PM package), the power derating factor for ambient temperatures greater than 55°C is –10.5 mW/°C.

#### recommended operating conditions (see Note 3)

|                     |                                    | SN54ABT18646 |          | SN74ABT18646 |          | UNIT |
|---------------------|------------------------------------|--------------|----------|--------------|----------|------|
|                     |                                    | MIN          | MAX      | MIN          | MAX      |      |
| $V_{CC}$            | Supply voltage                     | 4.5          | 5.5      | 4.5          | 5.5      | V    |
| $V_{IH}$            | High-level input voltage           | 2            |          | 2            |          | V    |
| $V_{IL}$            | Low-level input voltage            |              | 0.8      |              | 0.8      | V    |
| $V_I$               | Input voltage                      | 0            | $V_{CC}$ | 0            | $V_{CC}$ | V    |
| $I_{OH}$            | High-level output current          |              | –24      |              | –32      | mA   |
| $I_{OL}$            | Low-level output current           |              | 48       |              | 64       | mA   |
| $\Delta t/\Delta v$ | Input transition rise or fall rate |              | 10       |              | 10       | ns/V |
| $T_A$               | Operating free-air temperature     | –55          | 125      | –40          | 85       | °C   |

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

| PARAMETER                     | TEST CONDITIONS                                                                      |                                           | T <sub>A</sub> = 25°C |                  |                   | SN54ABT18646 |      | SN74ABT18646 |      | UNIT |
|-------------------------------|--------------------------------------------------------------------------------------|-------------------------------------------|-----------------------|------------------|-------------------|--------------|------|--------------|------|------|
|                               |                                                                                      |                                           | MIN                   | TYP <sup>†</sup> | MAX               | MIN          | MAX  | MIN          | MAX  |      |
| V <sub>IK</sub>               | V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = –18 mA                                     |                                           |                       |                  | –1.2              |              | –1.2 |              | –1.2 | V    |
| V <sub>OH</sub>               | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = –3 mA                                     |                                           | 2.5                   |                  |                   | 2.5          |      | 2.5          |      | V    |
|                               | V <sub>CC</sub> = 5 V, I <sub>OH</sub> = –3 mA                                       |                                           | 3                     |                  |                   | 3            |      | 3            |      |      |
|                               | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = –24 mA                                    |                                           | 2                     |                  |                   | 2            |      |              |      |      |
|                               | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = –32 mA                                    |                                           | 2 <sup>‡</sup>        |                  |                   |              |      | 2            |      |      |
| V <sub>OL</sub>               | V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA                                     |                                           |                       |                  | 0.55              |              | 0.55 |              |      | V    |
|                               | V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA                                     |                                           |                       |                  | 0.55 <sup>‡</sup> |              |      |              | 0.55 |      |
| I <sub>I</sub>                | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND                     | CLK, DIR, $\overline{\text{OE}}$ , S, TCK |                       |                  | ±1                |              | ±1   |              | ±1   | μA   |
|                               |                                                                                      | A or B ports                              |                       |                  | ±100              |              | ±100 |              | ±100 |      |
| I <sub>IH</sub>               | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub>                            | TDI, TMS                                  |                       |                  | 10                |              | 10   |              | 10   | μA   |
| I <sub>IL</sub>               | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = GND                                        | TDI, TMS                                  |                       |                  | –160              |              | –160 |              | –160 | μA   |
| I <sub>OZH</sub> <sup>§</sup> | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V                                      |                                           |                       |                  | 50                |              | 50   |              | 50   | μA   |
| I <sub>OZL</sub> <sup>§</sup> | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V                                      |                                           |                       |                  | –50               |              | –50  |              | –50  | μA   |
| I <sub>off</sub>              | V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 5.5 V                        |                                           |                       |                  | ±100              |              |      |              | ±100 | μA   |
| I <sub>CEX</sub>              | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V                                      | Outputs high                              |                       |                  | 50                |              | 50   |              | 50   | μA   |
| I <sub>O</sub> <sup>¶</sup>   | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V                                      |                                           | –50                   | –100             | –180              | –50          | –180 | –50          | –180 | mA   |
| I <sub>CC</sub>               | V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND | A or B ports                              |                       |                  |                   |              |      |              |      | mA   |
|                               |                                                                                      | Outputs high                              |                       |                  | 0.9               | 2            | 2    | 2            | 2    |      |
|                               |                                                                                      | Outputs low                               |                       |                  | 30                | 38           | 38   | 38           | 38   |      |
|                               |                                                                                      | Outputs disabled                          |                       |                  | 0.9               | 2            | 2    | 2            | 2    |      |
| ΔI <sub>CC</sub> <sup>#</sup> | V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND  |                                           |                       |                  | 1.5               |              | 1.5  |              | 1.5  | mA   |
| C <sub>i</sub>                | V <sub>I</sub> = 2.5 V or 0.5 V                                                      | Control inputs                            |                       |                  | 3                 |              |      |              |      | pF   |
| C <sub>iO</sub>               | V <sub>O</sub> = 2.5 V or 0.5 V                                                      | A or B ports                              |                       |                  | 10                |              |      |              |      | pF   |
| C <sub>O</sub>                | V <sub>O</sub> = 2.5 V or 0.5 V                                                      | TDO                                       |                       |                  | 8                 |              |      |              |      | pF   |

NOTE 4: Preliminary specifications based on SPICE analysis

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V.

<sup>‡</sup> On products compliant to MIL-STD-883, Class B, this parameter does not apply.

<sup>§</sup> The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

<sup>¶</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>#</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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## SCAN TEST DEVICES WITH

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 2)

|                    |                 |                                                        | SN54ABT18646 |     | SN74ABT18646 |     | UNIT |
|--------------------|-----------------|--------------------------------------------------------|--------------|-----|--------------|-----|------|
|                    |                 |                                                        | MIN          | MAX | MIN          | MAX |      |
| $f_{\text{clock}}$ | Clock frequency | CLKAB or CLKBA                                         | 0            | 100 | 0            | 100 | MHz  |
| $t_w$              | Pulse duration  | CLKAB or CLKBA high or low                             |              |     | 3            |     | ns   |
| $t_{\text{su}}$    | Setup time      | A before CLKAB $\uparrow$ or B before CLKBA $\uparrow$ |              |     | 5            |     | ns   |
| $t_h$              | Hold time       | A after CLKAB $\uparrow$ or B after CLKBA $\uparrow$   |              |     | 0            |     | ns   |

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 2)

|                    |                 |                                                                     | SN54ABT18646 |     | SN74ABT18646 |     | UNIT          |
|--------------------|-----------------|---------------------------------------------------------------------|--------------|-----|--------------|-----|---------------|
|                    |                 |                                                                     | MIN          | MAX | MIN          | MAX |               |
| $f_{\text{clock}}$ | Clock frequency | TCK                                                                 | 0            | 50  | 0            | 50  | MHz           |
| $t_w$              | Pulse duration  | TCK high or low                                                     |              |     | 5            |     | ns            |
| $t_{\text{su}}$    | Setup time      | A, B, CLK, DIR, $\overline{\text{OE}}$ , or S before TCK $\uparrow$ |              |     | 5            |     | ns            |
|                    |                 | TDI before TCK $\uparrow$                                           |              |     | 6            |     |               |
|                    |                 | TMS before TCK $\uparrow$                                           |              |     | 6            |     |               |
| $t_h$              | Hold time       | A, B, CLK, DIR, $\overline{\text{OE}}$ , or S after TCK $\uparrow$  |              |     | 0            |     | ns            |
|                    |                 | TDI after TCK $\uparrow$                                            |              |     | 0            |     |               |
|                    |                 | TMS after TCK $\uparrow$                                            |              |     | 0            |     |               |
| $t_d$              | Delay time      | Power up to TCK $\uparrow$                                          |              |     | 50           |     | ns            |
| $t_r$              | Rise time       | $V_{\text{CC}}$ power up                                            |              |     | 1            |     | $\mu\text{s}$ |

NOTE 4: Preliminary specifications based on SPICE analysis

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 2)

| PARAMETER  | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC} = 5\text{ V}$ ,<br>$T_A = 25^\circ\text{C}$ |     |     | SN54ABT18646 |     | SN74ABT18646 |     | UNIT |
|------------|-----------------|----------------|-----------------------------------------------------|-----|-----|--------------|-----|--------------|-----|------|
|            |                 |                | MIN                                                 | TYP | MAX | MIN          | MAX | MIN          | MAX |      |
| $f_{\max}$ | CLKAB or CLKBA  |                | 100                                                 | 130 |     | 100          |     | 100          |     | MHz  |
| $t_{PLH}$  | A or B          | B or A         |                                                     |     |     |              |     | 1            | 6   | ns   |
| $t_{PHL}$  |                 |                |                                                     |     |     |              |     | 1            | 6   |      |
| $t_{PLH}$  | CLKAB or CLKBA  | B or A         |                                                     |     |     |              |     | 2            | 6   | ns   |
| $t_{PHL}$  |                 |                |                                                     |     |     |              |     | 2            | 6   |      |
| $t_{PLH}$  | SAB or SBA      | B or A         |                                                     |     |     |              |     | 2            | 8   | ns   |
| $t_{PHL}$  |                 |                |                                                     |     |     |              |     | 2            | 8   |      |
| $t_{PZH}$  | DIR             | B or A         |                                                     |     |     |              |     | 2            | 7.5 | ns   |
| $t_{PZL}$  |                 |                |                                                     |     |     |              |     | 2            | 7.5 |      |
| $t_{PZH}$  | $\overline{OE}$ | B or A         |                                                     |     |     |              |     | 2            | 7.5 | ns   |
| $t_{PZL}$  |                 |                |                                                     |     |     |              |     | 2            | 7.5 |      |
| $t_{PHZ}$  | DIR             | B or A         |                                                     |     |     |              |     | 2            | 7.5 | ns   |
| $t_{PLZ}$  |                 |                |                                                     |     |     |              |     | 2            | 7.5 |      |
| $t_{PHZ}$  | $\overline{OE}$ | B or A         |                                                     |     |     |              |     | 2            | 7.5 | ns   |
| $t_{PLZ}$  |                 |                |                                                     |     |     |              |     | 2            | 7.5 |      |

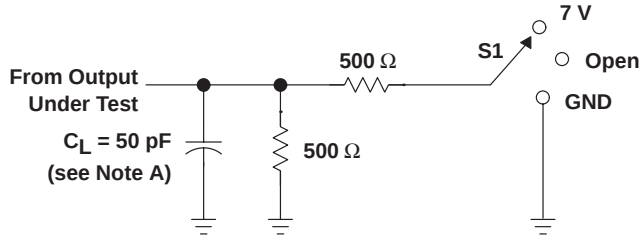
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 2)

| PARAMETER  | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC} = 5\text{ V}$ ,<br>$T_A = 25^\circ\text{C}$ |     |     | SN54ABT18646 |     | SN74ABT18646 |     | UNIT |
|------------|-----------------|----------------|-----------------------------------------------------|-----|-----|--------------|-----|--------------|-----|------|
|            |                 |                | MIN                                                 | TYP | MAX | MIN          | MAX | MIN          | MAX |      |
| $f_{\max}$ | TCK             |                | 50                                                  | 90  |     | 50           |     | 50           |     | MHz  |
| $t_{PLH}$  | TCK↓            | A or B         |                                                     |     |     |              |     | 3            | 12  | ns   |
| $t_{PHL}$  |                 |                |                                                     |     |     |              |     | 3            | 12  |      |
| $t_{PLH}$  | TCK↓            | TDO            |                                                     |     |     |              |     | 2            | 7   | ns   |
| $t_{PHL}$  |                 |                |                                                     |     |     |              |     | 2            | 7   |      |
| $t_{PZH}$  | TCK↓            | A or B         |                                                     |     |     |              |     | 3            | 14  | ns   |
| $t_{PZL}$  |                 |                |                                                     |     |     |              |     | 3            | 14  |      |
| $t_{PZH}$  | TCK↓            | TDO            |                                                     |     |     |              |     | 2            | 8   | ns   |
| $t_{PZL}$  |                 |                |                                                     |     |     |              |     | 2            | 8   |      |
| $t_{PHZ}$  | TCK↓            | A or B         |                                                     |     |     |              |     | 3            | 14  | ns   |
| $t_{PLZ}$  |                 |                |                                                     |     |     |              |     | 3            | 14  |      |
| $t_{PHZ}$  | TCK↓            | TDO            |                                                     |     |     |              |     | 2            | 8   | ns   |
| $t_{PLZ}$  |                 |                |                                                     |     |     |              |     | 2            | 8   |      |

NOTE 4: Preliminary specifications based on SPICE analysis

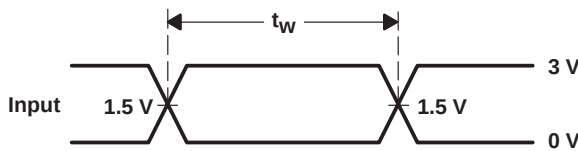
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## PARAMETER MEASUREMENT INFORMATION

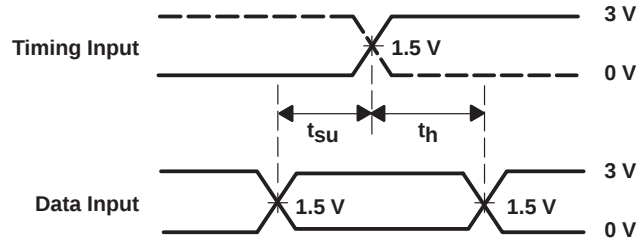


LOAD CIRCUIT FOR OUTPUTS

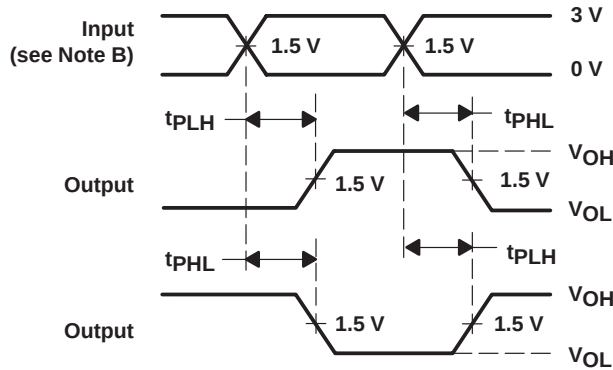
| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | Open |



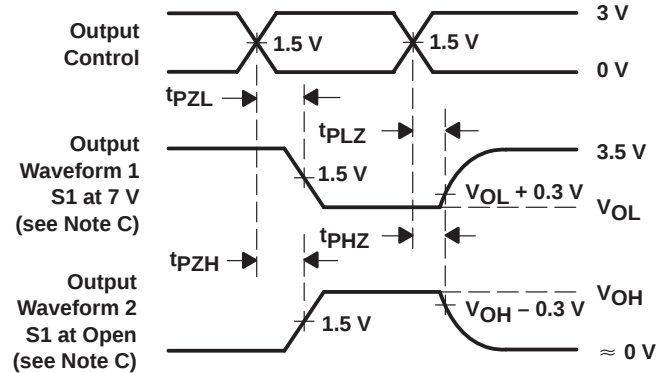
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NON-INVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

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