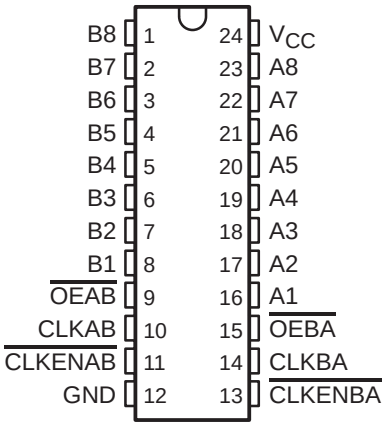
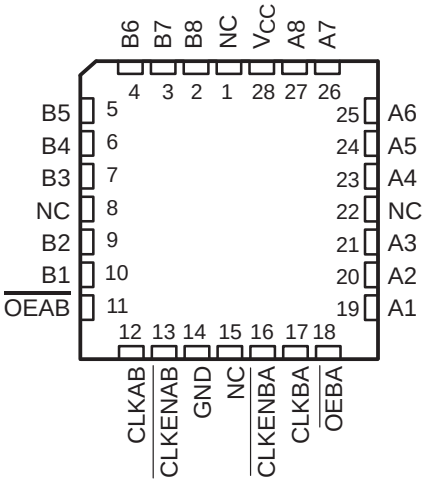
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Two 8-Bit Back-to-Back Registers Store Data Flowing in Both Directions**
- **Noninverting Outputs**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54ABT2952 . . . JT PACKAGE
SN74ABT2952 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT2952 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ′ABT2952 consists of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) input is low. Taking the output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) input low accesses the data on either port.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT2952 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT2952 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT2952 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

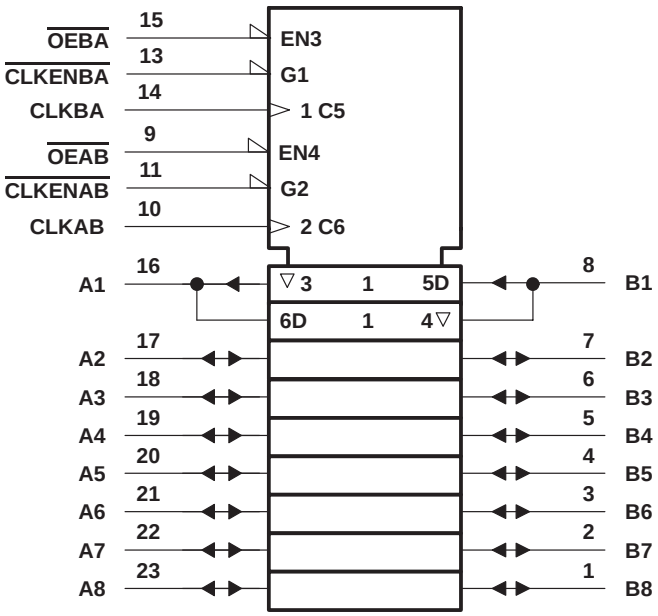
EPIC-IIB is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{\text{CLKENAB}}$	CLKAB	$\overline{\text{OEAB}}$	A	B
H	X	L	X	B_0‡
X	H or L	L	X	B_0‡
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses $\overline{\text{CLKENBA}}$, CLKBA, and $\overline{\text{OEBA}}$.
‡ Level of B before the indicated steady-state input conditions were established.

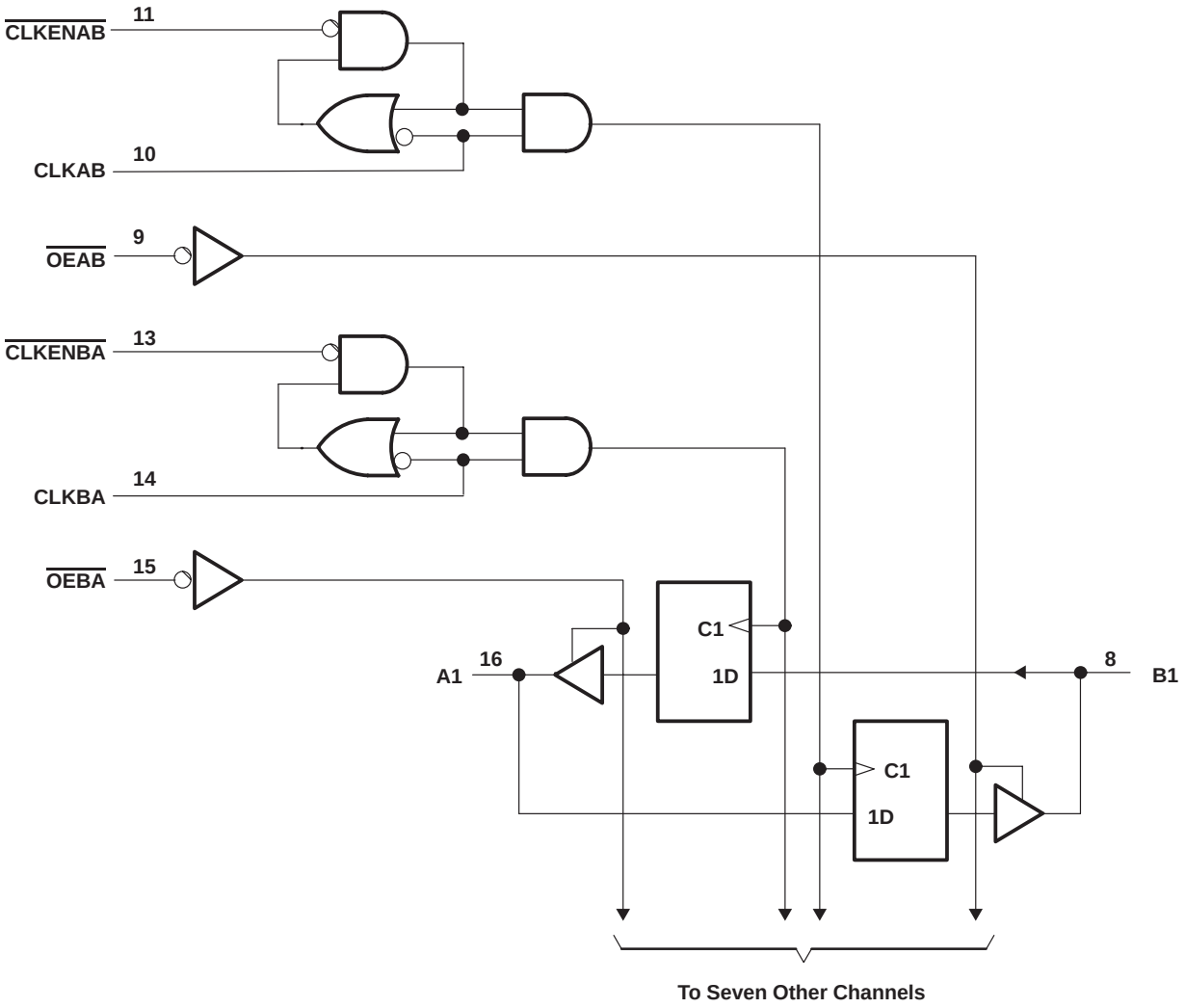
logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and NT packages.

PRODUCT PREVIEW

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT2952 . . . . . 96 mA
SN74ABT2952 . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package . . . . . 0.7 W
DW package . . . . . 1 W
NT package . . . . . 1.3 W
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			SN54ABT2952		SN74ABT2952		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT2952		SN74ABT2952		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = –18 mA					–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = – 3 mA			2.5			2.5		2.5		V
	V_{CC} = 5 V, I_{OH} = – 3 mA			3			3		3		
	V_{CC} = 4.5 V, I_{OH} = –24 mA			2			2				
	V_{CC} = 4.5 V, I_{OH} = – 32 mA			2‡					2		
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA					0.55		0.55			V
	V_{CC} = 4.5 V, I_{OL} = 64 mA					0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}§	V_{CC} = 5.5 V, V_O = 2.7 V					50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V, V_O = 0.5 V					–50		–50		–50	µA
I_{off}	V_{CC} = 0, V_I or $V_O \le$ 4.5 V					±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V, V_O = 2.5 V			–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		1	250		250		250	µA
			Outputs low		24	35		35		35	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3.5						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		7.5						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				V_{CC} = 5 V, T_A = 25°C		SN54ABT2952		SN74ABT2952		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			0	150	0	150	0	150	MHz
t_w	Pulse duration		CLK high	3		3		3		ns
			CLK low	3.5		3.5		3.5		
t_{su}	Setup time before CLK↑	A or B	High	4		4		4		ns
			Low	3		3		3		
		$\overline{\text{CLKEN}}$	High	3.5		3.5		3.5		
			Low	2.5		2.5		2.5		
t_h	Hold time after CLK↑	A or B		0		0		0		ns
		$\overline{\text{CLKEN}}$		0		0		0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT2952		SN74ABT2952		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150			150		150		MHz
t_{PLH}	CLKAB or CLKBA	B or A								ns
t_{PHL}										
t_{PZH}	OEBA or OEAB	A or B								ns
t_{PZL}										
t_{PHZ}	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$	A or B								ns
t_{PLZ}										

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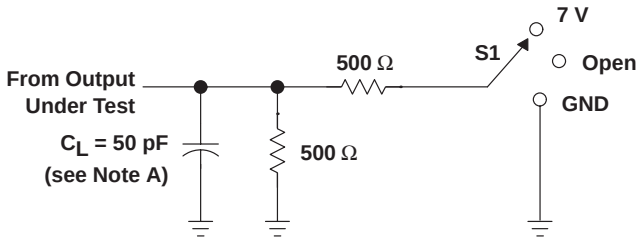
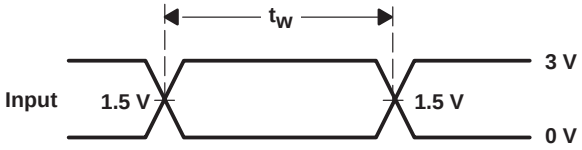
PARAMETER MEASUREMENT INFORMATION

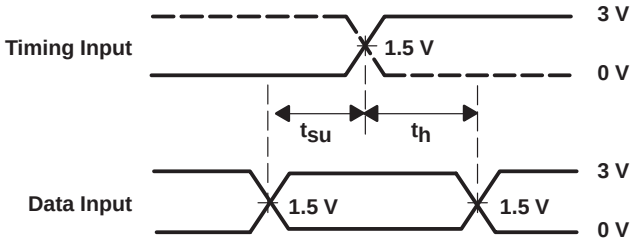


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

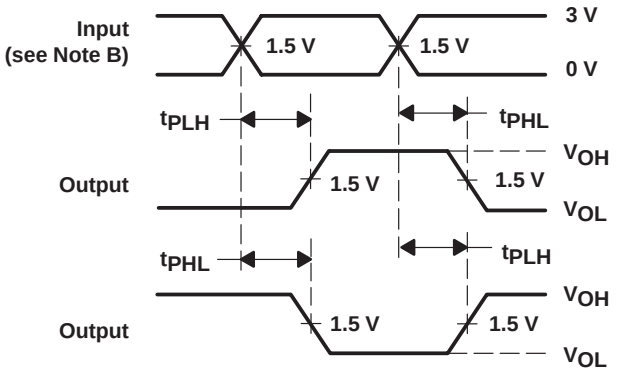
LOAD CIRCUIT FOR OUTPUTS



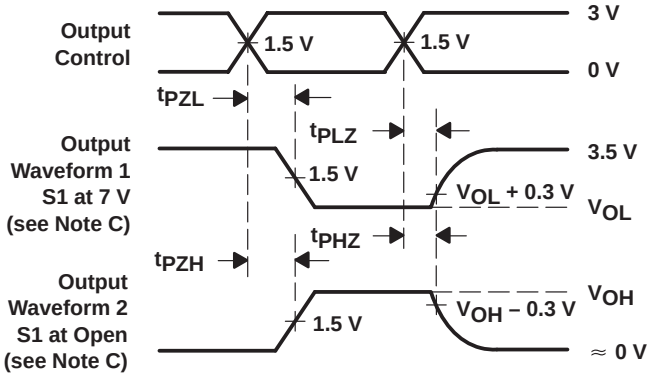
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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