

SN54LVTH543, SN74LVTH543 3.3-V ABT OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS704D – AUGUST 1997 – REVISED APRIL 1999

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Thin Very Small-Outline (DGV) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (JT) DIPs

description

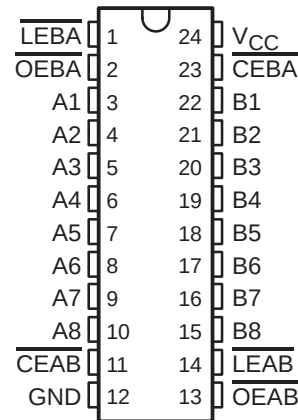
These octal transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH543 devices contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

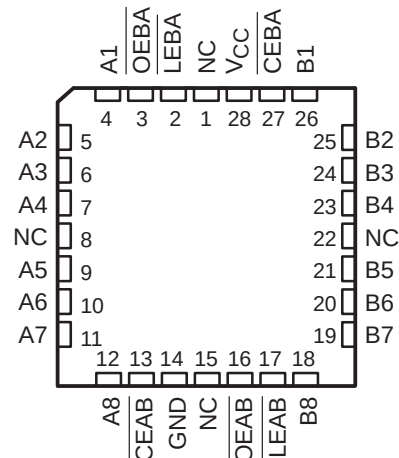
The A-to-B enable ($\overline{CEAB}$) input must be low to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

SN54LVTH543 . . . JT OR W PACKAGE
SN74LVTH543 . . . DB, DGV, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTH543 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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INSTRUMENTS**

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description (continued)

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN54LVTH543 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH543 is characterized for operation from -40°C to 85°C .

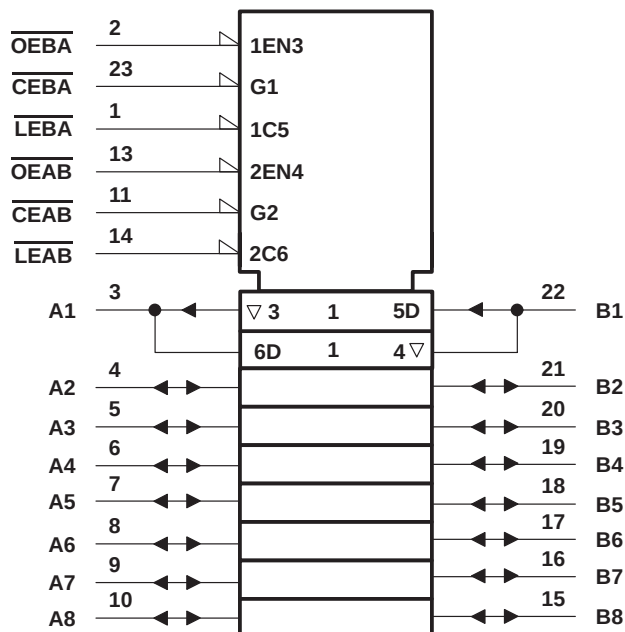
FUNCTION TABLE[†]

INPUTS				OUTPUT B
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	$B_0^{\ddagger}$
L	L	L	L	L
L	L	L	H	H

[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.

[‡] Output level before the indicated steady-state input conditions were established

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DGV, DW, JT, PW, and W packages.

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The diagram illustrates a 16-to-1 multiplexer implemented using four 3-to-1 multiplexers (labeled C1 1D) and four 2-to-1 multiplexers (represented by triangles). The inputs are grouped into four 4-bit buses: OEBA (2, 23), CEBA (1, 13), LEBA (11, 14), and LEAB (3, 22). The output is B1 (22). The logic involves selecting one of the four 4-bit inputs based on the 4-bit select input (A1, 3) and routing it to the output. The diagram shows the internal connections between the multiplexers and the final output B1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH543	96 mA
SN74LVTH543	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH543	48 mA
SN74LVTH543	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	104°C/W
DGV package	139°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T_{sta}	−65°C to 150°C

NOTES:

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JEDEC 51.

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recommended operating conditions (see Note 4)

			SN54LVTH543		SN74LVTH543		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate			200		200	μ s/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH543			SN74LVTH543			UNIT	
				MIN	TYP†	MAX	MIN	TYP†	MAX		
V _{IK}		V _{CC} = 2.7 V, I _I = −18 mA		−1.2			−1.2			V	
V _{OH}		V _{CC} = 2.7 V to 3.6 V, I _{OH} = −100 μA		V _{CC} −0.2			V _{CC} −0.2			V	
		V _{CC} = 2.7 V, I _{OH} = −8 mA		2.4			2.4				
		V _{CC} = 3 V	I _{OH} = −24 mA	2							
			I _{OH} = −32 mA				2				
V _{OL}		V _{CC} = 2.7 V	I _{OL} = 100 μA	0.2			0.2			V	
			I _{OL} = 24 mA	0.5			0.5				
			V _{CC} = 3 V	I _{OL} = 16 mA	0.4			0.4			
		I _{OL} = 32 mA		0.5			0.5				
		I _{OL} = 48 mA		0.55							
		I _{OL} = 64 mA					0.55				
		I _I	Control inputs	V _{CC} = 3.6 V, V _I = V _{CC} or GND		±1			±1		
V _{CC} = 0 or 3.6 V, V _I = 5.5 V				10			10				
A or B ports‡	V _{CC} = 3.6 V		V _I = 5.5 V		20			20			
			V _I = V _{CC}		1			1			
			V _I = 0		−5			−5			
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V					±100			μA	
I _I (hold)	A or B ports	V _{CC} = 3 V	V _I = 0.8 V		75			75			μA
			V _I = 2 V		−75			−75			
		V _{CC} = 3.6 V§		V _I = 0 to 3.6 V					±500		
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 to 3 V, OE = don't care		±100*			±100			μA	
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 to 3 V, OE = don't care		±100*			±100			μA	
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		0.19			0.19			mA
			Outputs low		5			5			
			Outputs disabled		0.19			0.19			
ΔI _{CC} ¶		V _{CC} = 3 V to 3.6 V, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		0.2			0.2			mA	
C _i		V _I = 3 V or 0		4			4			pF	
C _{io}		V _O = 3 V or 0		9			9			pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused terminals are at $V_{CC}\text{ or GND}$.

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

|| This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				SN54LVTH543				SN74LVTH543				UNIT
				$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration,	$\overline{LEAB}$ or $\overline{LEBA}$ low		3.3		3.3		3.3		3.3		ns
t_{su}	Setup time	A or B before $\overline{LEAB}$ or $\overline{LEBA}\uparrow$	Data high	0.4		0.4		0.4		0.4		ns
			Data low	1		1.5		1		1.5		
		A or B before $\overline{CEAB}$ or $\overline{CEBA}\uparrow$	Data high	0.2		0.2		0.2		0.2		
			Data low	0.7		1.2		0.7		1.2		
t_h	Hold time	A or B after $\overline{LEAB}$ or $\overline{LEBA}\uparrow$	Data high	1.5		0.6		1.5		0.6		ns
			Data low	1.3		1.5		1.3		1.5		
		A or B after $\overline{CEAB}$ or $\overline{CEBA}\uparrow$	Data high	1.6		0.5		1.6		0.5		
			Data low	1.4		1.6		1.4		1.6		

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH543				SN74LVTH543				UNIT	
			$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t _{PLH}	A or B	B or A	1.2	3.9	4.5		1.3	2.5	3.7	4.3		ns
t _{PHL}			1.2	3.9	4.5		1.3	2.5	3.7	4.3		
t _{PLH}	$\overline{LE}$	A or B	1.2	5.1	6.1		1.3	2.9	4.7	5.9		ns
t _{PHL}			1.2	5.1	6.1		1.3	2.9	4.7	5.9		
t _{PZH}	$\overline{OE}$	A or B	1	5.1	6.4		1.1	2.9	4.9	6.2		ns
t _{PZL}			1	5.1	6.4		1.1	3.2	4.9	6.2		
t _{PHZ}	$\overline{OE}$	A or B	1.9	5.6	6.2		2	3.4	5.3	5.9		ns
t _{PLZ}			1.9	5.6	6.2		2	3.7	5.3	5.9		
t _{PZH}	$\overline{CE}$	A or B	1.2	5.5	7		1.3	3.2	5.3	6.8		ns
t _{PZL}			1.2	5.5	7		1.3	3.5	5.3	6.8		
t _{PHZ}	$\overline{CE}$	A or B	2.2	5.7	6.2		2.3	3.8	5.4	5.9		ns
t _{PLZ}			2.2	5.7	5.9		2.3	3.9	5.4	5.6		

[†] All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

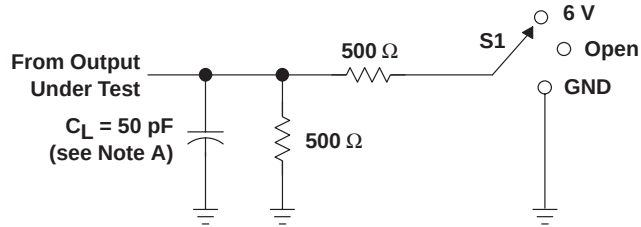
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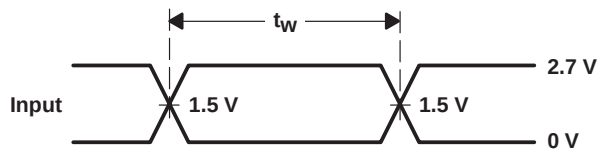
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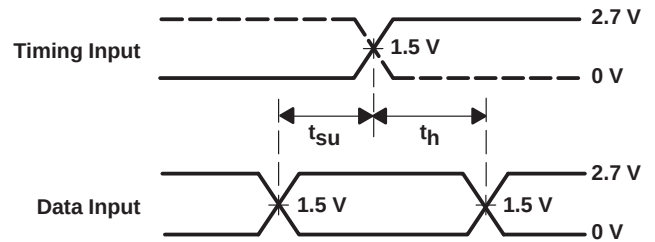
PARAMETER MEASUREMENT INFORMATION



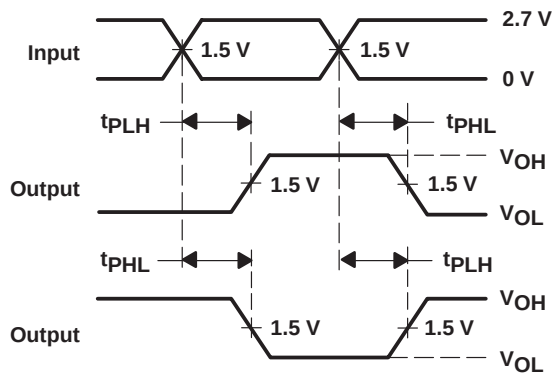
LOAD CIRCUIT



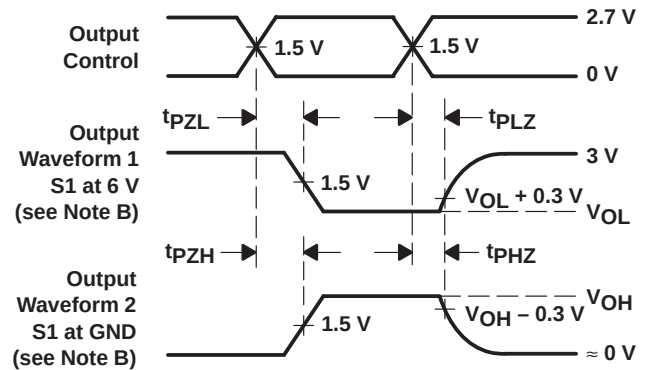
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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