

CD74FCT844A BiCMOS 9-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCBS728 – JULY 2000

- BiCMOS Technology With Low Quiescent Power
- Buffered Inputs
- Inverted Outputs
- Input/Output Isolation From V_{CC}
- Controlled Output Edge Rates
- 48-mA Output Sink Current
- Output Voltage Swing Limited to 3.7 V
- SCR Latch-Up-Resistant BiCMOS Process and Circuit Design
- Packaged in Standard Plastic DIP

description

The CD74FCT844A is a 9-bit, D-type latch with 3-state outputs, designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

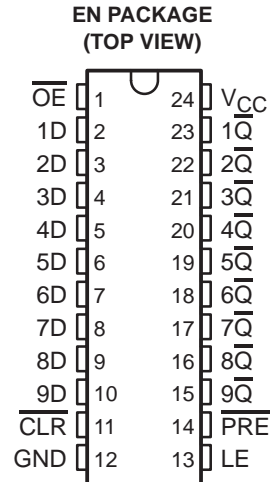
The device uses a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output high level to two diode drops below V_{CC} . This resultant lowering of output swing (0 V to 3.7 V) reduces power-bus ringing [a source of electromagnetic interference (EMI)] and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 mA.

The CD74FCT844A outputs are transparent to the inputs when the latch-enable (LE) input is high. When LE goes low, the data is latched. The output-enable (\overline{OE}) input controls the 3-state outputs. When \overline{OE} is high, the outputs are in the high-impedance state. The latch operation is independent of the state of \overline{OE} . This device, having preset (\overline{PRE}) and clear (\overline{CLR}), is ideal for parity-bus interfacing. When \overline{PRE} is low, the outputs are high if \overline{OE} is low. \overline{PRE} overrides \overline{CLR} . When \overline{CLR} is low, the outputs are low if \overline{OE} is low. When \overline{CLR} is high, data can be entered into the latch.

\overline{OE} can be used to place the nine outputs in either a normal logic state (high or low logic levels) or the high-impedance state. The outputs also are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The CD74FCT844A is characterized for operation from 0°C to 70°C.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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INSTRUMENTS**

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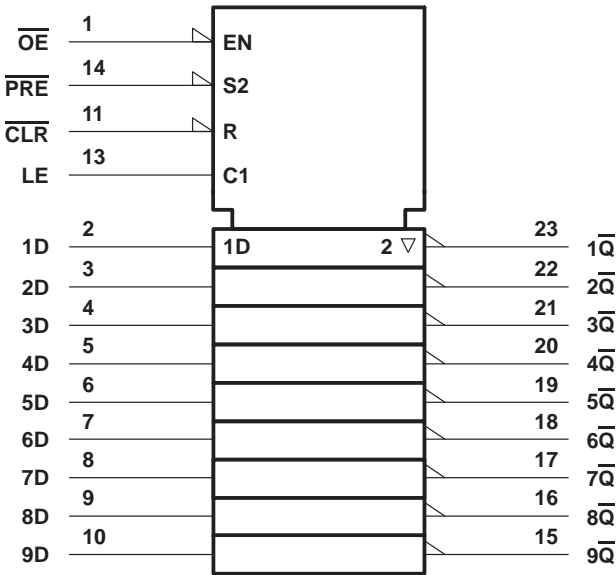
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FUNCTION TABLE
(each latch)

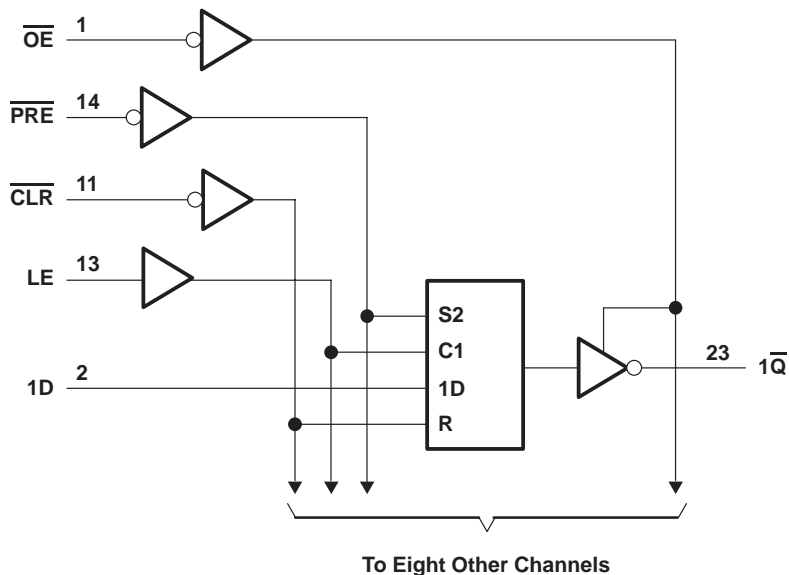
INPUTS					OUTPUT
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	$\overline{\text{OE}}$	LE	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	H
H	H	L	H	H	L
H	H	L	L	X	Q_0
X	X	H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

DC supply voltage range, V_{CC}	–0.5 V to 6 V
DC input clamp current, I_{IK} ($V_I < -0.5$ V)	–20 mA
DC output clamp current, I_{OK} ($V_O < -0.5$ V)	–50 mA
DC output sink current per output pin, I_{OL}	70 mA
DC output source current per output pin, I_{OH}	–30 mA
Continuous current through V_{CC} , (I_{CC})	237 mA
Continuous current through GND	453 mA
Package thermal impedance, θ_{JA} (see Note 1)	67°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JEDEC 51.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–15	mA
I_{OL}	Low-level output current		48	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	0	70	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
V _{IK}	I _I = -18 mA	4.75 V		-1.2	-1.2		V
V _{OH}	I _{OH} = -15 mA	4.75 V	2.4		2.4		V
V _{OL}	I _{OL} = 48 mA	4.75 V		0.55	0.55		V
I _I	V _I = V _{CC} or GND	5.25 V	±0.1		±1		μA
I _{OZ}	V _O = V _{CC} or GND	5.25 V	±0.5		±10		μA
I _{OS} [†]	V _I = V _{CC} or GND, V _O = 0	5.25 V	-75		-75		mA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.25 V	8		80		μA
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at V _{CC} or GND	5.25 V	1.6		1.6		mA
C _i	V _I = V _{CC} or GND			10	10		pF
C _o	V _O = V _{CC} or GND			15	15		pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 100 ms.

[‡] This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating temperature conditions (unless otherwise noted) (see Figure 1)

		MIN	MAX	UNIT
t _w Pulse duration	CLR low	8		ns
	PRE low	8		
	LE low	4		
t _{su} Setup time	Data before LE↓	2.5		ns
	PRE inactive	2.5		
	CLR inactive	2.5		
t _h Hold time	Data before LE↓	2.5		ns
t _{rec} Recovery time	PRE, CLR	14		ns

switching characteristics over recommended operating temperature conditions (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C	MIN	MAX	UNIT
			TYP			
t _{pd}	D	\bar{Q}	7.5	1.5	10	ns
	LE		9	1.5	12	
t _{PLH}	PRE	\bar{Q}	9	1.5	12	ns
t _{PHL}	CLR		9.8	1.5	13	
t _{en}	OE	\bar{Q}	10.5	1.5	14	ns
t _{dis}	OE	\bar{Q}	6	1.5	8	ns



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noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		1		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		0.5		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

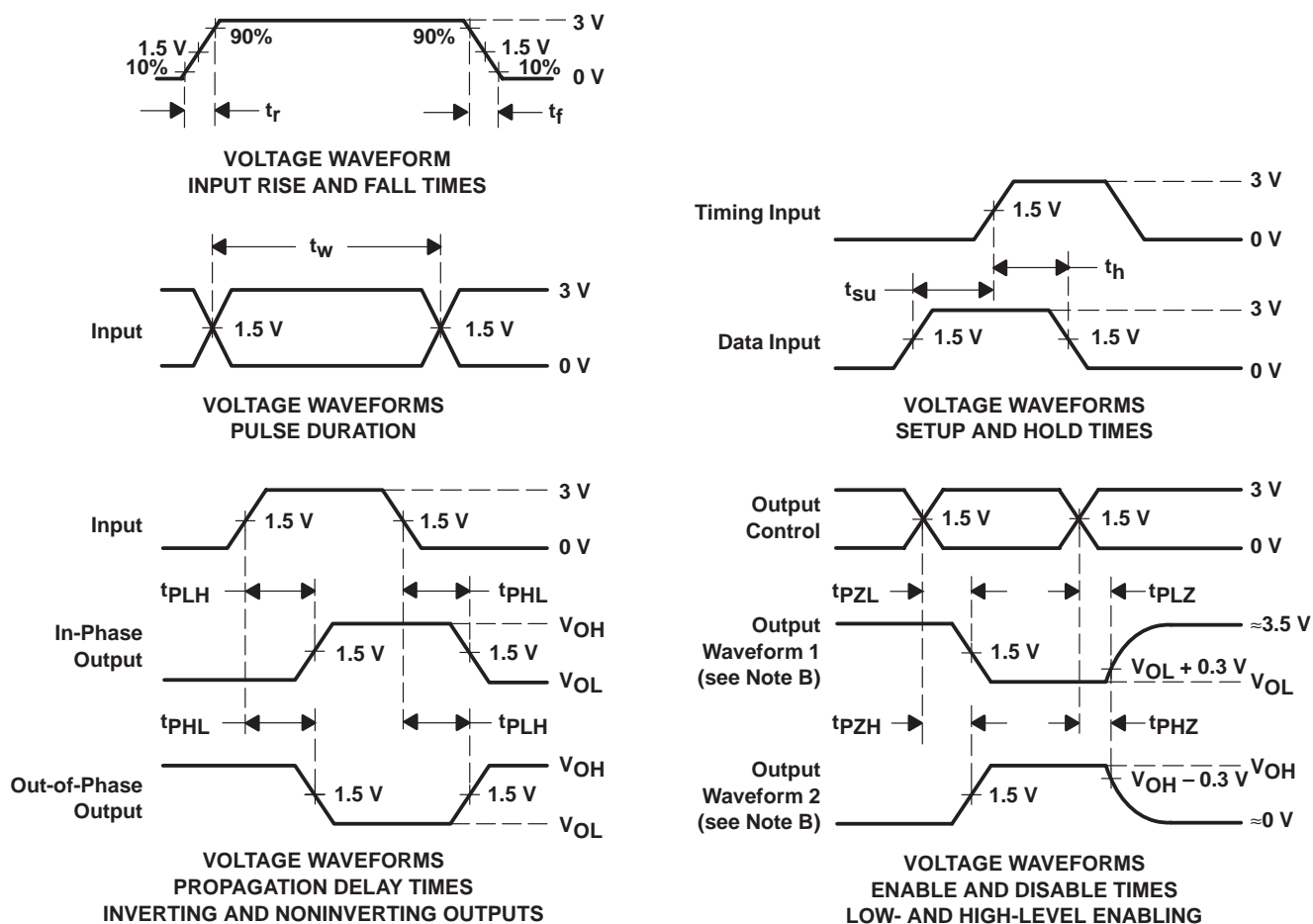
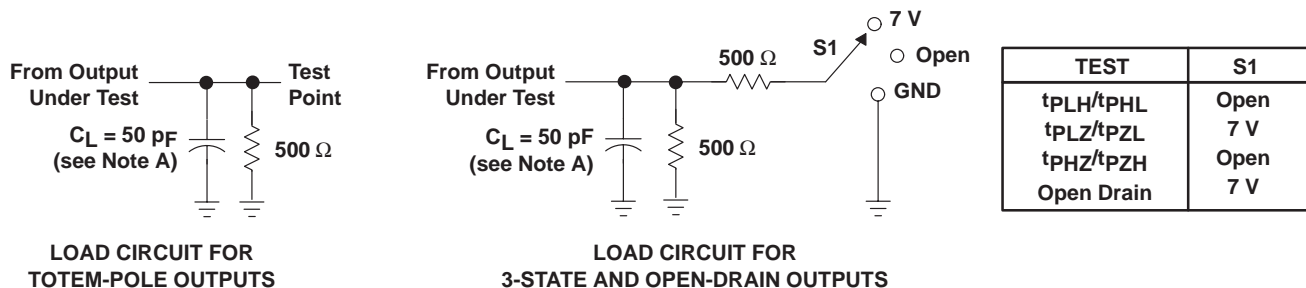
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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, t_r and $t_f = 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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