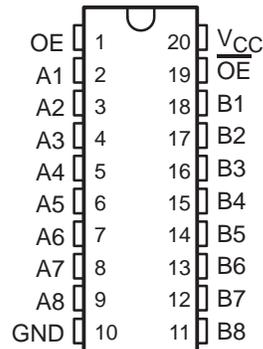


# SN74CBT3345 8-BIT FET BUS SWITCH

SCDS027E – MAY 1995 – REVISED MAY 2000

- Standard '245-Type Pinout
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Shrink Small-Outline (DB, DBQ), Thin Very Small-Outline (DGV), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages

DB, DBQ, DGV, DW, OR PW PACKAGE  
(TOP VIEW)



## description

The SN74CBT3345 provides eight bits of high-speed TTL-compatible bus switching in a standard '245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

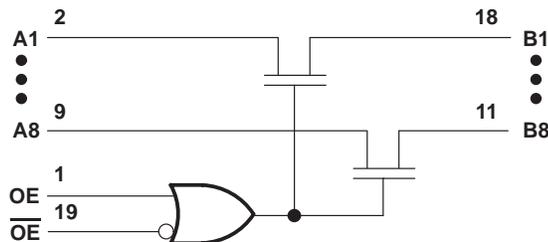
The device is organized as one 8-bit switch bank with dual output-enable ( $\overline{OE}$  and  $OE$ ) inputs. When  $\overline{OE}$  is low or  $OE$  is high, the switch is on, and port A is connected to port B. When  $\overline{OE}$  is high and  $OE$  is low, the switch is open, and a high-impedance state exists between the two ports.

The SN74CBT3345 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

## logic diagram (positive logic)



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**TEXAS  
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# SN74CBT3345

## 8-BIT FET BUS SWITCH

SCDS027E – MAY 1995 – REVISED MAY 2000

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, $I_{IK}$ ( $V_{I/O} < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
DB package	70°C
DBQ package	68°C
DGV package	92°C
DW package	58°C
PW package	83°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5.5	V
$V_{IH}$ High-level control input voltage	2		V
$V_{IL}$ Low-level control input voltage		0.8	V
$T_A$ Operating free-air temperature	0	70	°C

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT	
$V_{IK}$	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			–1.2	V	
$I_I$	$V_{CC} = 5.5$ V,	$V_I = 5.5$ V or GND			±1	µA	
$I_{CC}$	$V_{CC} = 5.5$ V,	$I_O = 0$ , $V_I = V_{CC}$ or GND			50	µA	
$\Delta I_{CC}$ §	Control inputs	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND			3.5	mA	
$C_i$	Control inputs	$V_I = 3$ V or 0			3	pF	
$C_{io(OFF)}$	$V_O = 3$ V or 0,	$\overline{OE} = V_{CC}$ or $OE = GND$			6	pF	
$r_{on}$ ¶	$V_{CC} = 4.5$ V	$V_I = 0$			5	7	Ω
					5	7	
		$V_I = 2.4$ V,	$I_I = 15$ mA	10	15		

‡ All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

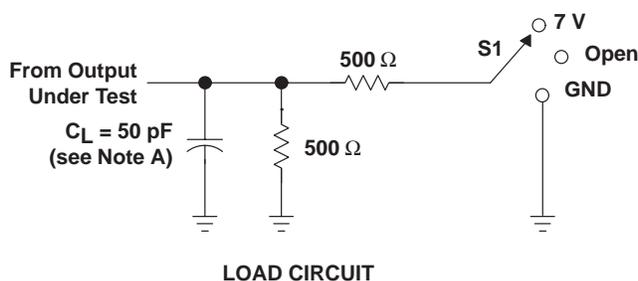


switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

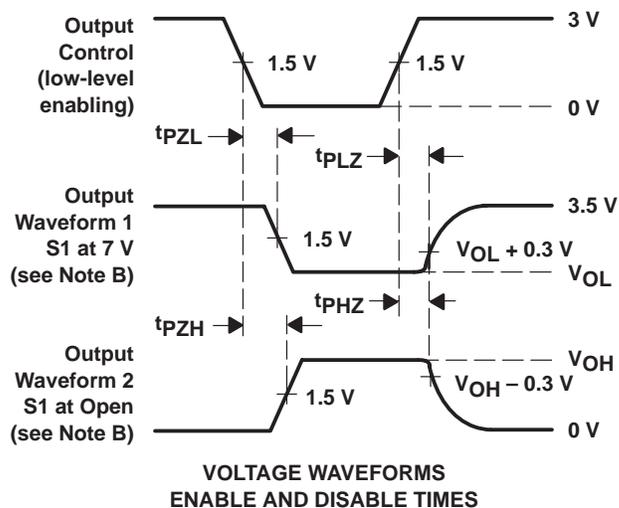
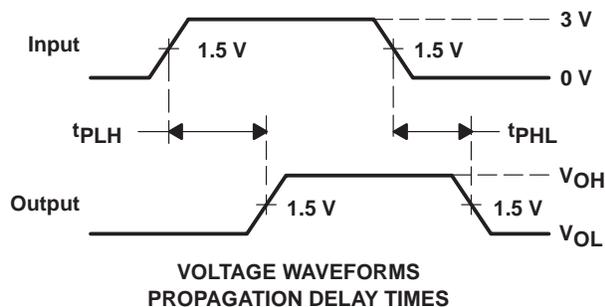
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	
$t_{pd}^\dagger$	A or B	B or A	0.25		ns
$t_{en}$	$\overline{OE}$ or OE	A or B	1	9.1	ns
$t_{dis}$	$\overline{OE}$ or OE	A or B	1	8.7	ns

† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10$  MHz,  $Z_O = 50$   $\Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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