

# SN74CBT162292

## 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

SCDS052D – MARCH 1998 – REVISED MAY 2000

- **TTL-Compatible Control Input Levels**
- **Isolation Under Power-Off Conditions**
- **Make-Before-Break Feature**
- **Internal 500- $\Omega$  Pulldown Resistors to Ground**
- **A-Port Inputs/Outputs Have Equivalent 25- $\Omega$  Series Resistors, So No External Resistors Are Required**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and Shrink Small-Outline (DL) Packages**

### description

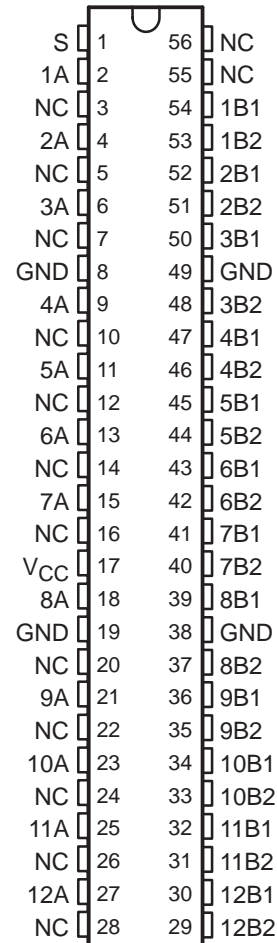
The SN74CBT162292 is a 12-bit 1-of-2 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When the select (S) input is low, port A is connected to port B1, and  $R_{INT}$  is connected to port B2. When S is high, port A is connected to port B2, and  $R_{INT}$  is connected to port B1.

The A-port inputs/outputs include equivalent 25- $\Omega$  series resistors to reduce overshoot and undershoot.

The SN74CBT162292 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

### DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC – No internal connection

### FUNCTION TABLE

INPUT S	FUNCTION
L	A port = B1 port $R_{INT}$ = B2 port
H	A port = B2 port $R_{INT}$ = B1 port



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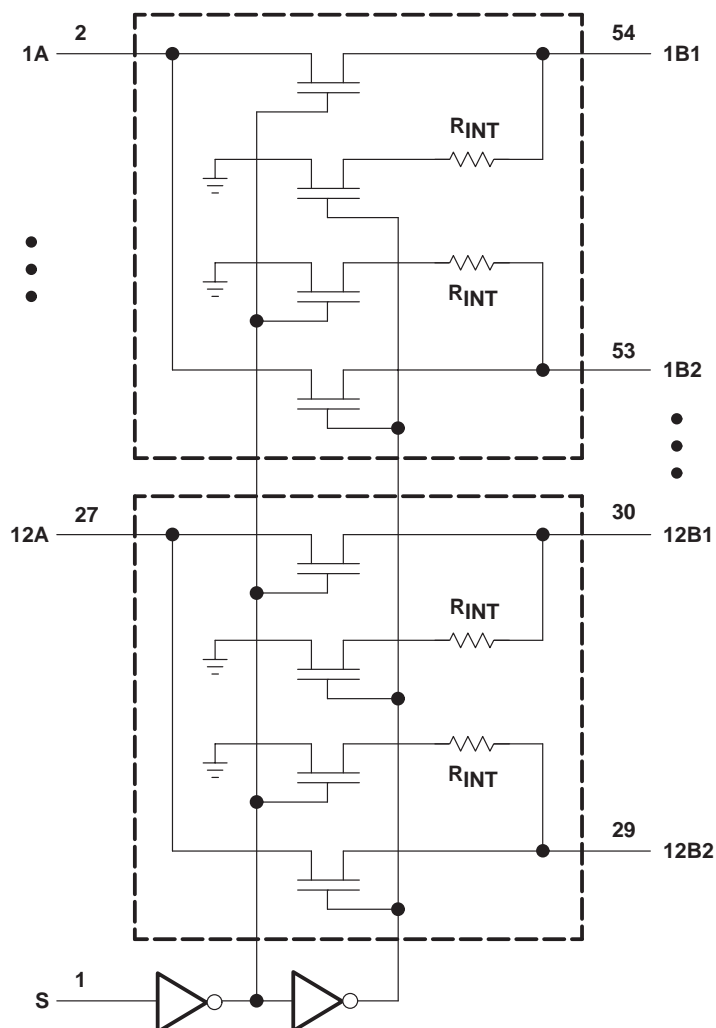
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### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
DGG package	64°C/W
DGV package	48°C/W
DL package	56°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51.



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**recommended operating conditions (see Note 3)**

	MIN	MAX	UNIT
V <sub>CC</sub> Supply voltage	4	5.5	V
V <sub>IH</sub> High-level control input voltage	2		V
V <sub>IL</sub> Low-level control input voltage		0.8	V
T <sub>A</sub> Operating free-air temperature	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = −18 mA			−1.2	V
I <sub>I</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub> or GND			±5	μA
I <sub>off</sub>		V <sub>CC</sub> = 0,	V <sub>I</sub> or V <sub>O</sub> = 0 to 7 V			10	μA
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V,	I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND			3	μA
ΔI <sub>CC</sub> ‡	Control input	V <sub>CC</sub> = 5.5 V,	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			2.5	mA
C <sub>i</sub>	Control input	V <sub>I</sub> = 3 V or 0				3.5	pF
C <sub>io</sub>		V <sub>CC</sub> = 0,	V <sub>O</sub> = 3 V or 0			8	pF
r <sub>on</sub> §		V <sub>CC</sub> = 4 V, TYP at V <sub>CC</sub> = 4 V	V <sub>I</sub> = 2.4 V, I <sub>I</sub> = 15 mA			38 55	Ω
		V <sub>CC</sub> = 4.5 V	V <sub>I</sub> = 0	I <sub>I</sub> = 45 mA		39 63	
				I <sub>I</sub> = 30 mA		37 55	
			V <sub>I</sub> = 2.4 V, I <sub>I</sub> = 15 mA			37 55	

† All typical values are at V<sub>CC</sub> = 5 V (unless otherwise noted), T<sub>A</sub> = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

**switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF, (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t <sub>pd</sub> ¶	A or B	B or A		1.9		1.85	ns
t <sub>en</sub>	S	A or B	1	10.7	1	9.5	ns
t <sub>dis</sub>	S	A or B	1	10.9	1	9.7	ns

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

**switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF, (unless otherwise noted) (see Figure 1)**

PARAMETER	DESCRIPTION	V <sub>CC</sub> = 4 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
		MIN	MAX	MIN	MAX	
t <sub>mhb</sub> #	Make-before-break time	0	2	0	2	ns

# The make-before-break time is the time interval between make and break, during the transition from one selected port to the other.



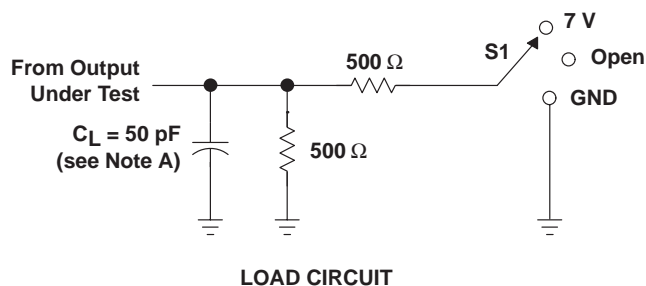
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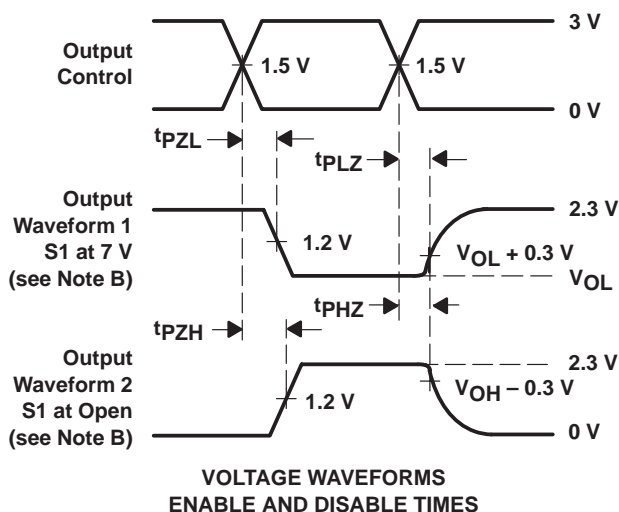
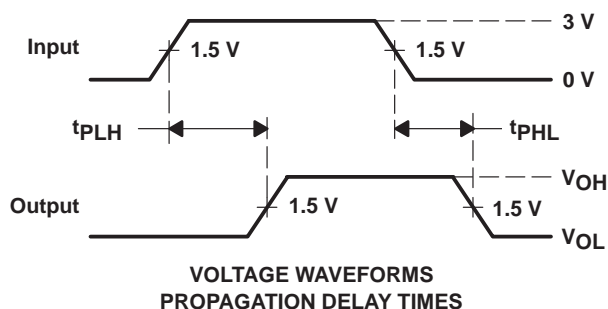
### WITH INTERNAL PULLDOWN RESISTORS

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#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{pd}$	Open
$t_{PZL}/t_{PLZ}$	7 V
$t_{PZH}/t_{PHZ}$	Open



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when connected to the internal 500- $\Omega$  pulldown resistor. Waveform 2 is for an output with internal conditions such that the output is high except when connected to the internal 500- $\Omega$  pulldown resistor.
  - All pulse inputs and DC inputs are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  $Z = R_{INT} = 500 \Omega$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  $Z = R_{INT} = 500 \Omega$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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