

SN74CBTK32245
32-BIT FET BUS SWITCH
WITH ACTIVE-CLAMP UNDERSHOOT-PROTECTION CIRCUIT
SCDS106B – APRIL 2000 – REVISED JULY 2000

- Member of the Texas Instruments *Widebus+*™ Family
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- I_{off} Supports Partial-Power-Down Mode Operation
- Active-Clamp Undershoot-Protection Circuit on the I/Os Clamps Undershoots Up to -2 V
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Packaged in Plastic Fine-Pitch Ball Grid Array Package

description

The SN74CBTK32245 device provides 32 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The A and B ports have an active-clamp undershoot-protection circuit. When there is an undershoot, the active-clamp circuit is enabled and current from V_{CC} is supplied to clamp the output, preventing the pass transistor from turning on.

The device is organized as four 8-bit bus switches, two 16-bit bus switches, or one 32-bit bus switch. When output-enable (\overline{OE}) input is low, the switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open and a high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The SN74CBTK32245 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE
(each 8-bit bus switch)

INPUT \overline{OE}	FUNCTION
L	A port = B port
H	Disconnect



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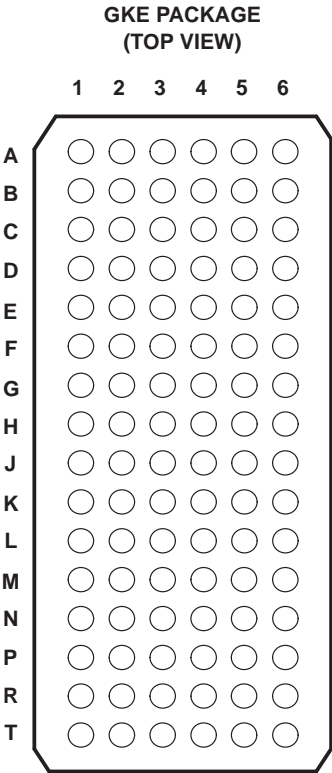
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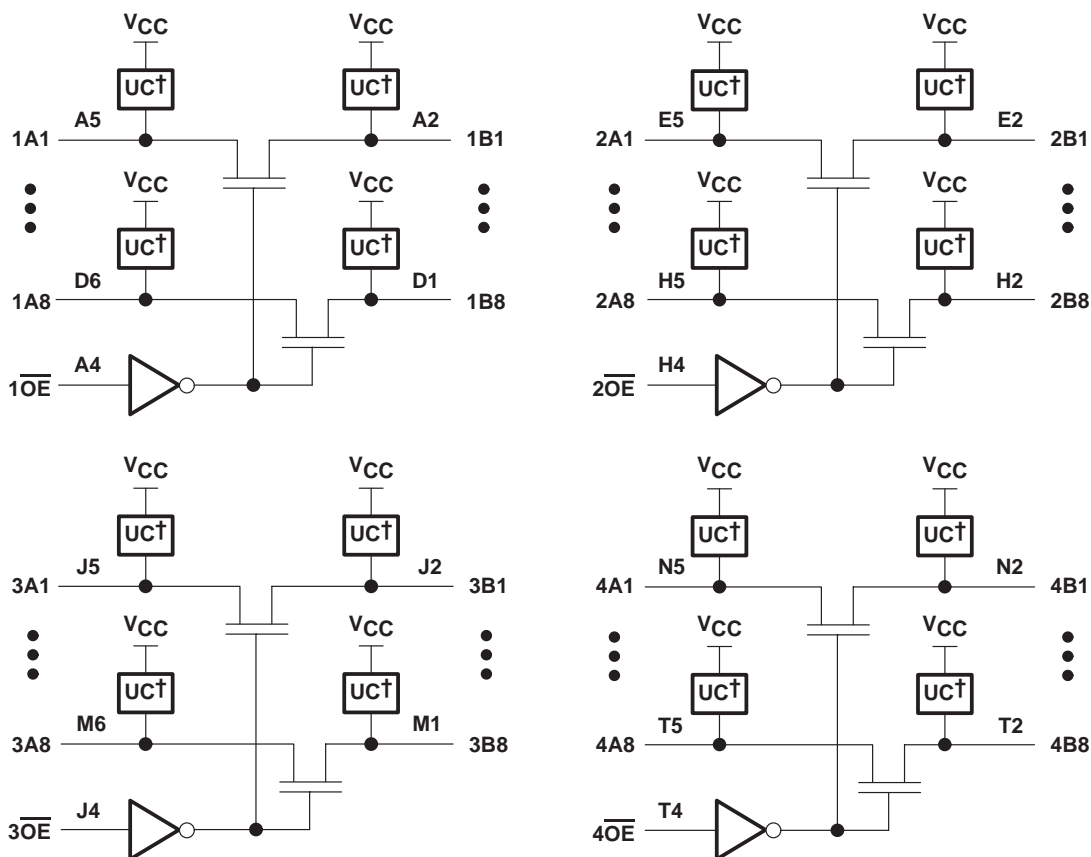


terminal assignments

	1	2	3	4	5	6
A	1B2	1B1	NC	1OE	1A1	1A2
B	1B4	1B3	GND	GND	1A3	1A4
C	1B6	1B5	VCC	VCC	1A5	1A6
D	1B8	1B7	GND	GND	1A7	1A8
E	2B2	2B1	GND	GND	2A1	2A2
F	2B4	2B3	VCC	VCC	2A3	2A4
G	2B6	2B5	GND	GND	2A5	2A6
H	2B7	2B8	NC	2OE	2A8	2A7
J	3B2	3B1	NC	3OE	3A1	3A2
K	3B4	3B3	GND	GND	3A3	3A4
L	3B6	3B5	VCC	VCC	3A5	3A6
M	3B8	3B7	GND	GND	3A7	3A8
N	4B2	4B1	GND	GND	4A1	4A2
P	4B4	4B3	VCC	VCC	4A3	4A4
R	4B6	4B5	GND	GND	4A5	4A6
T	4B7	4B8	NC	4OE	4A8	4A7

NC – No internal connection

logic diagram (positive logic)



† Undershoot clamp

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2)	40°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

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SCDS106B – APRIL 2000 – REVISED JULY 2000

recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
V_{CC} Supply voltage	4	5.5	V
V_{IH} High-level control input voltage	2		V
V_{IL} Low-level control input voltage		0.8	V
T_A Operating free-air temperature	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}		V _{CC} = 4.5 V, I _I = −18 mA				−1.2	V
V _{IKU}		V _{CC} = 5.5 V, 0 mA ≥ I _I ≥ −50 mA, \overline{OE} = 5.5 V				−2	V
I _I		V _{CC} = 5.5 V, V _I = 5.5 V or GND				±5	μA
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 5.5 V				20	μA
I _{CC}		V _{CC} = 5.5 V, V _I = V _{CC} or GND, I _O = 0				60	μA
ΔI _{CC} ‡	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND				3.5	mA
C _i	Control inputs	V _I = 3 V or 0				3.5	pF
C _{io} (OFF)		V _O = 3 V or 0, \overline{OE} = V _{CC}				5.5	pF
r _{on} §	V _{CC} = 4 V, TYP at V _{CC} = 4 V		V _I = 2.4 V, I _I = 15 mA			14 20	Ω
	V _{CC} = 4.5 V	V _I = 0	I _I = 64 mA		5 7		
			I _I = 30 mA		5 7		
			V _I = 2.4 V, I _I = 15 mA		8 12		

† All typical values are at $V_{CC} = 5$ V (unless otherwise noted), $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL-voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4$ V		$V_{CC} = 5$ V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}^\P	A or B	B or A	0.35		0.25		ns
t_{en}	\overline{OE}	A or B	7.4		1.6	4.9	ns
t_{dis}	\overline{OE}	A or B	7.4		4.2	7.5	ns

† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OUTU}	See Figures 1 and 2, and Table 1	2	$V_{OH}-0.3$		V

† All typical values are at $V_{CC} = 5\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

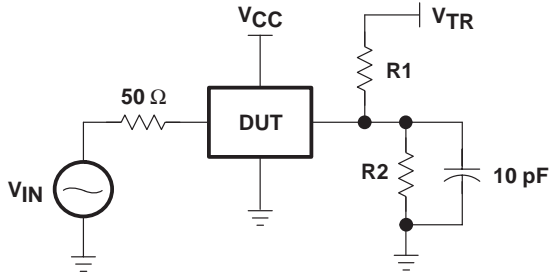


Figure 1. Device Test Setup

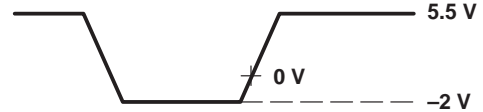


Figure 2. Transient Input Voltage Waveform

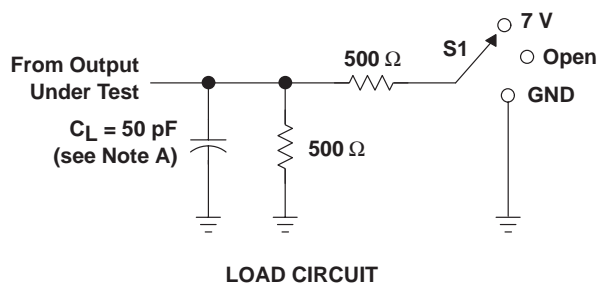
Table 1. Device Test Conditions

PARAMETER	VALUE	UNIT
B port under test†	See Figure 1	
V_{IN}	See Figure 2	V
t_w	20	ns
t_r	2	ns
t_f	2	ns
$R1 = R2$	100	k Ω
V_{TR}	11	V
V_{CC}	5.5	V

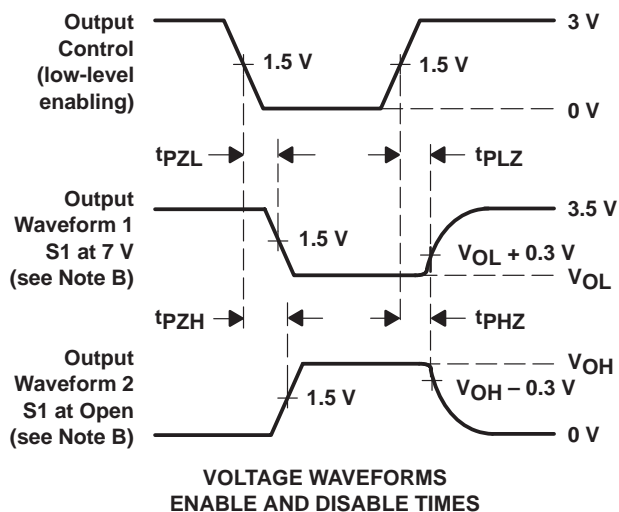
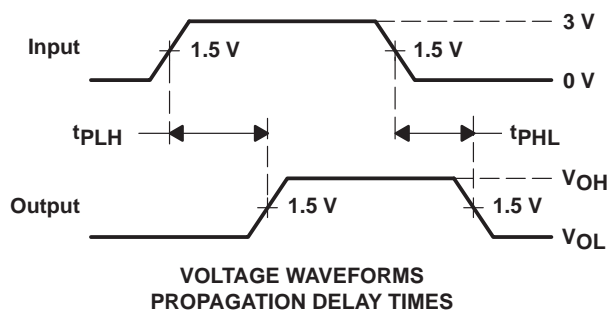
† Other B-port outputs are open

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 SCDS106B – APRIL 2000 – REVISED JULY 2000

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

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