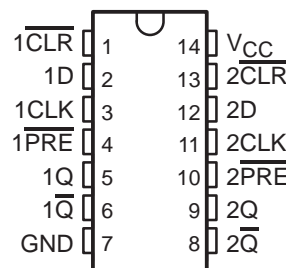


# SN54LV74A, SN74LV74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

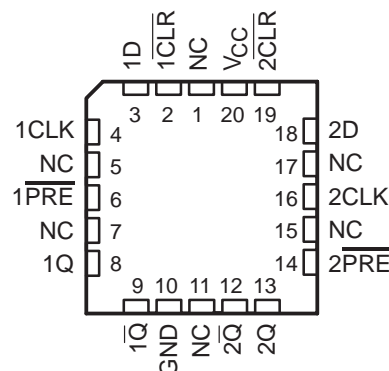
SCLS381E – AUGUST 1997 – REVISED MAY 2000

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical  $V_{OLP}$  (Output Ground Bounce)**  
 $<0.8\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$
- **Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)**  
 $>2.3\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$
- **2-V to 5.5-V  $V_{CC}$  Operation**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200\text{ pF}$ ,  $R = 0$ )**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

SN54LV74A ... J OR W PACKAGE  
SN74LV74A ... D, DB, DGV, NS, OR PW PACKAGE  
(TOP VIEW)



SN54LV74A ... FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description

These dual positive-edge-triggered D-type flip-flops are designed for 2-V to 5.5-V  $V_{CC}$  operation.

A low level at the preset ( $\overline{\text{PRE}}$ ) or clear ( $\overline{\text{CLR}}$ ) inputs sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are inactive (high), data at the data (D) inputs meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The SN54LV74A is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74LV74A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

FUNCTION TABLE

| INPUTS                  |                         |     |   | OUTPUTS |                       |
|-------------------------|-------------------------|-----|---|---------|-----------------------|
| $\overline{\text{PRE}}$ | $\overline{\text{CLR}}$ | CLK | D | Q       | $\overline{\text{Q}}$ |
| L                       | H                       | X   | X | H       | L                     |
| H                       | L                       | X   | X | L       | H                     |
| L                       | L                       | X   | X | H†      | H†                    |
| H                       | H                       | ↑   | H | H       | L                     |
| H                       | H                       | ↑   | L | L       | H                     |
| H                       | H                       | L   | X | $Q_0$   | $\overline{Q}_0$      |

† This configuration is unstable; that is, it does not persist when  $\overline{\text{PRE}}$  or  $\overline{\text{CLR}}$  returns to its inactive (high) level.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC is a trademark of Texas Instruments.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

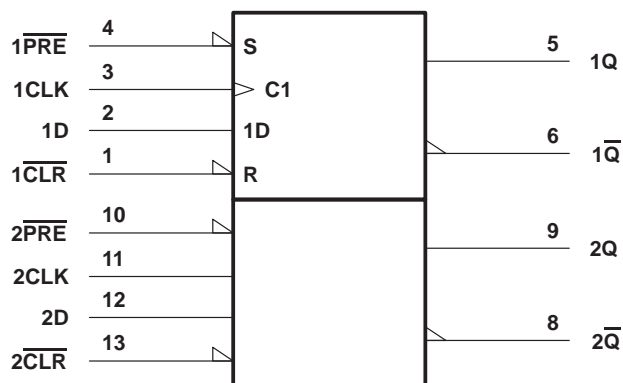
Copyright © 2000, Texas Instruments Incorporated

# SN54LV74A, SN74LV74A

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

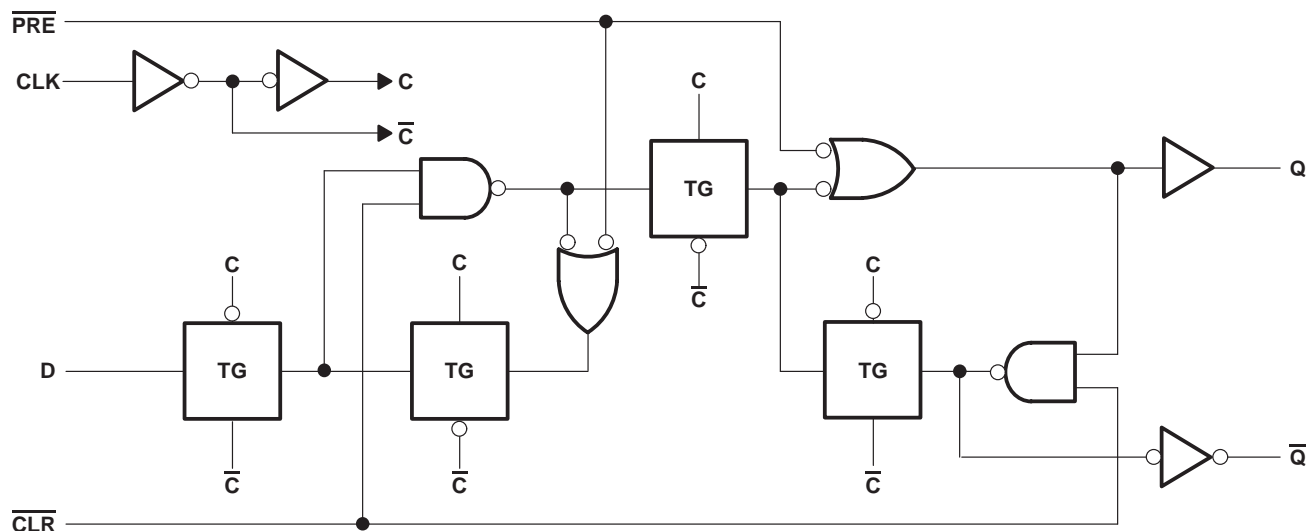
SCLS381E – AUGUST 1997 – REVISED MAY 2000

### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

### logic diagram, each flip-flop (positive logic)



# SN54LV74A, SN74LV74A

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

SCLS381E – AUGUST 1997 – REVISED MAY 2000

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|  |                            |
|--|----------------------------|
| Supply voltage range, $V_{CC}$   | –0.5 V to 7 V              |
| Input voltage range, $V_I$ (see Note 1)  | –0.5 V to 7 V              |
| Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) | –0.5 V to 7 V              |
| Output voltage range, $V_O$ (see Notes 1 and 2)  | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )  | –20 mA                     |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )                                   | ±50 mA                     |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )                                       | ±25 mA                     |
| Continuous current through $V_{CC}$ or GND   | ±50 mA                     |
| Package thermal impedance, $\theta_{JA}$ (see Note 3): D package                                 | 86°C/W                     |
| DB package   | 96°C/W                     |
| DGV package  | 127°C/W                    |
| NS package   | 76°C/W                     |
| PW package   | 113°C/W                    |
| Storage temperature range, $T_{stg}$   | –65°C to 150°C             |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
  2. This value is limited to 5.5 V maximum.
  3. The package thermal impedance is calculated in accordance with JESD 51.



# SN54LV74A, SN74LV74A

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

SCLS381E – AUGUST 1997 – REVISED MAY 2000

### recommended operating conditions (see Note 4)

|                 |                                    |                                  | SN54LV74A             |                 | SN74LV74A             |                 | UNIT |
|-----------------|------------------------------------|----------------------------------|-----------------------|-----------------|-----------------------|-----------------|------|
|                 |                                    |                                  | MIN                   | MAX             | MIN                   | MAX             |      |
| V <sub>CC</sub> | Supply voltage                     |                                  | 2                     | 5.5             | 2                     | 5.5             | V    |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 2 V            | 1.5                   |                 | 1.5                   |                 | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V | V <sub>CC</sub> × 0.7 |                 | V <sub>CC</sub> × 0.7 |                 |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | V <sub>CC</sub> × 0.7 |                 | V <sub>CC</sub> × 0.7 |                 |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | V <sub>CC</sub> × 0.7 |                 | V <sub>CC</sub> × 0.7 |                 |      |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 2 V            | 0.5                   |                 | 0.5                   |                 | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V | V <sub>CC</sub> × 0.3 |                 | V <sub>CC</sub> × 0.3 |                 |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | V <sub>CC</sub> × 0.3 |                 | V <sub>CC</sub> × 0.3 |                 |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | V <sub>CC</sub> × 0.3 |                 | V <sub>CC</sub> × 0.3 |                 |      |
| V <sub>I</sub>  | Input voltage                      |                                  | 0                     | 5.5             | 0                     | 5.5             | V    |
| V <sub>O</sub>  | Output voltage                     |                                  | 0                     | V <sub>CC</sub> | 0                     | V <sub>CC</sub> | V    |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 2 V            | −50                   |                 | −50                   |                 | μA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V | −2                    |                 | −2                    |                 | mA   |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | −6                    |                 | −6                    |                 |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | −12                   |                 | −12                   |                 |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 2 V            | 50                    |                 | 50                    |                 | μA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V | 2                     |                 | 2                     |                 | mA   |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | 6                     |                 | 6                     |                 |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | 12                    |                 | 12                    |                 |      |
| Δt/Δv           | Input transition rise or fall rate | V <sub>CC</sub> = 2.3 V to 2.7 V | 0                     | 200             | 0                     | 200             | ns/V |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | 0                     | 100             | 0                     | 100             |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | 0                     | 20              | 0                     | 20              |      |
| T <sub>A</sub>  | Operating free-air temperature     |                                  | −55                   | 125             | −40                   | 85              | °C   |

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS   | V <sub>CC</sub> | SN54LV74A            |     |     | SN74LV74A            |     |     | UNIT |
|------------------|---|-----------------|----------------------|-----|-----|----------------------|-----|-----|------|
|                  |   |                 | MIN                  | TYP | MAX | MIN                  | TYP | MAX |      |
| V <sub>OH</sub>  | I <sub>OH</sub> = −50 μA                                    | 2 V to 5.5 V    | V <sub>CC</sub> −0.1 |     |     | V <sub>CC</sub> −0.1 |     |     | V    |
|                  | I <sub>OH</sub> = −2 mA                                     | 2.3 V           | 2                    |     |     | 2                    |     |     |      |
|                  | I <sub>OH</sub> = −6 mA                                     | 3 V             | 2.48                 |     |     | 2.48                 |     |     |      |
|                  | I <sub>OH</sub> = −12 mA                                    | 4.5 V           | 3.8                  |     |     | 3.8                  |     |     |      |
| V <sub>OL</sub>  | I <sub>OL</sub> = 50 μA                                     | 2 V to 5.5 V    | 0.1                  |     |     | 0.1                  |     |     | V    |
|                  | I <sub>OL</sub> = 2 mA                                      | 2.3 V           | 0.4                  |     |     | 0.4                  |     |     |      |
|                  | I <sub>OL</sub> = 6 mA                                      | 3 V             | 0.44                 |     |     | 0.44                 |     |     |      |
|                  | I <sub>OL</sub> = 12 mA                                     | 4.5 V           | 0.55                 |     |     | 0.55                 |     |     |      |
| I <sub>I</sub>   | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 0 V to 5.5 V    | ±1                   |     |     | ±1                   |     |     | μA   |
| I <sub>CC</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5 V           | 20                   |     |     | 20                   |     |     | μA   |
| I <sub>off</sub> | V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V               | 0 V             | 5                    |     |     | 5                    |     |     | μA   |
| C <sub>i</sub>   | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 3.3 V           | 2                    |     |     | 2                    |     |     | pF   |
|                  |   | 5 V             | 2                    |     |     | 2                    |     |     |      |

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54LV74A, SN74LV74A

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

SCLS381E – AUGUST 1997 – REVISED MAY 2000

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)**

| PARAMETER |                                      |   | $T_A = 25^\circ\text{C}$ |     | SN54LV74A |     | SN74LV74A |     | UNIT |
|-----------|--------------------------------------|---|--------------------------|-----|-----------|-----|-----------|-----|------|
|           |                                      |   | MIN                      | MAX | MIN       | MAX | MIN       | MAX |      |
| $t_W$     | Pulse duration                       | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low      | 8                        |     | 9         |     | 9         |     | ns   |
|           |                                      | CLK   | 8                        |     | 9         |     | 9         |     |      |
| $t_{su}$  | Setup time before CLK $\uparrow$     | Data  | 8                        |     | 9         |     | 9         |     | ns   |
|           |                                      | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive | 7                        |     | 7         |     | 7         |     |      |
| $t_h$     | Hold time, data after CLK $\uparrow$ |   | 0.5                      |     | 0.5       |     | 0.5       |     | ns   |

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)**

| PARAMETER |                                      |   | $T_A = 25^\circ\text{C}$ |     | SN54LV74A |     | SN74LV74A |     | UNIT |
|-----------|--------------------------------------|---|--------------------------|-----|-----------|-----|-----------|-----|------|
|           |                                      |   | MIN                      | MAX | MIN       | MAX | MIN       | MAX |      |
| $t_W$     | Pulse duration                       | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low      | 6                        |     | 7         |     | 7         |     | ns   |
|           |                                      | CLK   | 6                        |     | 7         |     | 7         |     |      |
| $t_{su}$  | Setup time before CLK $\uparrow$     | Data  | 6                        |     | 7         |     | 7         |     | ns   |
|           |                                      | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive | 5                        |     | 5         |     | 5         |     |      |
| $t_h$     | Hold time, data after CLK $\uparrow$ |   | 0.5                      |     | 0.5       |     | 0.5       |     | ns   |

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

| PARAMETER |                                      |   | $T_A = 25^\circ\text{C}$ |     | SN54LV74A |     | SN74LV74A |     | UNIT |
|-----------|--------------------------------------|---|--------------------------|-----|-----------|-----|-----------|-----|------|
|           |                                      |   | MIN                      | MAX | MIN       | MAX | MIN       | MAX |      |
| $t_W$     | Pulse duration                       | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low      | 5                        |     | 5         |     | 5         |     | ns   |
|           |                                      | CLK   | 5                        |     | 5         |     | 5         |     |      |
| $t_{su}$  | Setup time before CLK $\uparrow$     | Data  | 5                        |     | 5         |     | 5         |     | ns   |
|           |                                      | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive | 3                        |     | 3         |     | 3         |     |      |
| $t_h$     | Hold time, data after CLK $\uparrow$ |   | 0.5                      |     | 0.5       |     | 0.5       |     | ns   |

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT)                                       | TO (OUTPUT)         | LOAD CAPACITANCE     | $T_A = 25^\circ\text{C}$ |       |     | SN54LV74A |     | SN74LV74A |     | UNIT |
|-----------|--|---------------------|----------------------|--------------------------|-------|-----|-----------|-----|-----------|-----|------|
|           |  |                     |                      | MIN                      | TYP   | MAX | MIN       | MAX | MIN       | MAX |      |
| $f_{max}$ |  |                     | $C_L = 15\text{ pF}$ | 50*                      | 100*  |     | 40*       |     | 40        |     | MHz  |
|           |  |                     | $C_L = 50\text{ pF}$ | 30                       | 70    |     | 25        |     | 25        |     |      |
| $t_{pd}$  | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or $\overline{Q}$ | $C_L = 15\text{ pF}$ | 9.8*                     | 14.8* |     | 1*        | 17* | 1         | 17  | ns   |
|           | CLK  |                     |                      | 11.1*                    | 16.4* |     | 1*        | 19* | 1         | 19  |      |
| $t_{pd}$  | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or $\overline{Q}$ | $C_L = 50\text{ pF}$ | 13                       | 17.4  |     | 1         | 20  | 1         | 20  | ns   |
|           | CLK  |                     |                      | 14.2                     | 20    |     | 1         | 23  | 1         | 23  |      |

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54LV74A, SN74LV74A

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

SCLS381E – AUGUST 1997 – REVISED MAY 2000

**switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE    | T <sub>A</sub> = 25°C |       |     | SN54LV74A |       | SN74LV74A |      | UNIT |
|------------------|-----------------|----------------|------------------------|-----------------------|-------|-----|-----------|-------|-----------|------|------|
|                  |                 |                |                        | MIN                   | TYP   | MAX | MIN       | MAX   | MIN       | MAX  |      |
| f <sub>max</sub> |                 |                | C <sub>L</sub> = 15 pF | 80*                   | 140*  |     | 70*       |       | 70        |      | MHz  |
|                  |                 |                | C <sub>L</sub> = 50 pF | 50                    | 90    |     | 45        |       | 45        |      |      |
| t <sub>pd</sub>  | PRE or CLR      | Q or Q̄        | C <sub>L</sub> = 15 pF | 6.9*                  | 12.3* |     | 1*        | 14.5* | 1         | 14.5 | ns   |
|                  | CLK             |                |                        | 7.9*                  | 11.9* |     | 1*        | 14*   | 1         | 14   |      |
| t <sub>pd</sub>  | PRE or CLR      | Q or Q̄        | C <sub>L</sub> = 50 pF | 9.2                   | 15.8  |     | 1         | 18    | 1         | 18   | ns   |
|                  | CLK             |                |                        | 10.2                  | 15.4  |     | 1         | 17.5  | 1         | 17.5 |      |

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE    | T <sub>A</sub> = 25°C |      |     | SN54LV74A |      | SN74LV74A |      | UNIT |
|------------------|-----------------|----------------|------------------------|-----------------------|------|-----|-----------|------|-----------|------|------|
|                  |                 |                |                        | MIN                   | TYP  | MAX | MIN       | MAX  | MIN       | MAX  |      |
| f <sub>max</sub> |                 |                | C <sub>L</sub> = 15 pF | 130*                  | 180* |     | 110*      |      | 110       |      | MHz  |
|                  |                 |                | C <sub>L</sub> = 50 pF | 90                    | 140  |     | 75        |      | 75        |      |      |
| t <sub>pd</sub>  | PRE or CLR      | Q or Q̄        | C <sub>L</sub> = 15 pF | 5*                    | 7.7* |     | 1*        | 9*   | 1         | 9    | ns   |
|                  | CLK             |                |                        | 5.6*                  | 7.3* |     | 1*        | 8.5* | 1         | 8.5  |      |
| t <sub>pd</sub>  | PRE or CLR      | Q or Q̄        | C <sub>L</sub> = 50 pF | 6.6                   | 9.7  |     | 1         | 11   | 1         | 11   | ns   |
|                  | CLK             |                |                        | 7.2                   | 9.3  |     | 1         | 10.5 | 1         | 10.5 |      |

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**noise characteristics, V<sub>CC</sub> = 3.3 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C (see Note 5)**

| PARAMETER          |   | SN74LV74A |      |      | UNIT |
|--------------------|---|-----------|------|------|------|
|                    |   | MIN       | TYP  | MAX  |      |
| V <sub>OL(P)</sub> | Quiet output, maximum dynamic V <sub>OL</sub> |           | 0.1  | 0.8  | V    |
| V <sub>OL(V)</sub> | Quiet output, minimum dynamic V <sub>OL</sub> |           | 0    | −0.8 | V    |
| V <sub>OH(V)</sub> | Quiet output, minimum dynamic V <sub>OH</sub> |           | 3.2  |      | V    |
| V <sub>IH(D)</sub> | High-level dynamic input voltage              | 2.31      |      |      | V    |
| V <sub>IL(D)</sub> | Low-level dynamic input voltage               |           | 0.99 |      | V    |

NOTE 5: Characteristics are for surface-mount packages only.

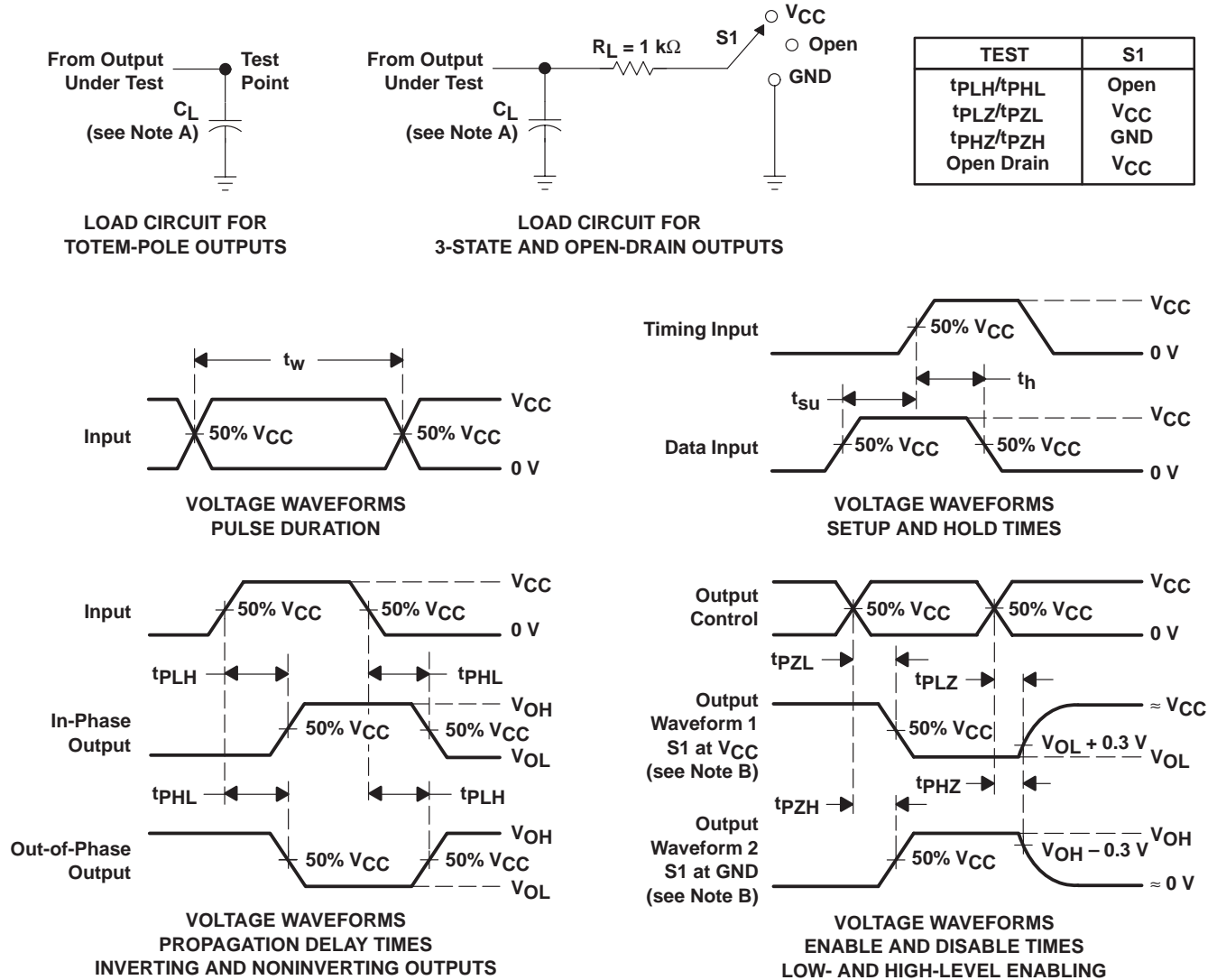
**operating characteristics, T<sub>A</sub> = 25°C**

| PARAMETER       |                               | TEST CONDITIONS                    | V <sub>CC</sub> | TYP | UNIT |
|-----------------|-------------------------------|------------------------------------|-----------------|-----|------|
| C <sub>pd</sub> | Power dissipation capacitance | C <sub>L</sub> = 50 pF, f = 10 MHz | 3.3 V           | 21  | pF   |
|                 |                               |                                    | 5 V             | 23  |      |

# SN54LV74A, SN74LV74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

SCLS381E – AUGUST 1997 – REVISED MAY 2000

## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{pLZ}$  and  $t_{pHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{pZL}$  and  $t_{pZH}$  are the same as  $t_{en}$ .
  - G.  $t_{pHL}$  and  $t_{pLH}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.