Low EMI Clock Generator for Pentium® II Systems

Preliminary

PRODUCT FEATURES

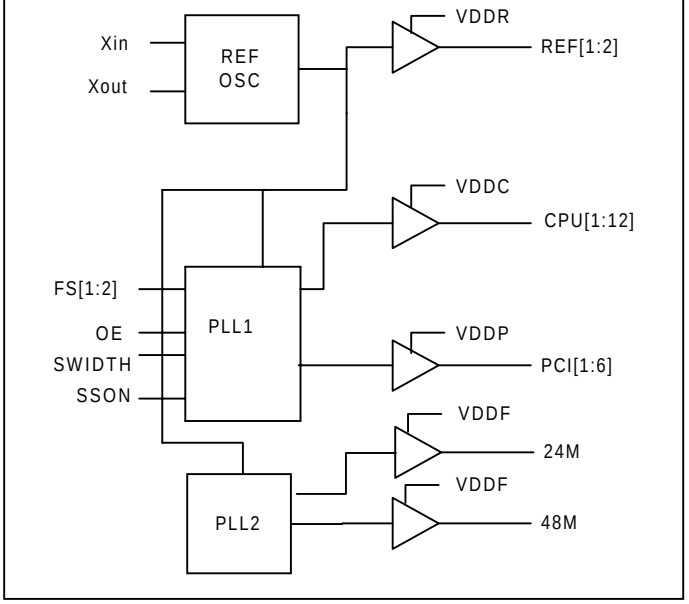
- Supports Pentium®. Pentium® II & Pro CPUs.
- Designed to meet Intel chipset specification
- 12 CPU and 6 PCI clocks
- One 48 MHz fixed clocks for USB.
- One 24 MHz fixed clocks Super IO.
- Separate power supply pins for mixed CPU, Fixed and PCI clock voltages
- < 250 ps Max. skew among CPU clocks.
- < 250 ps Max. skew among PCI clocks.
- Controlled current output buffers
- 48-pin SSOP package
- Spread Spectrum EMI reduction mode
- Selectable Spread Widths

FREQUENCY TABLE

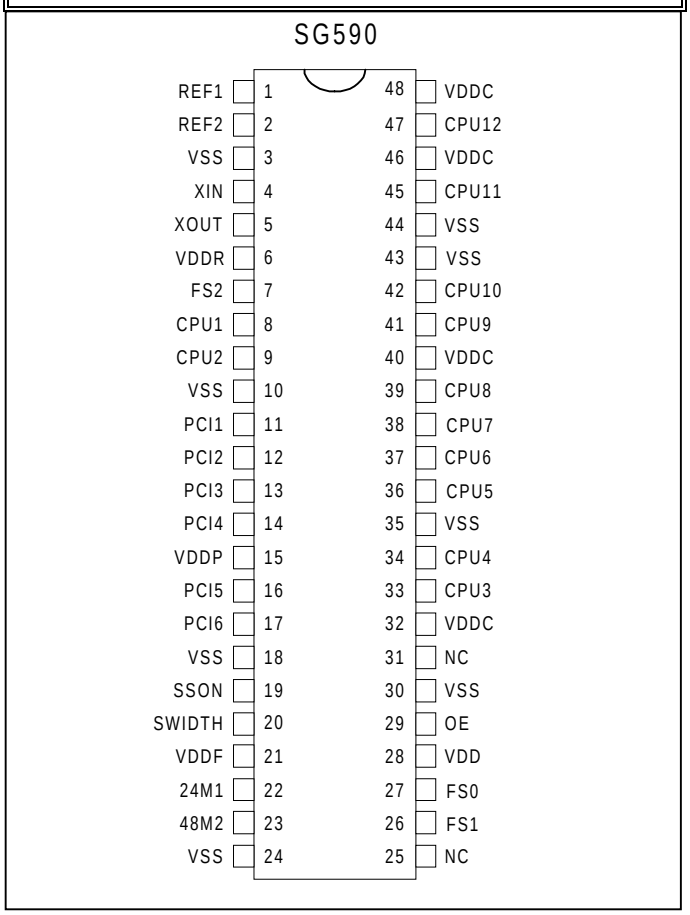
FS2	FS1	FS0	CPU	PCI
0	0	0	75	37.5
0	0	1	100	33.3
0	1	0	Tri-State	Tri-State
0	1	1	XIN/2	XIN/4
1	0	0	50	25
1	0	1	60	30
1	1	0	66.6*	33.3*
1	1	1	55	27.5

* may be selected to - .625% or -1.0% down spread

BLOCK DIAGRAM



CONNECTION DIAGRAM



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PIN DESCRIPTION

PIN No.	Pin Name	PWR	I/O	TYPE	Description
4	**Xin**	VDD	I	OSC1	On-chip reference oscillator input pin. Requires either an external parallel resonant crystal (nominally 14.318 MHz) or externally generated reference signal
5	**Xout**	VDD	O	OSC1	O-chip reference oscillator output pin. Drives an external parallel resonant crystal when an externally generated reference signal is used, is left unconnected
27, 26, 7	**FS(0:2)**	-	I	PAD PU	Frequency select input pins. See frequency select table on page 1. These pin has an internal pull-up
8, 9, 33, 34, 36, 37, 38, 39, 41, 42, 45, 47	**CPU(1:12)**	VDDC	O	BUF1	Clock outputs. CPU frequency table specified on page 1.
11, 12, 13, 14, 16, 17	**PCI(1:7)**	VDDP	O	BUF4	PCI bus clocks. See frequency select table on page 1.
3, 10, 18, 24, 30, 35, 43, 44	**VSS**	-	PWR	-	Ground pins for the device.
15	**VDDP**	-	P	-	3.3 Volt power supply pins for PCI and PCI_F clock output buffers.
21	**VDDF**	-	PWR	-	3.3 Volt power supply pins for 24 Mhz and 48 MHz clock output buffers.
32, 40, 46, 48	**VDDC**	-	PWR	-	3.3 or 2.5 Volt power supply pins for CPU clock output buffers.
28	**VDD**	-	PWR	-	Power supply pins for analog circuits and core logic
1, 2	**REF(1:2)**	VDDR	O	BUF3	Buffered outputs of on-chip reference oscillator.
22	**24M**	VDDF	O	BUF3	Fixed 24 MHz frequency clock outputs.
23	**48M**	VDDF	O	BUF3	Fixed 48 MHz frequency clock outputs.
29	**OE**	-	I	PAD PU	When driven to a logic low level, this pin will tristate all output clocks
20	**SWIDTH**	VDD	I	PAD PU	Selects 0.625 % or 1.0 % Spread spectrum modulation width. 1.0% = Logic High
19	**SSON**	-	I	PAD PU	When driven to a logic low level this pin enables EMI reducing Spread Spectrum mode (affects only CPU and PCI clocks) for CPU Frequency of 66.6 Mhz only.
6	**VDDR**	-	PWR	-	Power supply for reference clock (Ref) buffers

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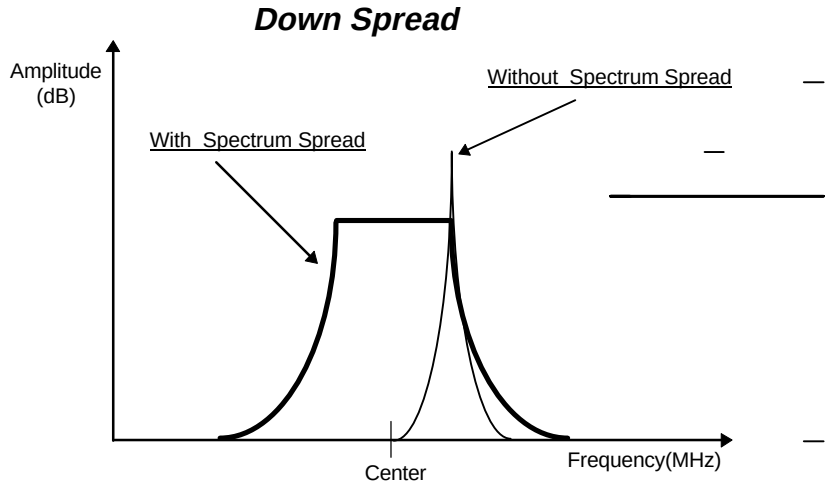
SPECTRUM SPREAD CLOCKING



CPU CLOCK SPECTRUM SPREADING SELECTION TABLE						
Unspread (MHz)	SWIDTH	Min (MHz)	Center (MHz)	Max (MHz)	% OF FREQUENCY SPREADING	MODE
66.6	0	66.18	66.39	66.6	0.625 % (- 0.625% + 0%)	Down Spread
66.6	1	65.9	66.27	66.6	1.0 % (- 1.% + 0%)	Down Spread

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MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	0ºC to + 125ºC
Operating Temperature:	0ºC to +70ºC
Maximum Power Supply:	5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input Low Current	IIL	-66		-	µA	
Input High Current	IIH			5	µA	
Output Low Voltage IOL = 4mA	VOL	-	-	0.4	Vdc	All Outputs (see buffer spec)
Output High Voltage IOH = 4mA	VOH	2.4	-	-	Vdc	All Outputs Using 3.3V Power (see buffer spec)
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd	-	-	TBD	mA	CPU = 66.6 MHz, PCI = 33.3 MHz
Static Supply Current	Isdd	-	-	TBD	µA	-
Crystal Oscillator Capacitance	Cx	-	18	-	pF	Xin and Xout crystal load capacitance values (each)
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 seconds

VDD = VDDP=VDDF =3.3V ±5%, VDDC =2.5V ±5%,, TA = 0ºC to +70ºC

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SWITCHING CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V
CPU to PCI Offset	tOFF	1.5	-	4	ns	CPU load = 20 pF, PCI load = 3 pF measured at 1.5V PCI and 1.25V CPU
Buffer out Skew All CPU Buffer Outputs	$tSKEW_1$	-	-	175	ps	20 pf Load Measured at 1.5V
Buffer out Skew All PCI Buffer Outputs	$tSKEW_2$	-	-	250	ps	30 pf Load Measured at 1.5V
ΔPeriod Adjacent Cycles	ΔP	-	-	±250	ps	-
Jitter Spectrum 20 dB Bandwidth from Center	BW_J			500	KHz	
VDD = VDDP=VDDF =3.3V ±5%, VDDC = 2.5V ±5%, TA = 0ºC to +70ºC						

BUFFER 1 CHARACTERISTICS FOR CPUCLK(1:12)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	-27	-	-	mA	Vout = 1.0 V
Pull-Up Current Max	IOH_{max}	-	-	-27	mA	Vout = 2.38 V
Pull-Down Current Min	IOL_{min}	27	-	-	mA	Vout = 1.2 V
Pull-Down Current Max	IOL_{max}	-	-	27	mA	Vout = 0.3 V
Rise/Fall Time Min Between 0.4 V and 2.0 V	TRF_{min}	0.4	-	1.6	ns	20 pF Load
VDD = VDDP=VDDF=3.3V ±5%, VDDC =2.5V ±5%,, TA = 0ºC to +70ºC						

BUFFER 3 CHARACTERISTICS FOR REF(1:2), 24M and 48 M						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	-29	-	-	mA	Vout = 1.0 V
Pull-Up Current Max	IOH_{max}	-	-	-23	mA	Vout = 3.135 V
Pull-Down Current Min	IOL_{min}	29	-	-	mA	Vout = 1.95 V
Pull-Down Current Max	IOL_{max}	-	-	27	mA	Vout = 0.4 V
Rise/Fall Time Between 0.4 V and 2.4 V	TRF_{min}	0.5	-	2.0	ns	20 pF Load
VDD = VDDP=VDDF =3.3V ±5%, VDDC =2.5V ±5%,, TA = 0ºC to +70ºC						

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BUFFER 4 CHARACTERISTICS FOR PCICLK(1:6)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	-33	-	-	mA	Vout = 1.0 V
Pull-Up Current Max	IOH_{max}	-	-	-33	mA	Vout = 3.135 V
Pull-Down Current Min	IOL_{min}	30	-	-	mA	Vout = 1.95 V
Pull-Down Current Max	IOL_{max}	-	-	38	mA	Vout = 0.4 V
Rise/Fall Time Between 0.4 V and 2.4 V	TRF_{max}	0.5	-	2.0	ns	30 pF Load
VDD = VDDP=VDDF =3.3V ±5%, VDDC=2.5V ±5%,, TA = 0ºC to +70ºC						

CRYSTAL AND REFERENCE OSCILLATOR PARAMETERS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerence	TC	-	-	+/-100	PPM	Calibration note 1
	TS	-	-	+/- 100	PPM	Stability (Ta -10 to +60C) note 1
	TA	-	-	5	PPM	Aging (first year @ 25C) note 1
Mode	OM	-	-	-		Parallell Resonant
Pin Capacitance	CP		5		pF	Capacitance of XIN and Xout pins
DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Startup time	Ts	-	-	30	µS	
Load Capacitance	CL	-	20	-	pF	note 1
Effective Series resonant resistance	R1	-	-	40	Ohms	
Power Dissipation	DL	-	-	0.10	mW	note 1
Shunt Capacitance	CO	-	--	7	pF	
X1 and X2 Load	CL		17		pF	internal crystal loading gapacitors on each pin (to ground)

For maximum accuracy,the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors.

Budgeting Calculations

Typical trace capacitance, (< half inch) is 4 pF, Load to the crystal is therefore 2.0 pF

Clock generator internal pin capacitance of 36 pF, Load to the crystal is therefore 18.0 pF

the total parasitic capacitance would therefore be = 20.0 pF.(matching CL)

Note 1: It is recommended but not manditory that a crystal meets these specifications.

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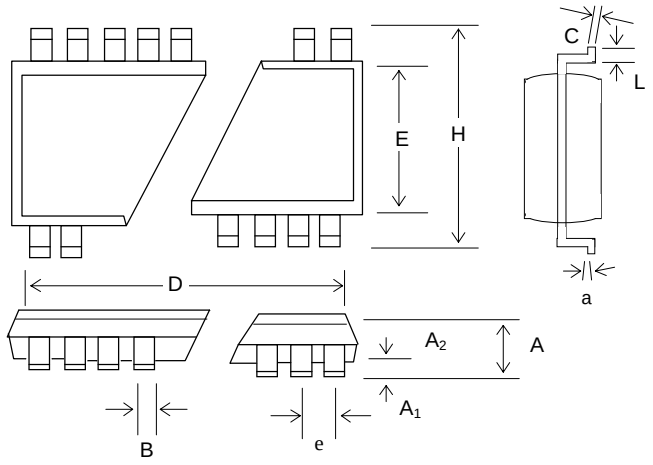
PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.20	0.31	0.41
A2	0.088	0.090	0.092	2.24	2.29	2.34
B	0.008	0.010	0.0135	0.203	0.254	0.343
C	0.005	-	0.010	0.127	-	0.254
D	0.620	0.625	0.630	15.75	15.88	16.00
E	0.292	0.296	0.299	7.42	7.52	7.59
e	0.025 BSC			0.635 BSC		
H	0.400	0.406	0.410	10.16	10.31	10.41
a	0.10	0.013	0.016	0.25	0.33	0.41
L	0.024	0.032	0.040	0.61	0.81	1.02
a	0º	5º	8º	0º	5º	8º
X	0.085	0.093	0.100	2.16	2.36	2.54

ORDERING INFORMATION

Part Number	Package Type	Production Flow
SG590AYB	48 PIN SSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SG590AYB
Date Code, Lot #

SG590AYB

- Flow: B = Commercial, 0ºC to + 70ºC
- Package: Y = SSOP
- Revision
- IMI Device Number