PowerFLEX ™

Surface-Mount Power Packaging

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TEXAS INSTRUMENTS

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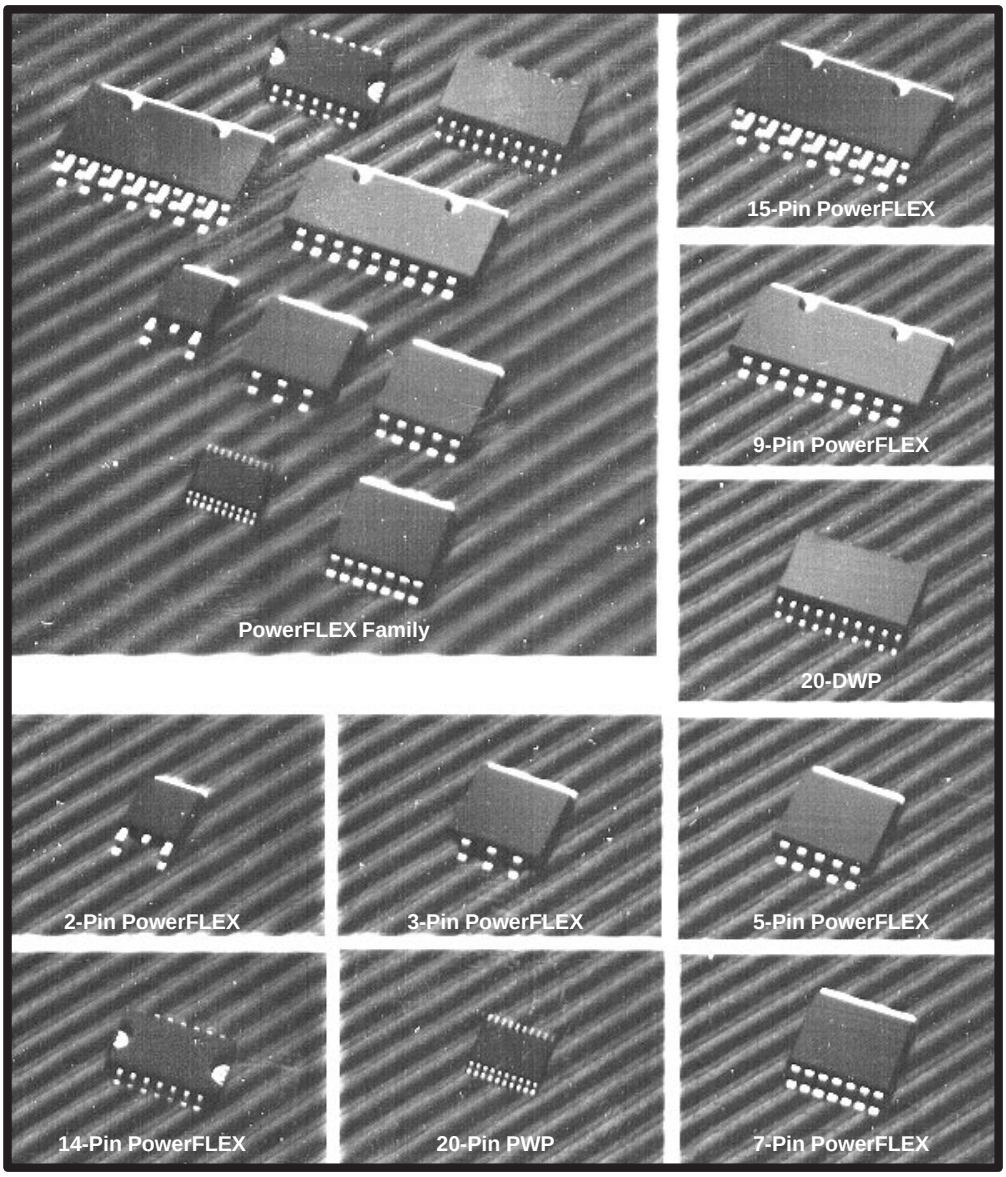
INTRODUCTION



PowerFLEX™ is a package family that has been designed to offer customers a surface-mountable power package. The package is designed to be low in cost and compatible with much of the existing assembly equipment in use at the assembly factories. The PowerFLEX package has a low profile while retaining most of the power dissipation characteristics. PowerFLEX is available in 3-, 5-, 7-, 9-, 14-, and 15-pin versions. Each version has its own technical capabilities. The PowerFLEX package is offered in both surface-mount and thru-hole lead configurations to give customers the same low cost in a smaller area.

Power semiconductor devices have historically been assembled in packages with large form factors, such as the TO-220. The demands of cost-effectiveness and compactness in several industries have compelled designers to ask for thin surface-mount packages for power devices. To address this trend, Texas Instruments (TI™) has recently developed a new type of package – the PowerFLEX family that is cost-effective, thermally enhanced, thin and surface-mountable on a standard Surface Mount Technology (SMT) assembly line.

The PowerFLEX family is comparable to the TO-220, DPAK, and power Single-In-Line Package (SIP). It consists of 2-, 3-, 5-, 7-, 9-, 14- and 15-pin packages, and can accommodate die sizes as large as 45.6K mils^2. Thin, surface-mountable, and thermally enhanced designs are three distinguishing features boasted by the PowerFLEX family. The body thickness of the PowerFLEX family is less than 2 mm. The maximum package length and width (excluding lead length) of the largest package in the family (15-pin) are only 2 cm and 1 cm, respectively. Moisture ingress protection, mechanical rigidity, and the locking of mold compound to the lead frame are achieved through special leadframe design. The tab(s), which are an extension of the die pad for all packages, can be used as the visual inspection site(s) of surface-mount quality. The exposed die pads, similar to that of a TO-220, enable the majority of the heat to dissipate directly into the underlying printed circuit board or heat sink. Silver-flake-filled epoxy is used as the die-mount material for the PowerFLEX family for cost and stress considerations. Thermal performance can be enhanced by utilizing effective printed circuit board (PCB) design, as the PCB dominates the thermal performance of the system.

The low-cost, low-profile, and enhanced thermal design advantages of the PowerFLEX family make it the package of choice for applications that are space and cost critical, while also requiring excellent power-dissipation capability. These applications include hard disk drives, printers, office automation equipment, automotive engine and body controllers, and wireless communication units.

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BOARD-MOUNTED TEMPERATURE-CYCLE DATA

Temperature-cycle testing of the printed wiring board (PWB) assembly was used to evaluate the capability of the assembly to withstand mechanical stress resulting from the differences in thermal expansion coefficients between the die, package, and PWB materials. The testing was also used to age the soldered thermal connection between the thermal pad and copper trace on the FR4. The degradation of the strength of that connection was evaluated by performing a Unit Pull Strength Test. The assemblies were cycled between temperature extremes of –55°C and 125°C for a duration of 1000 cycles.

Table 1. Temperature-Cycle Test Results

TOTAL UNIT CYCLES	FAILURES	AVERAGE CHANGE IN UNIT PULL STRENGTH
50 000	0	–1.5%

TEMPERATURE vs. TIME WAFER FAILURES

Major failure mechanisms in device-level reliability include gate oxide and interlevel (and intralevel) oxide (ILO) integrity, electromigration in metal lines, vias and contacts, channel hot carriers, junction leakage, and mobile ions.

Dielectric breakdown is a major failure mechanism of very large scale integration (VLSI) circuits and has become a serious reliability issue due to device scaling. The breakdown field of the oxide layer can be significantly lowered by contamination and defects existing in the oxide. Time-dependent dielectric breakdown (TDDB) is one of the methods used to measure oxide integrity. In the TDDB test, devices are stressed by a dc voltage until hard breakdown is observed, and the time-to-failure (TF) is recorded for each device. Since oxide breakdown can be accelerated by increasing the electric field (voltage) across the oxide, the TDDB tests are generally implemented at different electric fields. The stress fields are normally chosen to be in the region of the Fowler-Nordheim tunneling such

that a linear approximation can be used to predict the oxide lifetime under operating conditions. The acceleration exponent (y) is related to TF by equation 1:

$$TF = t_0 \exp(-yV/t_{ox}) \quad (1)$$

where t_0 is a constant, t_{ox} is the thickness of the oxide, and V is the applied voltage.

The channel hot carrier effect becomes significant when the feature size of transistors is shrinking into the deep submicron region. The higher electric field resulting from the shorter channel length accelerates the electrons (holes) to very high energy states. Some of these hot electrons (holes) are lucky enough to escape from the channel region into either silicon oxide or the substrate. Hot carriers can generate phonon emission and break bonds at the oxide/silicon interface and in the oxide itself. Those injected into the oxide can also create traps and oxide charges. The channel hot carrier effect has a negative activation energy since the electron (hole) mobility is higher at lower temperature.

Electromigration is a phenomenon that occurs under the influence of temperature gradient or excessive current density. The mechanism is atomic diffusion driven by a momentum exchange with the conduction electrons. A local divergence of atom flux can result in excessive vacancy formation. These vacancies grow into voids, and voids grow continuously until the conductor fails. Electromigration can occur on metal lines, vias, and contacts on an integrated circuit.

Mobile ions which are alkali ions result from impurities in chemicals or contamination in various device-manufacturing processes. These alkali ions have high mobility to drift in the oxide at relatively low applied voltages and could make MOSFET (metal-oxide semiconductor field-effect transistor) threshold voltage unstable for positive gate bias.

The pn junctions are basic building blocks of modern integrated circuits. The properties of junctions that are generally examined are the forward currents and reverse leakage currents, the reverse breakdown voltage, and the series resistance. Of these, reverse leakage currents are often used to monitor the quality of the pn junction.

The kinetics of each failure mechanism can be described by the Arrhenius equation that bears the general form in equation 2:

$$k = A \exp -(E/k_b T) \quad (2)$$

where k is the rate constant, A is a pre-exponential factor, E is the activation energy at which a specific failure mechanism becomes active (eV), k_b is the Boltzmann constant (8.61×10^{-5} eV/K), and T is absolute temperature (K).

The acceleration factor (AF) is defined as the quotient of the failure rate at one stress condition (temperature, current, voltage, moisture, mechanical stress, etc.) over the failure rate at another stress condition. It is used to convert the failure rate obtained from one stress condition to the failure rate at another stress condition (see equation 3).

$$AF = k_1 / k_2 = \exp(E/k_b(1/T_2 - 1/T_1)) \quad (3)$$

A method employed to measure the failure rates of these failure mechanisms is varying one stress condition (temperature or voltage) while holding the remaining stresses constant.

Table 2 lists the parameters related to each of the major failure mechanisms.

In equation 4, n is the acceleration exponent:

$$I = I_0[\exp(-qV/nk_b T) - 1] \quad (4)$$

where I, q, V, k_b, and T are current, charge, applied voltage, Boltzmann constant, and absolute temperature, respectively.

Table 2. Reliability Failure-Mechanism Acceleration Factors

FAILURE MECHANISM	TEMPERATURE		VOLTAGE	
	Ea†	AF‡ (25°C to 100°C)	FIT PARM§	AF‡ (2.5 V to 8.5V)
Gate Oxide	0.3 eV	13	y = 6.5 cm/MV	50,700
ILO¶	0.4 eV	30	y = 6.5 cm/MV	50,700
Electromigration				
Metal Line	0.7 eV	382	n = 2	2
Vias	0.7 eV	382	n = 2	2
Contacts	1.0 eV	4890	n = 2	2
Channel Hot Carriers	–0.2 eV	0.18	n = 3	100
Mobile Ions	1.0 eV	4890	n = 1	1.4
Junctions	0.7 eV	382	y = 1.7 V^{-1}	30

† Activation Energy
‡ Acceleration Factor
§ Fitting Parameter
¶ Interlevel and intralevel oxide

TEMPERATURE vs. TIME BOND FAILURES

Major package level reliability includes various forms of package crackings, chip crackings induced by stress from packaging processes and materials (mount materials or molding compounds), delamination at interfaces, ball/stitch bond liftoff, shift and fracture, and gold/aluminum (Au/Al) ball bond failure due to excessive Kirkendall voids, which results in insufficient high temperature storage lifetime (HTSL).

HTSL is a metric to measure the effect of molding compounds on wire-bond reliability. The brominated resin flame retardants and synergistic brominated resin/antimony-oxide flame retardants were introducted into the epoxy molding compounds in the mid-1970s. It was found that the thermally-induced bromine release accelerates degradation of Au/Al wire-bond strength through the Kirkendall voiding mechanism in the gold-aluminum intermetallics. The degradation of intermetallic layers between the gold wire and aluminum bond pad starts at the interface of the gold-rich intermetallic and the gold ball. Technology evolvement in the past decade has been able to slow down the degradation by introducing a new antimony oxide system or using “ion getters” to “freeze” the free bromine ions in the molding compounds.

Texas Instruments uses the wire-pull test method to determine the HTSL of a molding compound. In this method, packages molded by the subject molding compound are put into ovens with the capability of controlling to +/–2°C at temperatures of 195°C, 185°C, 175°C, 150°C, and 125°C. Two units of packages are pulled at each read interval, which varies from 50 hours to 500 hours, depending on the temperature. The wire-pull test is performed on decapped units. Testing at that temperature is discontinued when the wire-pull strength is below a predetermined failure value. The acceleration factor (AF) and activation energy (E) for each rate-limiting process can be calculated by using the time-to-failure (TF) at two different temperatures through the relationships shown in equations 5 and 6.

$$AF = k_1/k_2 = TF_2/TF_1 \quad (5)$$

$$E = R \ln(AF)/(1/T_2 - 1/T_1) \quad (6)$$

This data is used to predict the HTSL at different temperatures. Figure 1 is an example of the HTSL experimental data of one of the commonly used molding compounds. From this data, HTSL at different temperatures can be calculated and the results are shown in the inset of Figure 1.

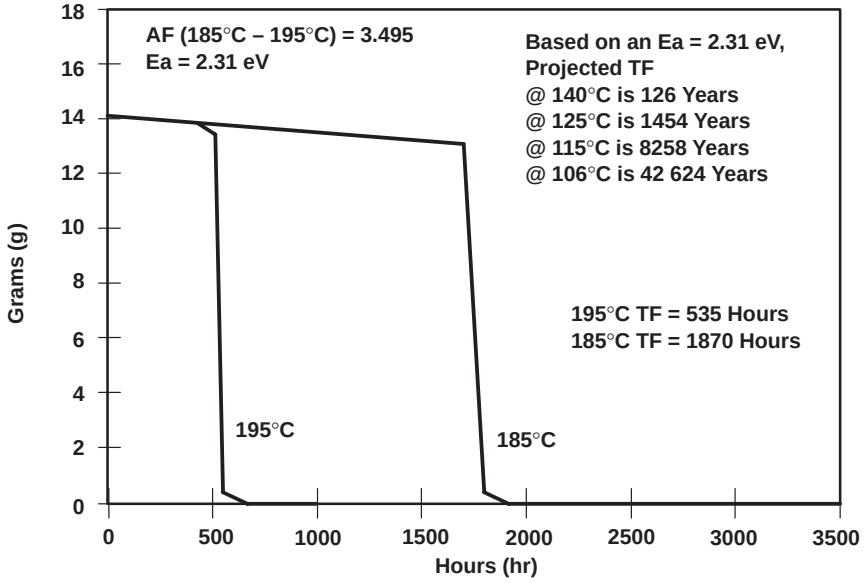


Figure 1. HTSL at Various Temperatures

RELIABILITY TEST CONDITIONS

Table 3. Reliability Test Conditions of the PowerFLEX Package Family

TEST TYPE	CONDITIONS	READ POINTS
Steady-State Life†	155°C	240 hrs
Biased Hast†	130°C 85% RH	96 hrs
Autoclave†	121°C 15 PSIG	240 hrs
Thermal Shock†	–65 / 150°C	1000 cycles
Solder Heat	260°C 10 sec	
Solvent Resistance		
Solderability	8 hrs	
Lead Fatigue		
Lead Pull		
Lead Finish Adhesion		
Physical Dimensions		
Flammability	UL94V-0	
	IEC 695-2-2	
Salt Atmosphere	24 hrs	
X-Ray	Top View Only	
Storage Life†	170°C	420 hrs

† Samples used for these stresses were preconditioned according to Joint Electronic Device Committee (JEDEC) A113, Level 1.

THERMAL DATA

Power dissipation from active elements on an integrated circuit device causes an increase in the junction temperature, which depends on the amount of power dissipation and on the thermal resistance between the junction and the case or ambient. The relation among these thermal properties, such as thermal resistance, power dissipation, and junction temperature, is analogous to Ohm's Law. In this analogy, temperature difference, power dissipation, and thermal resistance correspond to voltage drop, current, and electrical resistance, respectively. The assumption implied in this analogy is that the chip surface temperature and the case or ambient temperature are isothermal, although in reality, this is not usually the case. However, this analogy still holds true in most of the applications. The junction temperature, power dissipation, and thermal resistance can be related by equation 7 or 8:

$$R_{\theta Jx} = (T_j - T_x)/P \tag{7}$$

$$T_j = T_x + P \cdot R_{\theta Jx} \tag{8}$$

where $R_{\theta Jx}$ is the thermal resistance between the junction and the case or ambient (°C/W); T_j and T_x are the average temperatures of the junction and the case or ambient respectively (°C), and P is power dissipation (W).

Junction-to-case thermal resistance, $R_{\theta JC}$, and junction-to-ambient thermal resistance, $R_{\theta JA}$, are two commonly listed thermal resistances in the data books. $R_{\theta JC}$ can be very small when the measurement is directly under the die pad or can be very high when measured at places far away from the junction. Typically, it ranges from less than 1 °C/W to a few °C/W, depending on the measurement location, package type, active element size, die size, die-attach material type and quality, and leadframe material and thickness. The major heat flow in the PowerFLEX-type package follows the die-die mount-die pad path to the underlying PWB heatsink since this path offers the lowest thermal resistance. The thermal resistance of silver-filled polymer-based mount material is the major

contributor to junction-to-case thermal resistance in this type of package since this material has the poorest thermal conductivity compared to other materials in a package. Assembly process control is critical in minimizing the thermal resistance through the optimum control of thickness and voiding of the die attach layer.

Figure 2 is the thermal equivalent circuit of the steady state thermal behavior of a PowerFLEX type of package mounted on a heatsink, where $R_{\theta JC}$, $R_{\theta CA}$, $R_{\theta CH}$, and $R_{\theta HA}$ are the thermal resistances of junction-to-case, case-to-ambient, case-to-heatsink, and heatsink-to-ambient respectively. T_J, T_A, and T_H are the temperature of junction, ambient, and heatsink, respectively.

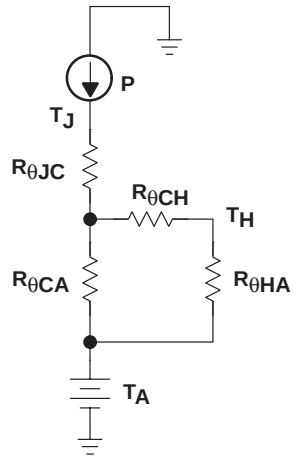


Figure 2. Thermal Equivalent Circuit of a Surface-Mounted Package Mounting on a Heatsink

The junction-to-ambient thermal resistance ($R_{\theta JA}$) can be expressed as

$$R_{\theta JA} = R_{\theta JC} + \frac{\left(R_{\theta CH} + R_{\theta HA}\right)}{\left(R_{\theta CA} + R_{\theta CH} + R_{\theta HA}\right)} \quad (9)$$

Case-to-ambient thermal resistance ($R_{\theta CA}$) is generally very large compared to other terms, hence, equation 8 can be simplified as

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CH} + R_{\theta HA} \quad (10)$$

$R_{\theta CH}$ is also called contact thermal resistance, whose value depends on the mounting pressure, thermal grease usage, and interface roughness. It is about 0.1 to 0.2°C/W when thermal grease is used and proper mounting pressure is applied.

The comparison of junction-to-ambient thermal resistance ($R_{\theta JA}$) between two packages is like comparing oranges to apples if both packages do not have the same heatsink configuration. The resistance of heat flow from the junction to ambient can be enhanced significantly when the heatsink, such as a printed circuit board, can be effectively designed to reduce heatsink-to-ambient thermal resistance ($R_{\theta HA}$).

The concept of thermal resistance is valid when the peak junction temperature is nearly equal to the average junction temperature, as in the case of high duty cycle and long pulses. When the applied pulses have a low duty cycle, the peak junction temperature can be significantly higher than the average junction temperature. Since the device lifetime-limiting factor is the peak junction temperature, the thermal impedance $Z_{\theta Jx}$, which is analogus to electrical impedance, should be used instead of the thermal resistance, $R_{\theta Jx}$.

$$Z_{\theta Jx} = \left(T_J max - T_x\right)/P \tag{11}$$

where $T_J$max is the maximum junction temperature.

For a singe-pulse condition, the junction-to-case thermal impedance for a PowerFLEX-type package directly mounted onto a heatsink can be approximated as the sum of a series of thermal impedances contributed from the individual materials as shown in equation 12:

$$Z_{\theta Jx}\left(t_P\right) = \sum_i R_{\theta i}\left(1 - e^{-\frac{t_P}{t_i}}\right) \tag{12}$$

where t_P is the single pulse duration; $R_{\theta i}$ is the steady-state thermal resistance; and t_i is the thermal time constant of the individual component.

Thermal time constant is another electrical analogy. It is defined as the time for the thermal impedance of a material to reach 63.2% of its steady-state thermal resistance. A conceptual example is shown in Figure 3, which is a curve of thermal impedance versus pulse duration. This curve is a summation of the thermal impedance of each material. One cannot observe the plateaus on the summation curve when the dominant contributor in that pulse duration period has a small time constant.

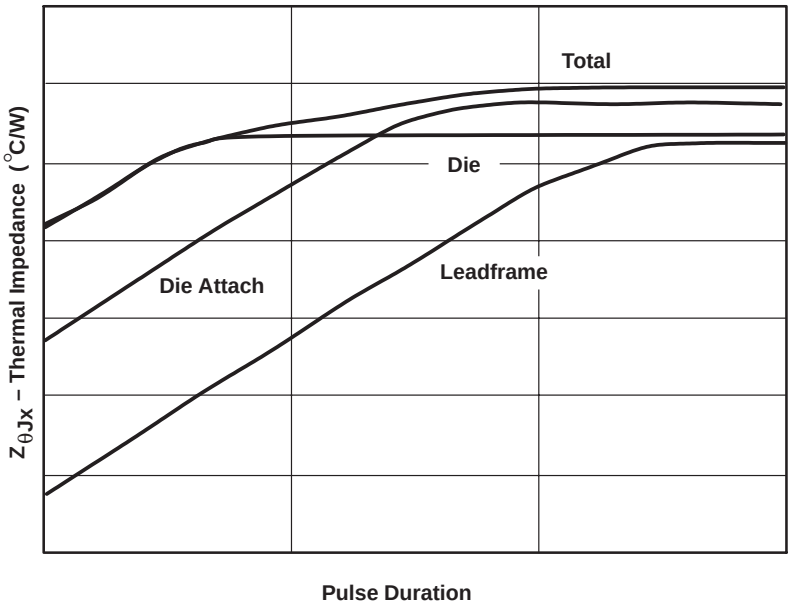


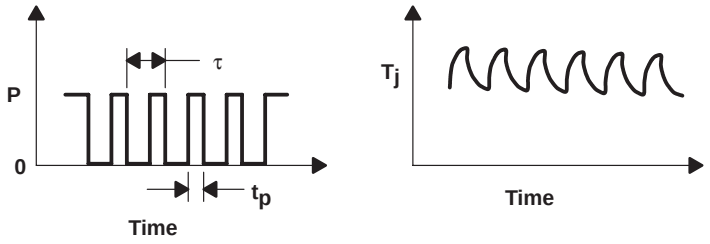
Figure 3. Conceptual Example of Total Thermal Impedance as a Sum of Individual Contributions

The thermal impedance, $Z_{\theta Jx,}$ of a long train of equal amplitude load pulses (Figure 4(a)) can be calculated from the thermal impedance, $Z_{\theta Jx}(t_p)$, of a single load pulse by equation 13:

$$Z_{\theta Jx} = \frac{\left(T_J - T_X\right)}{P} \qquad (13)$$

$$= d \times R_{\theta Jx} + t_p\left(1 - \frac{1}{d}\right) Z\left(\tau + t_p\right) - Z(\tau) + Z(t_p)$$

where τ is the period of load pulses, the duty cycle (d) is equal to t_p/τ.



(a) Power Dissipation **(b) Temperature Change**

Figure 4. Power Dissipation and Corresponding Temperature Change at Junction

Test Die Description

(a) Thermal Test Dies

Steady-state thermal measurements under forced airflow conditions were performed on packages assembled using TI's thermal test dies. Two different die sizes were used: one is 120 x 120 mil (1 mil = 0.001 inch), while the other is 62 x 62 mil, which is a 50% reduction in dimension from the first one. The use of two die sizes enables us to compare the thermal performance of packages with different active areas. Heat was generated by four banks of resistors on each test die; each bank has an electrical resistance of 12.5 Ω. A bipolar-type sensing diode that is located at the center of the die monitors the junction temperature. The power for junction-to-ambient thermal resistance measurements is 2 W using thermal test dies.

(b) Power DMOS (Double-Diffused Metal-Oxide Semiconductor) Devices

Four power DMOS devices were used in this study to reflect the thermal performance of actual power devices that can be assembled in PowerFLEX packages. These devices are power monolithic DMOS arrays that consist of different numbers of independent N-channel enhancement-mode DMOS transistors. Table 4 lists the parameters of each device. The calculations of power area has excluded the bond pad area on each transistor.

Table 4. Parameters of Power DMOS Devices

DEVICE	NO. OF TRANSISTORS	POWER AREA PER TRANSISTOR (K MIL^2)	TOTAL DIE AREA (K MIL^2)
1	3	6.50	31.3
2	6	1.93	21.3
3	2	2.15	7.2
4	2	7.87	25.0

Thermal Test Board Layout

Two types of thermal test boards were used in forced air measurements. Both types of boards have the same layout as shown in Figure 5. Each board was made of FR4 material with a total thickness of 0.062 inch and a dimension of 8.25 cm x 8.25 cm with two edge connectors on two opposite edges. The first type is a 2-layer board with minimal copper traces electrically connected from each package to one of the edge connectors. Two 1-oz copper layers on both sides of the test board with the same dimension as the exposed die pad were located on each package position. Thermal vias were used for thermal enhancement purposes and their numbers depend on the sizes of exposed die pads. The second type of board has the same configuration as the first one except that there are two additional 1-oz copper layers sandwiched by FR4 laminates to further enhance the thermal performance. PowerFLEX packages to be tested were solder-mounted on the board to simulate a real printed circuit board environment.

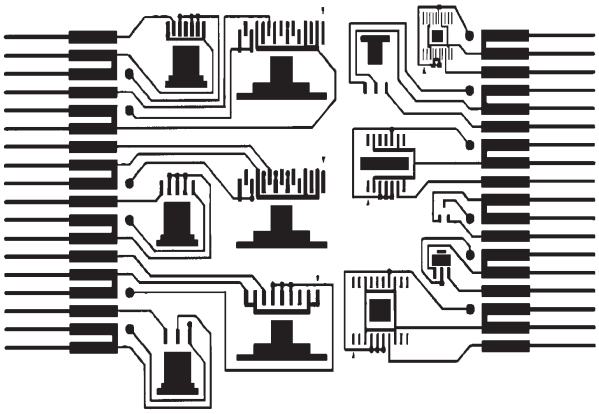


Figure 5. Thermal Test Board Layout

Calibration Curve of the Sensing Diode

Figure 6 is an example of the calibration curve of the sensing diode on the thermal test die. The V_{be} of the sensing diode at two different temperatures were first measured and the slope of the V_{be} versus the temperature curve was calculated. This slope is used to calculate the junction temperature at which another V_{be} is measured.

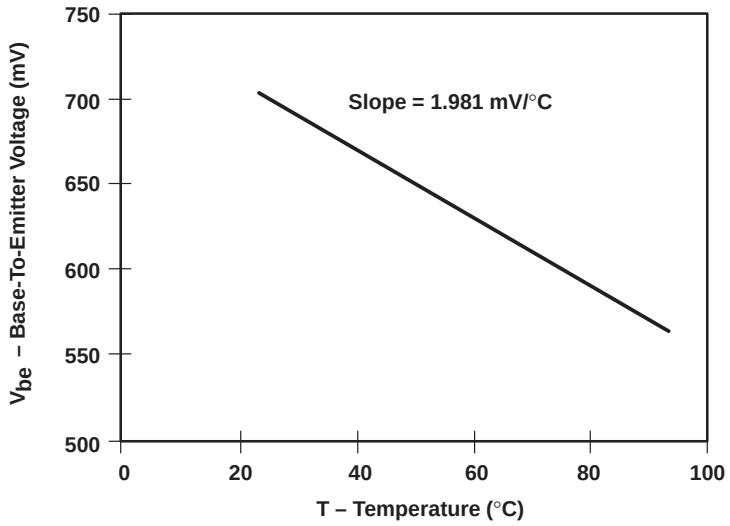


Figure 6. Calibration Curve of the Sensing Diode on the Thermal Test Die

(a) Cold Plate Method

The cold plate method used to measure junction-to-case thermal resistances can be referenced to the dynamic mode of the electrical test method as described in JEDEC JC15.1 *Integrated Circuit Thermal Measurement Method – Electrical Test Method (Single Semiconductor Device)*[1]. The cold plate method measures the average thermal resistance from the junction to the package surface that is in intimate contact with an infinite heatsink.

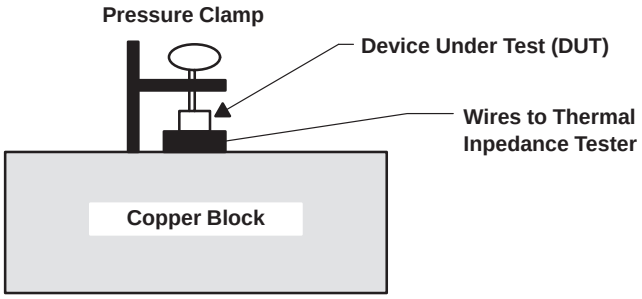


Figure 7. Experimental Setup of the Thermal Impedance Measurement

Figure 7 shows the experimental setup of the cold plate method. In this setup, the device under test (DUT) was pressure-clamped on top of a 8-inch x 8-inch x 4-inch copper block that acted as an infinite heatsink. Silicone thermal grease was applied between the heatsink and the package. A TESEC™ 9214-KT thermal impedance tester was used in these measurements. The tester first measured the drain-to-source voltage (V_{DS}) of the active device (DMOS arrays) and then switched to heat the DUT by forcing through a predetermined amount of power for a specific time period. The tester was then switched back to measure the V_{DS} of the active device again. The measurement current was set at 10 mA to ensure that it was small enough not to affect the device characteristics. To reflect the actual junction temperature, the delay time between the switch-off of the heating power and the post-heating measurement was set to be only 10 μs. The difference in the two measurements, ΔV_{DS}, was displayed by the tester and was used to calculate the device junction temperature at that test condition.

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Steady-State Thermal Measurements

(a) Still-Air Conditions

Still-air measurements were performed by placing the package-mounted test board in a 1-ft^3 air chamber. The board was oriented with the top facing upward. The ambient temperature was measured approximately 6 inches above the test board with a type J thermocoupler.

(b) Forced Airflow Conditions

Forced airflow measurements were made inside a calibrated wind tunnel. The overall wind tunnel dimensions were 6 inches x 6 inches x 74 inches with a test duct width of 6 inches. Measurements were performed at ambient temperature. The temperature and velocity measurement positions were at the center of the duct and about 6 inches ahead of the test board to avoid the wake effect and heating effect from the test board and package. The board and package orientation was vertical and located in the center region of the duct. The package was oriented with the lateral axis transversing airflow. Air velocity was monitored with a hot-wire anemometer probe. The air velocities used in these measurements were 100 ft/min, 200 ft/min, and 400 ft/min. Temperatures were monitored with a type J (iron/constantan) thermocoupler.

Junction-to-Case Thermal Resistance, $R_{\theta JC}$

Figure 8 shows the transient thermal response of device 1 in a 15-pin PowerFLEX package when mounted on an infinite heatsink. The thermal resistance decreases upon increasing the number of transistors turned on that effectively increases the heat dissipation area. This figure also shows that the thermal resistance of PowerFLEX packages can be under 2°C/W and is capable of being used for high-power dissipation applications.

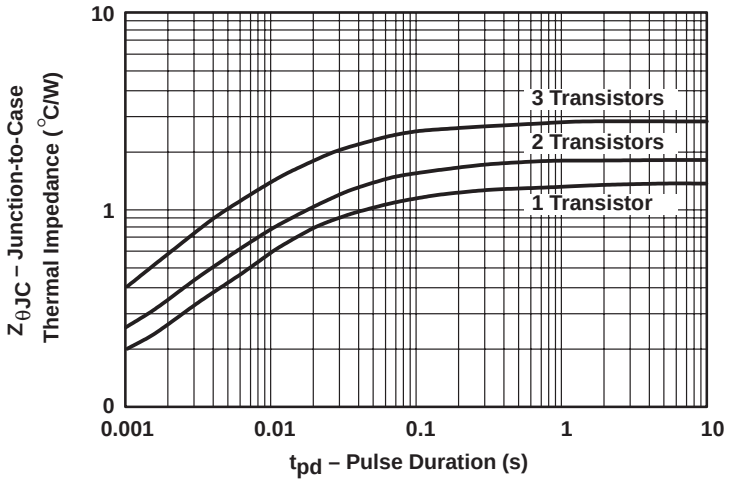


Figure 8. Transient Thermal Impedance of Device 1 in a 15-Pin PowerFLEX Package

Each curve corresponds to a different number of transistors turned on; power used is 5 W.

Figure 9 and 10 are the transient thermal responses of device 4 in a 7-pin and 15-pin PowerFLEX package, respectively. When the applications are in the short pulse and low-duty-cycle region, the maximum power dissipation can be calculated according to equation 10. For example, when device 4 in a 7-pin PowerFLEX package is used, the thermal impedance of a low-duty-cycle 1-ms pulse train is 0.6°C/W (see Figure 9). The maximum peak power dissipation can be up to 75 W when maximum junction temperature is 150°C and the ambient temperature is 105°C.

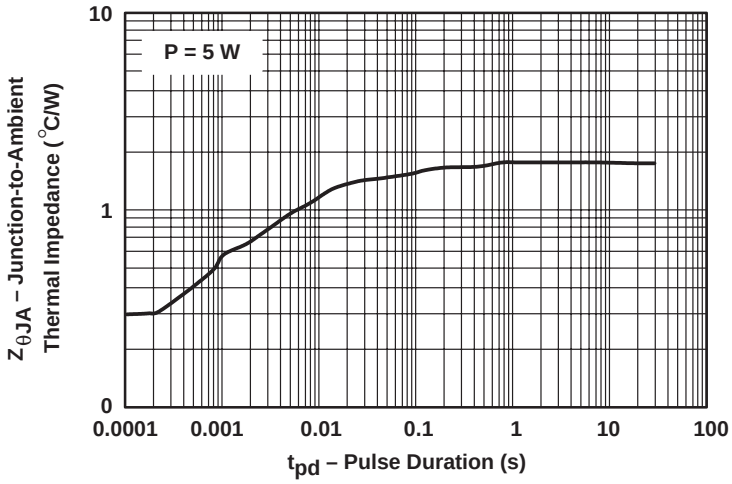


Figure 9. Transient Thermal Impedance of Device 4 in a 7-Pin PowerFLEX Package

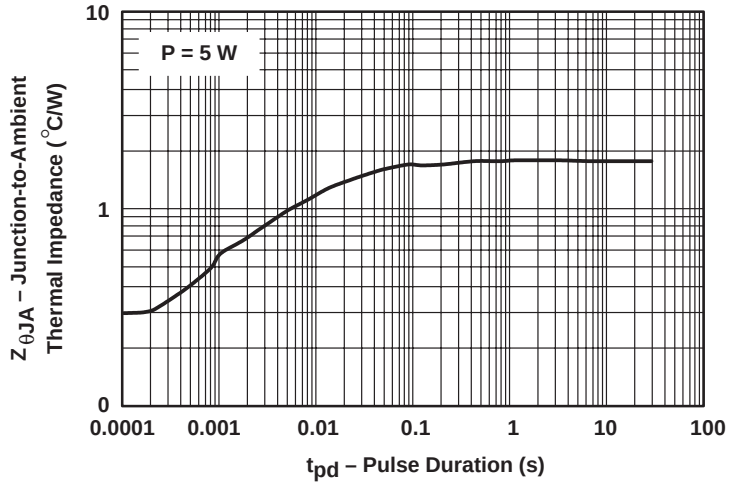


Figure 10. Transient Thermal Impedance of Device 4 in a 15-Pin PowerFLEX Package

Figure 11 is junction-to-case thermal resistance ($R_{\theta JC}$) as a function of power area for 15-pin PowerFLEX packages. This figure summarizes the data measured from devices 1, 2, 3, and 4 in a 15-pin PowerFLEX package. As indicated in this figure, these thermal resistance data points all fall on the same curve and can be described by the same equation. This can provide a way to predict the thermal resistance for any die size when all other assembly parameters are held constant.

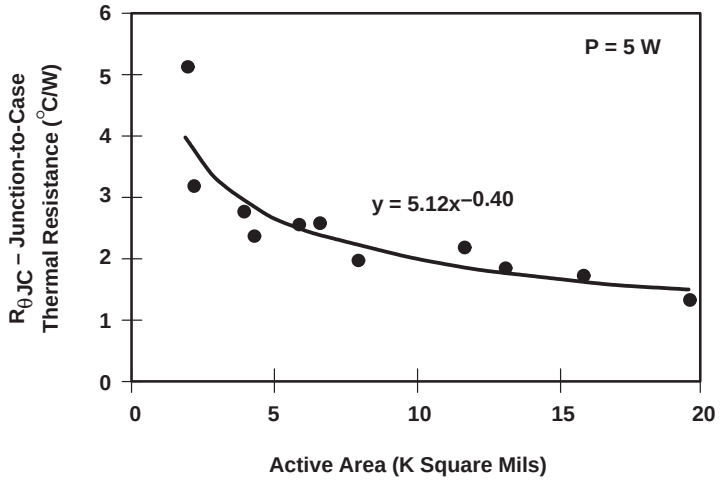


Figure 11. Thermal Resistance as a Function of Power Area for a 15-Pin PowerFLEX Package

Table 5 lists the thermal resistance of PowerFLEX packages of specific die sizes. Power used was 5 W in all cases .

Table 5. Typical Junction-to-Case Thermal Resistances of PowerFLEX Packages

PIN COUNT	2	3/5/7	9/15	14
Die Size (mil^2)	73 x 112	141 x 177	141 x 177	40 x 200
$R_{\theta JC}$ (°C/W)	4.4	1.9	1.8	4.1†

† Preliminary data

When a PowerFLEX package is in intimate contact with an infinite heatsink, the major heat dissipation path follows the silicon-die attach-leadframe-heatsink path since it offers the lowest overall thermal resistance. The junction-to-case thermal resistance ($R_{\theta JC}$) can, therefore, be approximated as the summation of resistances contributed from each individual component,

$$R_{\theta JC} = \sum_i \left(L_i/A_i\right)\left(1/k_i\right) \quad (14)$$

where L_i, A_i, and k_i are the thickness, heat dissipation area, and thermal conductivity of each material, respectively.

The above approximation is true when the package body is small, so that the heat dissipation by natural convection through the package surfaces is negligible. In this approximation, the package size has no significant impact on $R_{\theta JC}$; as can be observed from Table 5, the $R_{\theta JC}$ of 3-/5-/7- and 9-/15-pin packages are approximately the same when the same device was used. This approximation may break down when the heatsink changes from infinite type to finite type, such as a printed circuit board, since other thermal paths may contribute a significant portion of the heat dissipation.

Figure 12 and 13 show the thermal impedances of device 1 with 3 and 1 transistors turned on at various duty cycles (d). The power applied is 5 W in both cases. The curves of various duty cycles were calculated based on equation 13.

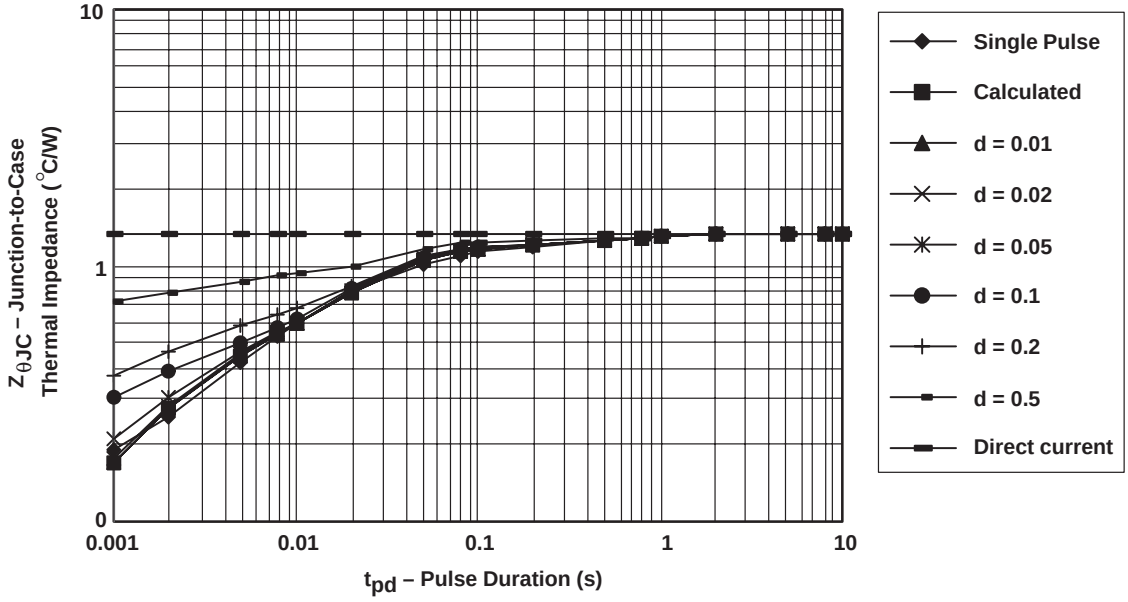


Figure 12. Thermal Impedance of Device 1 with Three Transistors Turned on at Various Duty Cycles

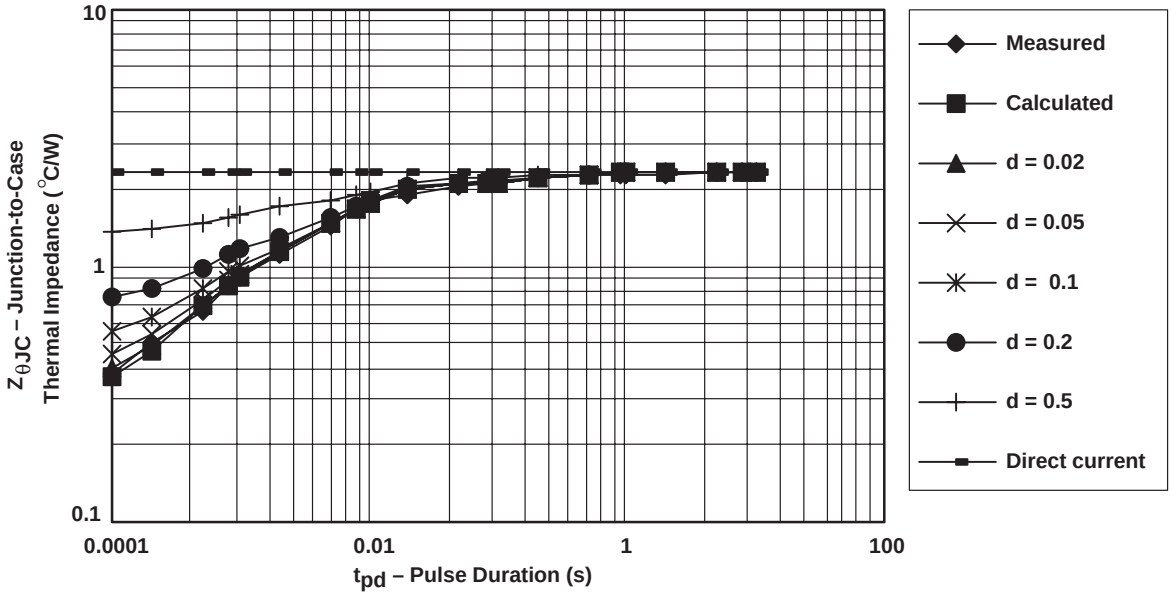


Figure 13. Thermal Impedance of Device 1 with One Transistor Turned on at Various Duty Cycles

Junction-to-Case Thermal Resistance vs. Void Percentage

PowerFLEX packages use silver-flake-filled polymer as the mount material. The quality of the die attach layer can have impact on the junction-to-case thermal resistance ($R_{\theta JC}$) of packages when not properly controlled. Figure 14 shows that void degradation of thermal performance of PowerFLEX packages becomes significant when the void percentage goes above 50 percent.

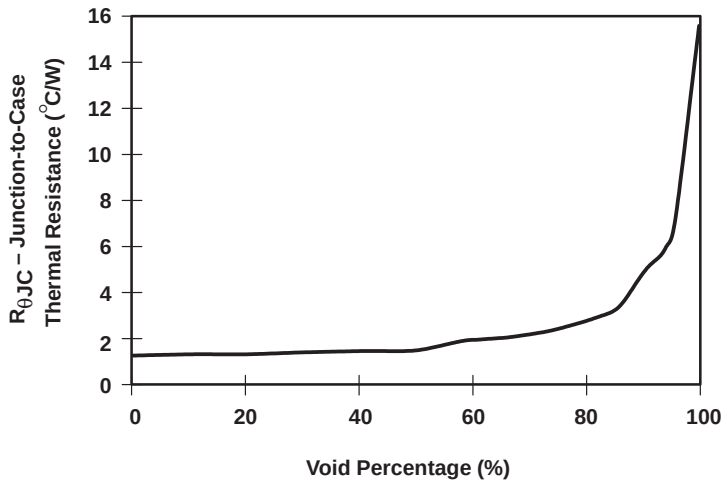


Figure 14. Junction-to-Case Thermal Resistance vs. Percentage Voids for a 7-Pin PowerFLEX Package

$R_{\theta JC}$ vs. Power

Figure 15 and 16 show the junction-to-case thermal resistance versus power dissipation of 15-pin and 7-pin PowerFLEX packages, respectively. The thermal resistance was observed to first decrease rapidly with the power, followed by a relatively constant zone, then increase again when very high powers were applied. The initial high thermal resistance is possibly related to the hot spot effect on the junction due to very low input current. With the increase in input current, the thermal resistance decreased rapidly and reached a constant value for a wide range of power dissipation. The increase of junction-to-case thermal resistance at very high power regimes can be related to the decrease of junction-to-case thermal conductivities of both silicon chip and leadframe materials at high temperatures.

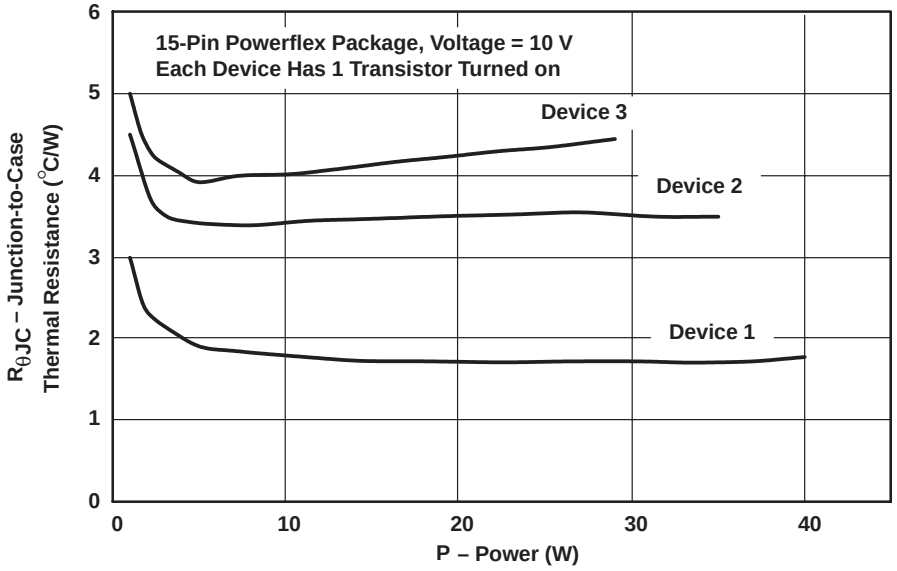


Figure 15. Junction-to-Case Thermal Resistance vs. Power Dissipation of a 15-Pin Package

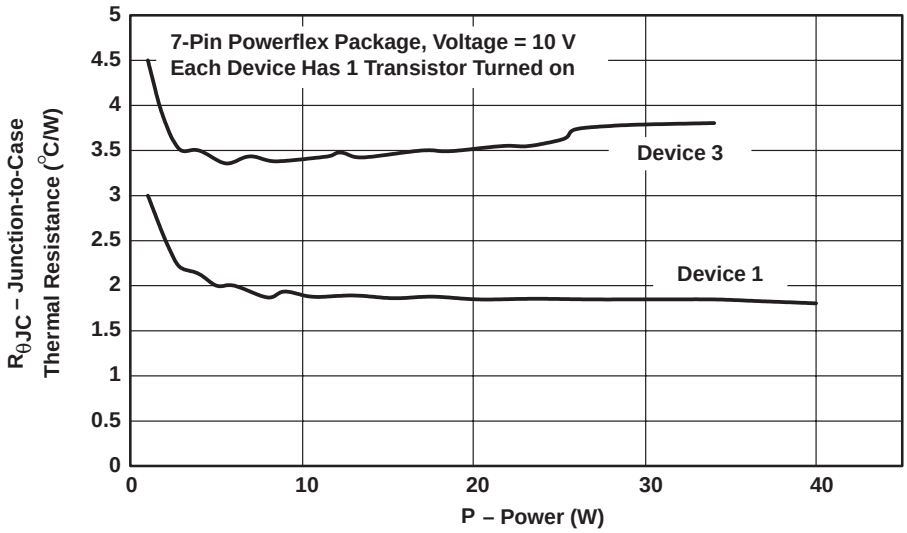


Figure 16. Junction-to-Case Thermal Resistance vs. Power Dissipation of a 7-Pin Package

Junction-to-Ambient Thermal Resistance, $R_{\theta JA}$

Figure 17 shows the junction-to-ambient thermal resistance, $R_{\theta JA}$, measured under still-air conditions. As one can see, the $R_{\theta JA}$ is a very strong function of package size and test board design. When the heatsink changes from an infinite to a finite type, the direct heat dissipation through the exposed leadframe becomes critically dependent on the heatsink efficiency. When the heatsink is not effective in dissipating heat, package size becomes important as convection to the ambient through package surfaces play more of a role in heat dissipation. This can be clearly observed in Figure 17. For packages mounted on a 2-layer board, the thermal resistances of smaller packages were much higher than those of larger packages since a 2-layer board was not as effective as a 4-layer board in heat dissipation. The difference was not that significant for packages mounted on a 4-layer board.

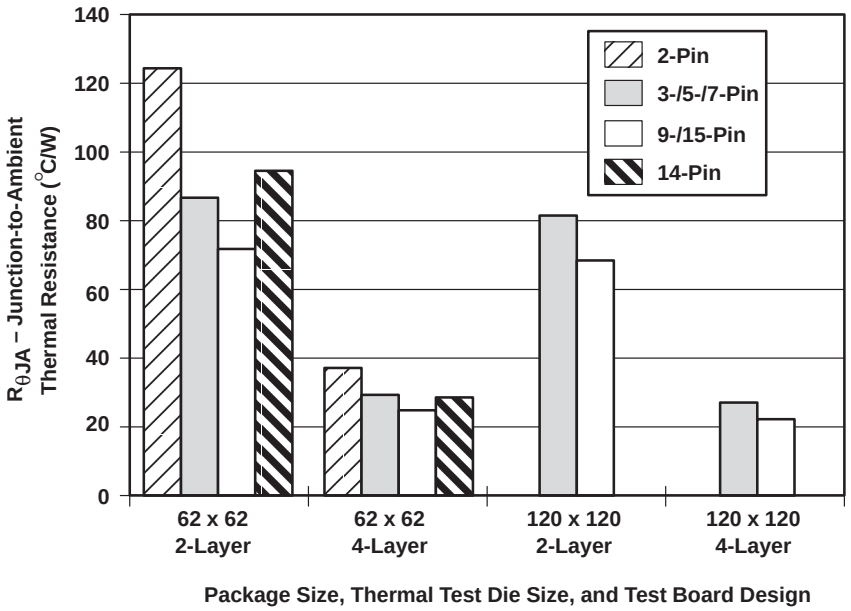
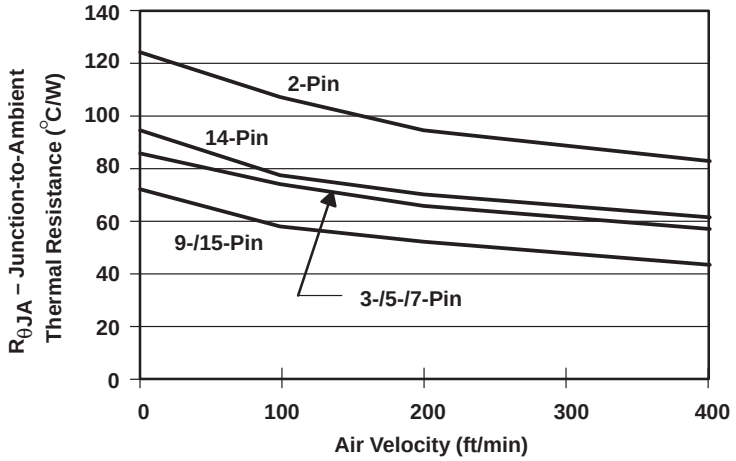


Figure 17. Junction-To-Ambient Thermal Resistances of PowerFLEX Packages Under Still-Air Conditions

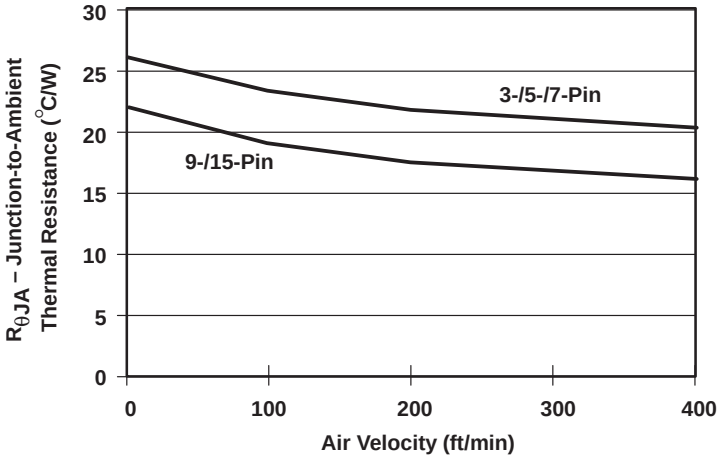
Also, Figure 18(a) and (b) show the $R_{\theta JA}$ of PowerFLEX packages under forced airflow conditions. Although forced air did reduce the $R_{\theta JA}$ of each pin count, it did not change it as much as an effective thermal test board design did. When the airflow changed from still-air conditions to 400 ft/min airflow, the $R_{\theta JA}$ of each pin

count reduced by 30–40% on a 2-layer board, while it was reduced by 20% – 30% on a 4-layer board. This also reflects that heat transfer through package surfaces is more important on a 2-layer board than on a 4-layer board.

There is little or no cooling air available for packages mounted on the printed circuit boards that are inside portable electronic equipment. To effectively remove heat dissipated by the hot devices, printed circuit board design has become the key to successful thermal management in equipment design.



(a) Packages mounted on 2-layer board



(b) Packages mounted on 4-layer board

Figure 18. Junction-to-Ambient Thermal Resistances of PowerFLEX Packages Under Forced-Air Conditions

Figure 19 and 20 show the transient thermal responses of device 4 in a 7-pin and 15-pin PowerFLEX package mounted on a 3-inch x 4.5-inch FR4 board with a 2-oz copper layer on top. Equation 11 can be used to calculate the maximum power for applications requiring low duty cycle and short pulse train.

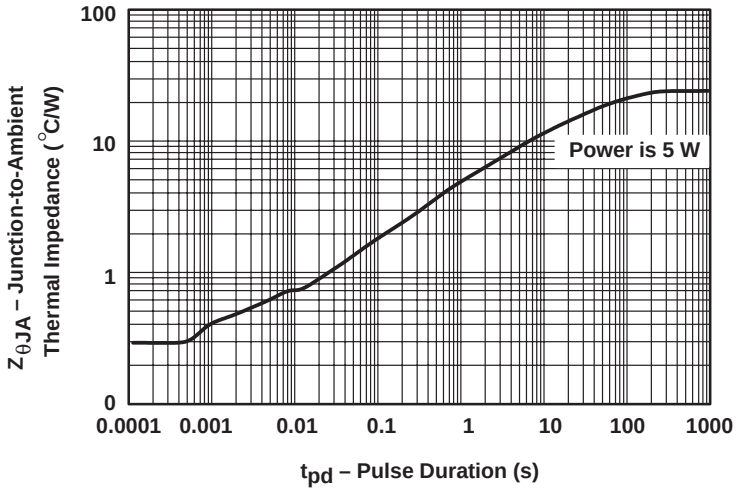


Figure 19. Transient Thermal Impedance of Device 4 in a 7-Pin PowerFLEX Package Mounted on a Printed Circuit Board

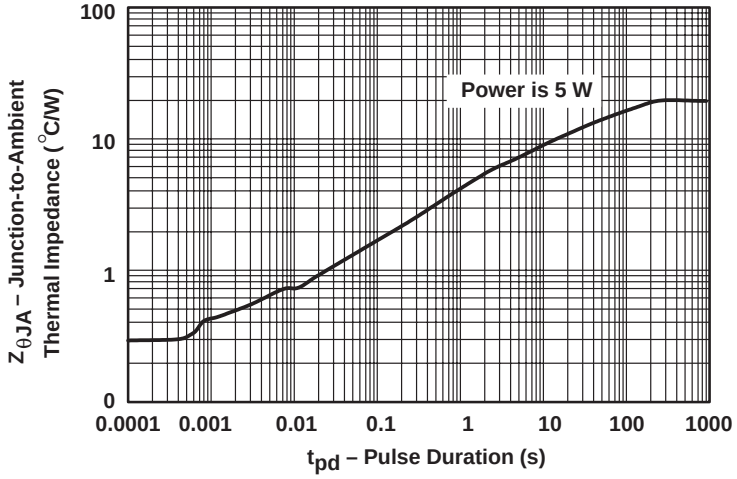


Figure 20. Transient Thermal Impedance of Device 4 in a 15-Pin PowerFLEX Package Mounted on a Printed Circuit Board

REFERENCES

1. JEDEC JC15.1 *Integrated Circuit Thermal Measurement Method – Electrical Test Method (Single Semiconductor Device*).
2. B.W. Williams, *Power Electronics – Devices, Drivers, Applications and Passive Components,* 2nd Edition., McGraw-Hill, Inc., 1995.

SURFACE-MOUNTING PowerFLEX PARTS

Design

Assembly

General Processing Safeguards

References

Over the past decade, surface mount has turned from an art into a science with the development of a general set of design rules and practices. Some of these are more formal, such as IPC-SM-782, Surface-Mount Land Pattern Design, while others are found in books (see References 1 and 2), articles (see Reference 3), and in-house specifications (see Reference 4). The objective of this article is to quickly review these rules and note the way PowerFLEX packaging impacts them.

The interplay of placement requirements, space and thermal constraints, solderability, testability, reparability and cleanability, and reliability has been given the title of Design For Manufacturability (DFM). Such important parts of DFM as cost targets, time-to-market requirements, and board type (I, II or III) are a backdrop to, but not a part of, this discussion. The surface-mount land patterns, sometimes called footprints or pads, and some general observations about board layout will be discussed.

A well designed board that follows the basic surface-mount technology (SMT) considerations greatly improves the cost, cycle time, and quality of the end product. Boards not designed with automation in mind cannot be built on SMT automated equipment, which wastes money, cycle time, and quality. The board envelope dimensions are set by the type of automated SMT being used, and usually include both a minimum and a maximum dimension. Many board shapes can be accommodated, but the front of the board should have a straight and square edge to help machine sensors detect it. Oddly shaped boards and small boards may require panelization or special assembly tooling to process in-line. The most desirable and least costly shape is rectangular with no cutouts. Normally, the maximum module height is taken to be 1.5 inches total height.

Fiducials, the optical alignment targets that align the module to the automated equipment, are an important subject that has received little written attention. These targets should allow vision-assisted equipment to accommodate the shrink and stretch of the raw board during processing. They also define the coordinate

system for all automated equipment such as printing and pick-and-place equipment. The following general guidelines have been found to be most useful:

- Automated equipment requires a minimum of two fiducials, although three are preferred.
- It is helpful when the fuducials are in an L configuration and orthogonal to optimize the stretch/shrink algorithms. When possible, the lower left fiducial should be the design origin (coordinate 0,0).
- All components should be within 4 inches of a fiducial to guarantee placement accuracy. For large boards or panels, a fourth fiducial should be added.
- A wide range of fiducial sizes and shapes can be used. The recommended shape is a circle 0.064 inches in diameter with annulus of 0.126 ID/0.146 OD. The outer ring is optional, but no other feature may be within 0.031 inch of the fiducial.

Two parallel board edges must have a clear zone of 0.125 inch where no component lands or fiducials can be placed. This area is used for conveyor transfer and eliminates the need for tooling. The cleared zone should be along the longest edges of the board, and the width should be based on machine handling capability. Panelization or breakaway tabs may be used as part of this cleared zone.

Panelization, as mentioned above, needs to be defined and addressed. It is the process where PWB material is left attached to the board by tabs with the intention of removing it later after assembly. There are two reasons to do this. The first is to build multiples of a board at the same time. This reduces the touch labor associated with loading and handling of individual boards. It also reduces the amount of machine run time, as the machine does not stop between boards for loading. The second reason for panelization is for small or odd-shaped boards. The extra material takes the place of an expensive tool and fits the board to an acceptable machine envelope. As little as a single board per panel may be run with this approach. Even at that level, it can save significant operator touch time and tooling cost. Panelization should be considered whenever either one of the above conditions exists. Since PWBs are already fabricated in panels, panelization should not be an extra effort for the board manufacturer.

Since PowerFLEX parts are not fine pitch, the many spacing considerations for fine-pitch layouts are beyond the scope of this article. However, since interpackage spacing is one of the key aspects of DFM, the question of how close you can safely put components next to each other is a critical one. The following list of component layout considerations are recommendations based on TI experience:

- A minimum of 0.02 inch should exist between lands of adjacent components to reduce the risk of shorting.
- The recommended minimum space between surface-mount device (SMD) component bodies is equal to the height of the tallest component. This allows for a 45° soldering angle in case manual work is needed.
- Polarization symbols need to be provided for discrete SMDs (diodes, tantalum capacitors, etc.) next to the positive pin.
- Pin-one indicators or features are needed to determine the keying of SMD components.
- Space between lands (under components) on backside discrete components should be a minimum of 0.03 inch. No open vias may be in this space.
- The direction of backside discretes for wave solder should be perpendicular to the direction through the wave.
- Fine-pitch components must allow for a step-down zone of at least 0.1 inch outside of the lands. No leadless chip carriers may be placed in this zone. This allows proper step-down regions for stencil manufacturing. A stencil opening must have an aspect ratio of opening to stencil thickness of 1:1.5 (meaning the maximum thickness of the stencil is two thirds of the opening size). The recommended standard stencil sizes are 12 mils thick for 50-mil components and discretes and 8 mils thick for 31.5-mil to 25-mil pitch.
- Do not put SMT components on the bottom side that exceed 200 grams per square inch of surface area (contact area with board).
- Space permitting, symbolize all reference designators within the land pattern of the respective components.
- It is preferred to have all components oriented in well-ordered columns and rows.
- Group similar components together whenever possible.
- Room for testing needs to be allowed.

The actual design of the land areas is addressed in the section on thermal management. There are two sets of pad designs included in this report, the standard footprints and the thermally enhanced footprints. Either set of footprints can be used, depending on the end use and preference of the end user.

The final step in design is to put together a data package for automated build. The data package will vary slightly from application to application, but at a minimum, will include:

- Bill of Materials
- Reference Designator List
- Component location data (X–Y data)
- Placement plot or assembly drawing
- Bare board specifications
- Gerber/Artwork and Aperture List

There is probably more literature on solders, solder pastes, and the printing of them than on any other aspect of surface-mount technology. The authors recommend Jennie Hwang's book (see Reference 5) as an excellent source for information on this subject. PowerFLEX parts do not present any unusual challenges for either solder paste application or placement. Parts can be shipped in either tube or tape-and-reel formats for ease of use in automated pick-and-place machines.

Fluxes and the move toward no-clean systems is another subject that has created a great deal of literature without any clear direction. PowerFLEX parts have been successfully mounted using mild (RA) fluxes without any reliability problems. No problems are anticipated with current no-clean systems.

Solder-reflow conditions are the next critical step in the surface-mount process. During reflow, the solvent in the solder paste evaporates, the flux cleans the metal surfaces, the solder particles melt, wetting of the metal surfaces takes place by wicking of the molten solder, and finally, solidification of the solder into a strong metallurgical bond completes the process. The desired end result is a uniform layer of solder strongly bonded to both the PWB and the package with few or no voids and a smooth, even fillet around the package. Conversely, when all the steps are not carefully fitted together, voids, gaps, uneven thickness, and insufficient fillet can occur. While the exact cycle used depends on the type of reflow system used, there are several key points all successful cycles have in common.

The first of these is a warm-up period sufficient to safely evaporate the solvent. This can be done with a pre-heat or bake, or by a hold in the cycle at evaporation temperatures, or even both, depending on the paste used. If there is less solvent in the paste (such as in a high viscosity, high metal-content paste), then the hold can be shorter. However, when the hold is not long enough to get all of the solvent out, or too fast to allow it to evaporate, many negative things happen. These range from solder-ball formation or heating too fast, to heating entrapped gas in the

solder, which leads to embrittlement due to not leaving enough time to complete evaporation. A significant number of reliability problems with solder joints can be solved with the warm-up step, so it needs careful attention.

The second thing successful cycles have in common is uniform heating across the package and the board. Solder will wick to the hottest spot, so uneven solder joint thickness may be an indicator that the profile needs adjusting. This may be more of a problem with some reflow methods, such as infrared (IR) reflow, than with others such as forced hot-air convection heating.

The type of reflow method used will also affect the third thing successful cycles have in common, which is a balance between too low, too late, or too short of a temperature, leading to insufficient flux activation, and too high, too long of a temperature, leading to excessive flux activation and oxidation. Heating the solder too hot and too fast before it melts can also dry the paste, leading to poor wetting.

PowerFLEX parts have been successfully mounted using the cycles shown in Figure 21. Vapor phase reflow and forced hot-air convection heating were used to perform the reflow operations. Visual inspections of the fillets showed good fillet formation.

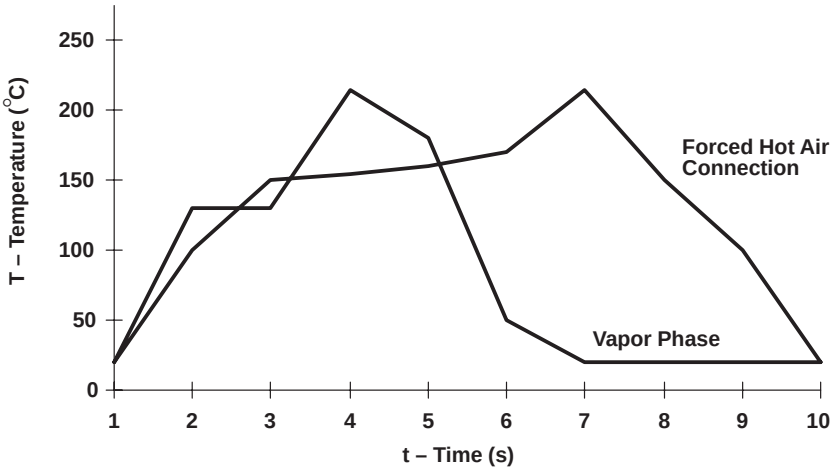


Figure 21. Typical Profiles Used for Reflow Soldering of PowerFLEX Parts

At this point, a brief discussion of fillets is needed. The PowerFLEX leads are plated with palladium (Pd) to eliminate the need for solder dipping or plating. This means that the visual appearance of the joint will differ slightly from the tin/lead (Sn/Pb)-dipped lead. Since the only solder available for joint formation is the screened-down type, the solder will probably not cover the top of the joint. Also, Pd joints tend to be somewhat duller in appearance. Texas Instruments has performed extensive testing which shows that Pd joints are as strong or stronger than Sn/Pb joints (Reference 6).

Thermal Management

Effective thermal management is the culmination of many factors. Many of these factors have been discussed elsewhere in this monograph. Thermal management with PowerFLEX packages depends on moving the primary thermal management from the package to the system. This, in turn, requires that the thermal connections between the various parts of the system (i.e., die to thermal pad, thermal pad to PWB, PWB to heatsink) be as efficient as possible. This discussion considers ways to make the thermal conduction between the thermal pad of the package and the land area on the PWB highly efficient.

The primary enemy to the efficient transmittal of heat from the thermal pad of the package to the land area of the PWB is solder voiding. Therefore, we need to consider ways to reduce or eliminate the voids in the solder. The first of these methods has already been discussed. Proper reflow cycles are the first line of defense against voiding. The second is package and board cleanliness.

The third method is the primary focus of this discussion, the footprint pattern on the PWB. Figure 22 (see the section on *Footprints for Soldering*) shows the conventional footprint pattern for the a typical PowerFLEX package—in this case, the 15-lead package. Extensive experience has shown that it is very difficult to make solder joints with this type of footprint that are free of trapped gas and other void-forming defects. The solution recommended by Texas Instruments is shown in Figure 23. In Figure 23, the land areas are broken up by channels that allow the gases to escape. When the width of the channels is held to about 0.02 inch,

experience has further shown that the solder wets across the top of the channel on the surface of the thermal pad to form a nearly continuous layer. This gives an upside-down fillet or a tunnel along the channels that provides a very efficient thermal path.

When extra reliability is desired, posts of solder mask can be printed to hold the package up, off the PWB surface. This has the effect of increasing the solder thickness to the height of the post and imposes solder uniformity across the entire joint.

GENERAL PROCESSING SAFEGUARDS

During the solder-reflow process, packages and assemblies are subjected to heat that, in some cases, can be above the rated temperature for the device. Therefore, precaution should be taken to carefully control both the duration and peak temperature that these devices receive. The packages should always be preheated, and the temperature differential between the preheat and the peak temperature should never exceed 100°C. A better practice is to keep this differential between 50°C and 75°C. The maximum soldering temperature should never exceed 260°C for more than 5 seconds.

Care should be exercised on cooldown as well as heat-up. Forced cooling can generate unacceptable thermal and mechanical stresses in the solder joint, leading to reduced joint lifetime and early failure. A very useful rule of thumb is to allow at least 3 minutes of unforced cooling. Rapid, jarring movement of the assembly during the reflow process can also cause package dislocation, stress buildup, and other undesirable effects.

The heat across the assembly should be kept as even as possible, both for solder thickness reasons discussed above and to keep built-in stress as low as possible. No more than 10°C should be allowed, even (or especially) with IR heating.

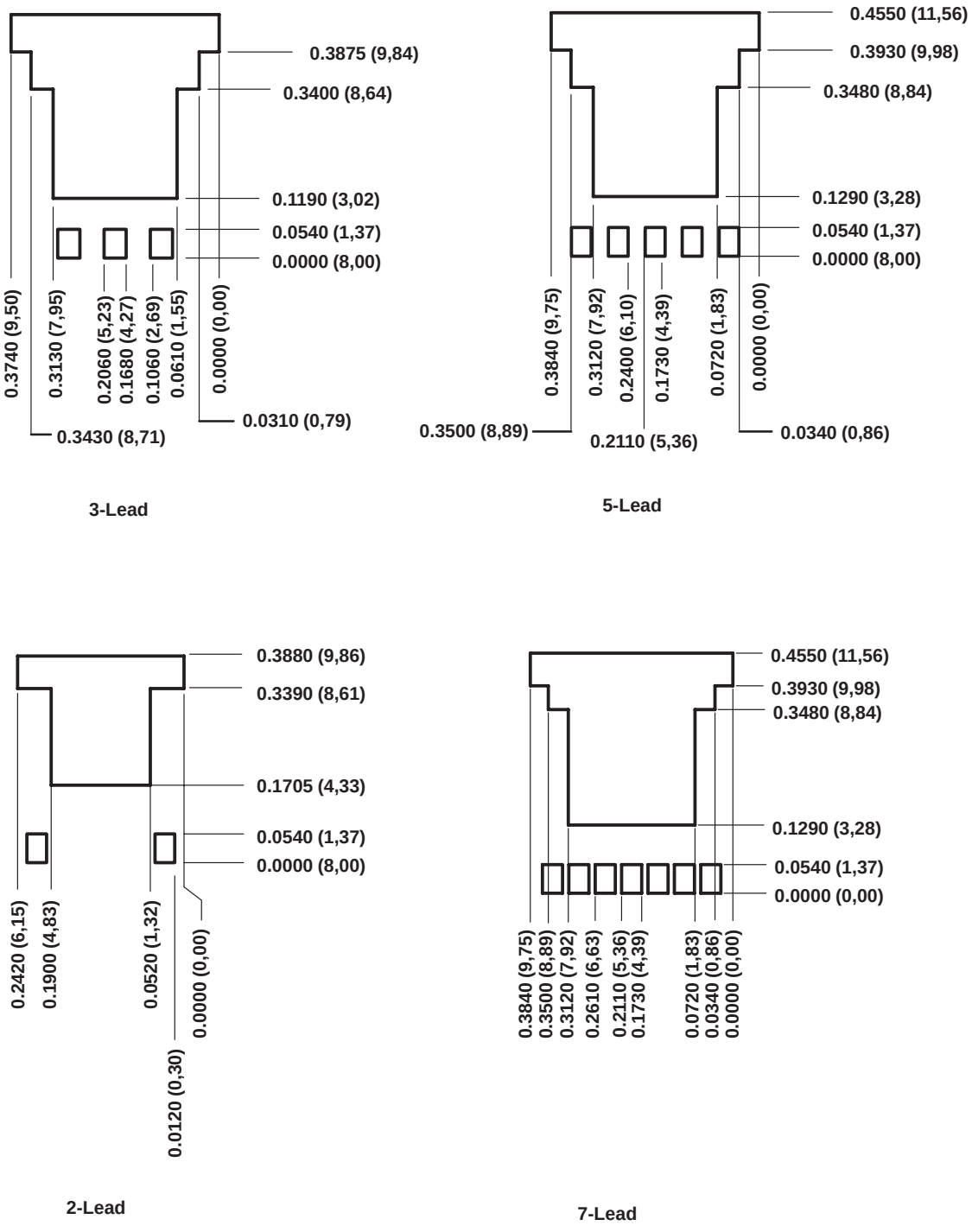
Wave soldering is not recommended for PowerFLEX package attachment. Attaining the level of void-free attachment needed between the thermal pad and the PWB is almost impossible with wave-soldering techniques.

REFERENCES

1. *Surface Mount Technology*, ISHM Technical Monograph, Silver Spring, MD, 1984.
2. Ray Prasad, *Surface Mount Technology: Principles and Practice*, Van Nostrand and Reinhold, New York, 1997.
3. *Surface Mount in 10 Easy Steps*, SMT Magazine, IHS Publishing Group, a series of 10 monthly installments in 1994.
4. Curtis Clark, *SMT Design Guidelines for Assembly*, private communication.
5. Jennie S. Hwang, *Solder Paste in Electronics Packaging*, Van Nostrand and Reinhold, New York, 1992.
6. Douglas Romm, *Palladium Lead Finish User's Manual*, Texas Instruments, Dallas, TX.

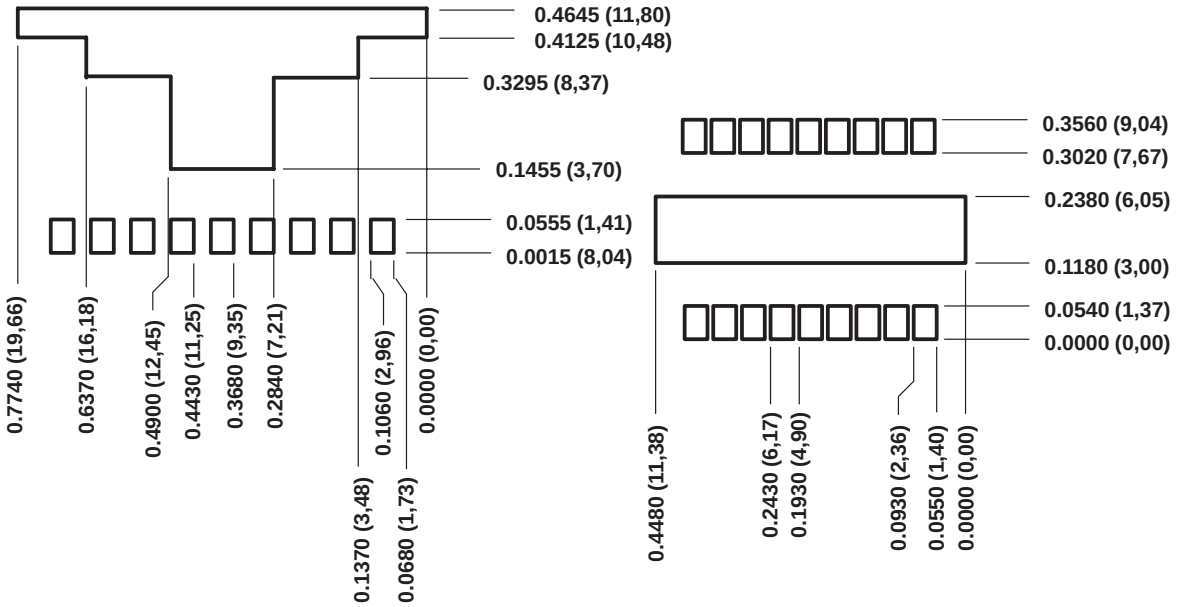
FOOTPRINTS FOR SOLDERING

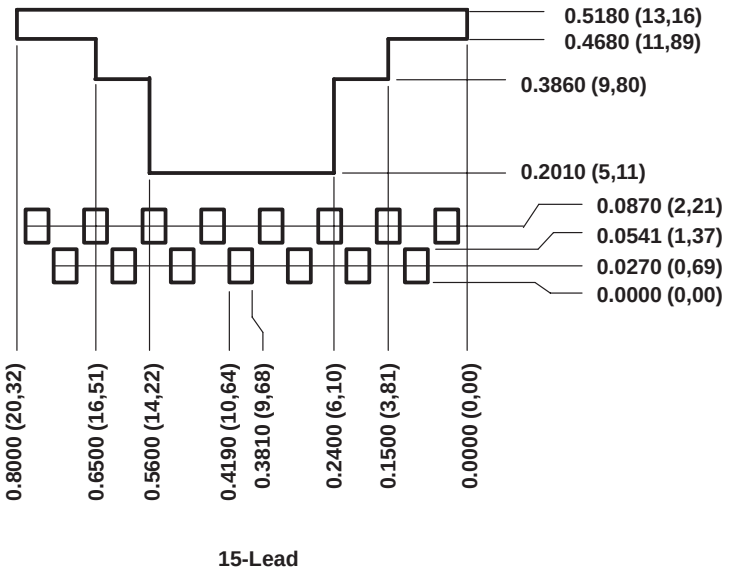
PowerFLEX Footprints



NOTE A: All linear dimensions are in inches (mm).

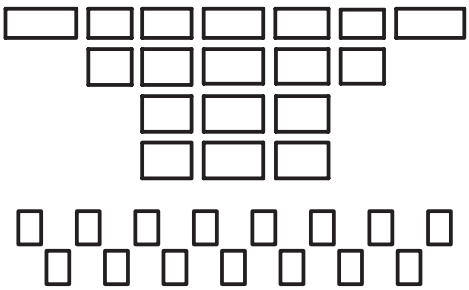
Figure 22. PowerFLEX Package Footprints





NOTE A: All linear dimensions are in inches (mm).

Figure 22. PowerFLEX Package Footprints (Continued)



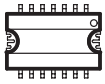
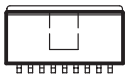
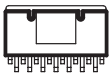
15-Lead

Figure 23. Segmented 15-Lead Footprint

PACKAGE OUTLINES

PowerFLEX Line-up

PowerFLEX LINE-UP

PINS	2/3	3	5	7	9	14	15
PITCH	0.180/0.090	0.100	0.067	0.050	0.075	0.050	0.050
PACKAGE TYPE							
Surface Mount 						R–PDSO–G14 DBX 	
Surface Mount 	R–PSFM–G2 KTP  .282 x .238 x .075	R–PSFM–G3 KTE  .355 x .370 x .075	R–PSFM–G5 KTG  .355 x .370 x .075	R–PSFM–G7 KTN  .355 x .370 x .075	R–PSFM–G9 KTA  .380 x .770 x .075		R–PSFM–G15 KTC & KTR  .380 x .770 x .075