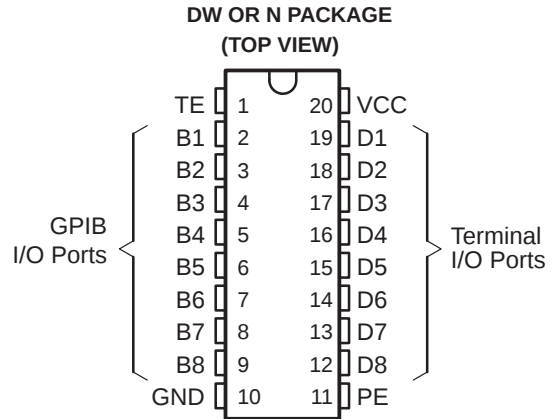


SN75163B

OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

SLLS006A – D2611, OCTOBER 1985 – REVISED FEBRUARY 1993

- 8-Channel Bidirectional Transceivers
- Power-Up/Power-Down Protection (Glitch Free)
- High-Speed Low-Power Schottky Circuitry
- Low Power Dissipation . . . 66 mW Max Per Channel
- High-impedance PNP Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device Is Powered Down ($V_{CC} = 0$)



description

The SN75163B octal general-purpose interface bus transceiver is a monolithic, high-speed, low-power Schottky device. It is designed for two-way data communications over single-ended transmission lines. The transceiver features driver outputs that can be operated in either the open-collector or 3-state modes. If talk enable (TE) is high, these outputs have the characteristics of open-collector outputs when pullup enable (PE) is low and of 3-state outputs when PE is high. Taking TE low places the outputs in the high-impedance state. The driver outputs are designed to handle loads of up to 48 mA of sink current. Each receiver features pnp transistor inputs for high input impedance and 400 mV of hysteresis for increased noise immunity.

NOT RECOMMENDED FOR NEW DESIGN

Output glitches during power up and power down are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when $V_{CC} = 0$.

The SN75163B is characterized for operation from 0°C to 70°C.

Function Tables

EACH DRIVER				EACH RECEIVER			
INPUTS			OUTPUT B	INPUTS			OUTPUT D
D	TE	PE		B	TE	PE	
H	H	H	H	L	L	X	L
L	H	H	L	H	L	X	H
H	X	L	Z	X	H	X	Z
L	H	L	L				
X	L	X	Z				

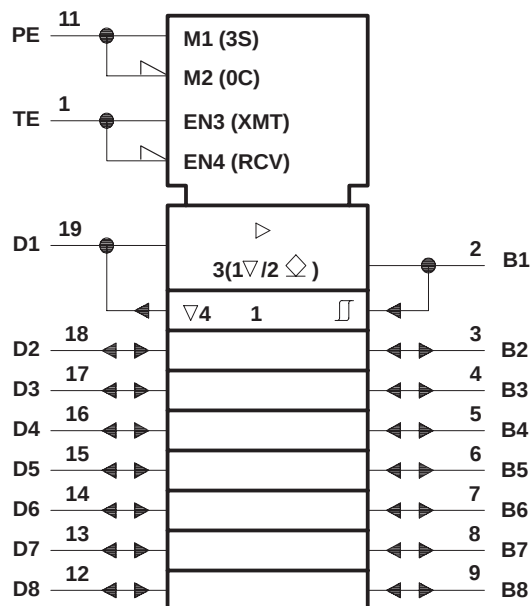
H = high level, L = low level, X = irrelevant, Z = high-impedance state

SN75163B

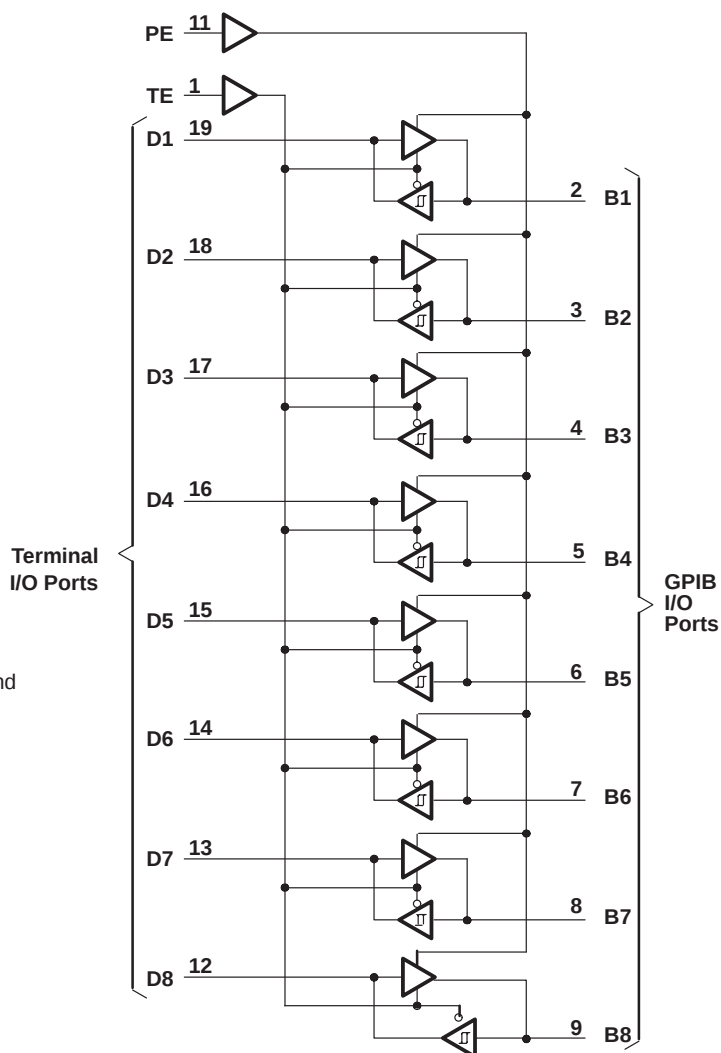
OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

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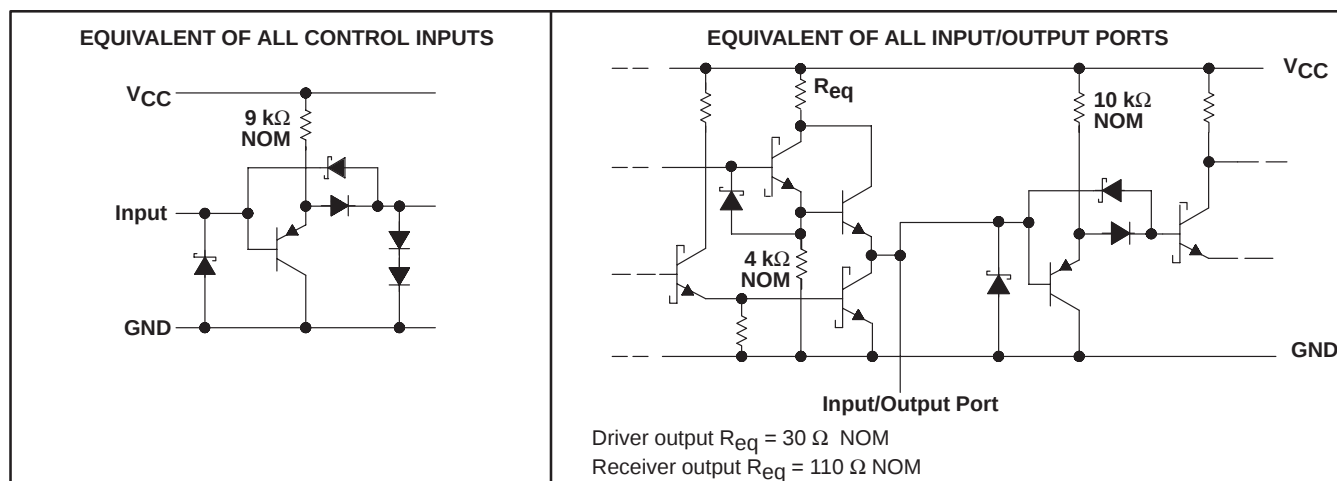
logic symbol†



logic diagram (positive logic)



schematics of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Low-level driver output current	100 mA
Continuous total power dissipation (see Note 2)	See Dissipation Rating Table
Operating free-air temperature range	0°C to 70°C
Storage temperature range	– 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds	260°C

NOTES: 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			–10	mA
	Terminal ports			–800	μA
High-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C



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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V _{IK}	Input clamp voltage		I _I = –18 mA	–0.8	–1.5		V
V _{hys}	Hysteresis (V _{T+} – V _{T–})	Bus	See Figure 8	0.4	0.65		V
V _{OH}	High-level output voltage	Terminal	I _{OH} = –800 µA, TE at 0.8 V	2.7	3.5		V
		Bus	I _{OH} = –10 mA, PE and TE at 2 V	2.5	3.3		
V _{OL}	Low-level output voltage	Terminal	I _{OL} = 16 mA, TE at 0.8 V		0.3	0.5	V
		Bus	I _{OL} = 48 mA, PE and TE at 2 V		0.4	0.5	
I _{OH}	High-level output current (open-collector mode)	Bus	V _O = 5.5 V, PE at 0.8 V, D and TE at 2 V			100	µA
I _{OZ}	Off-state output current (3-state mode)	Bus	PE at 2 V, V _O = 2.7 V			20	µA
			TE at 0.8 V, V _O = 0.4 V			–20	
I _I	Input current at maximum input voltage	Terminal	V _I = 5.5 V		0.2	100	µA
I _{IH}	High-level input current	Terminal	V _I = 2.7 V		0.1	20	µA
I _{IL}	Low-level input current	Terminal	V _I = 0.5 V		–10	–100	µA
I _{OS}	Short-circuit output current	Terminal		–15	–35	–75	mA
		Bus		–25	–50	–125	
I _{IL}	Supply current	No load	Receivers low and enabled			80	mA
			Drivers low and enabled			100	
C _{I/O(bus)}	Bus-port capacitance		V _{CC} = 5 V to 0, V _{I/O} = 0 to 2 V, f = 1 MHz		30		pF

[†] All typical values are at V_{CC} = 5, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C _L = 30 pF, See Figure 1		14	20	ns
t _{PHL}	Propagation delay time, high-to-low-level output					14	20	
t _{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C _L = 30 pF, See Figure 2		10	20	ns
t _{PHL}	Propagation delay time, high-to-low-level output					15	22	
t _{PZH}	Output enable time to high level	TE	Bus	See Figure 3		25	35	ns
t _{PHZ}	Output disable time from high level					13	22	
t _{PZL}	Output enable time to low level					22	35	
t _{PLZ}	Output disable time from low level					22	32	
t _{PZH}	Output enable time to high level	TE	Terminal	See Figure 4		20	30	ns
t _{PHZ}	Output disable time from high level					12	20	
t _{PZL}	Output enable time to low level					23	32	
t _{PLZ}	Output disable time from low level					19	30	
t _{en}	Output pullup enable time	PE	Terminal	See Figure 5		15	22	ns
t _{dis}	Output pullup disable time					13	20	



PARAMETER MEASUREMENT INFORMATION

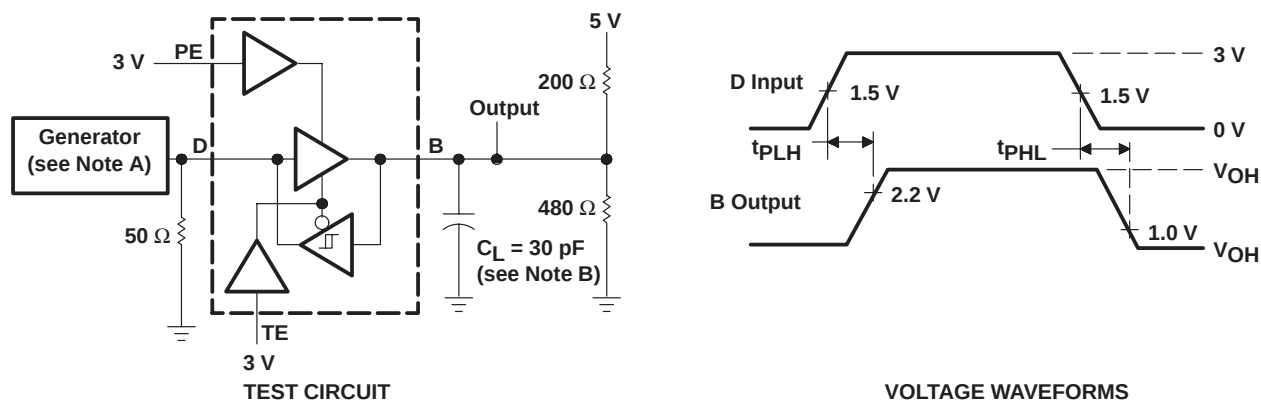


Figure 1. Terminal-to-Bus Test Circuit and Voltage Waveforms

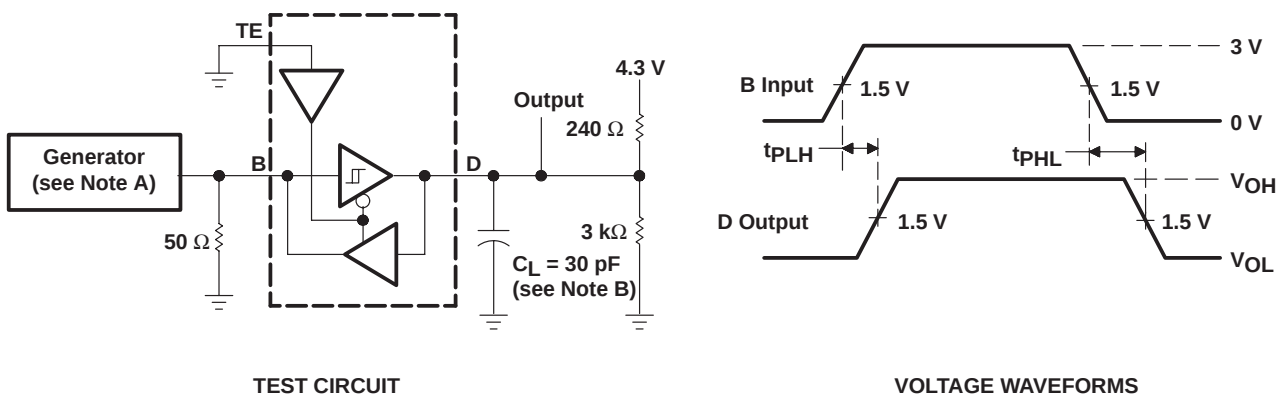


Figure 2. Bus-to-Terminal Test Circuit and Voltage Waveforms

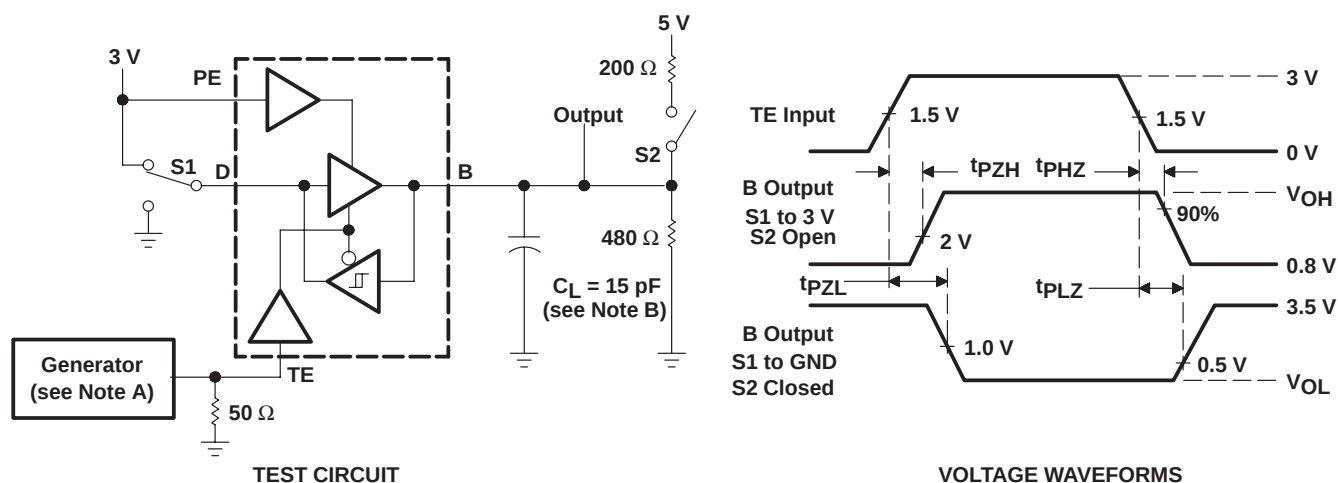


Figure 3. TE-to-Bus Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR $\leq$ 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

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TEST CIRCUIT

Generator (see Note A) is connected to the TE input of the 74VHC04 through a 50 Ω resistor. The output of the inverter is connected to a 240 Ω resistor, which is then connected to a 3 kΩ resistor and a 15 pF load capacitor ($C_L = 15 \text{ pF}$, see Note B). The output is also connected to a 4.3 V source through a switch S2. The input B is connected to a 3 V source through a switch S1.

VOLTAGE WAVEFORMS

The top waveform shows the TE Input (1.5 V) and D Output (1.5 V) for S1 to 3 V and S2 Open. The propagation delay t_{PHZ} is the time from the input transition to the output transition. The rise time t_{PZH} is the time for the output to rise from 90% V_{OH} to 100% V_{OH} .

The bottom waveform shows the TE Input (1.5 V) and D Output (1.0 V) for S1 to GND and S2 Closed. The propagation delay t_{PLZ} is the time from the input transition to the output transition. The fall time t_{PZL} is the time for the output to fall from 90% V_{OL} to 100% V_{OL} .

TEST CIRCUIT

Generator (see Note A)

PE

50 Ω

D

3 V

TE

B

$R_L = 480 \Omega$

$C_L = 15 \text{ pF}$ (see Note B)

Output

VOLTAGE WAVEFORMS

PE Input

1.5 V

1.5 V

3 V

0 V

t_{PD}

t_{dis}

B Output

2 V

90%

V_{OH}

$V_{OL} = 0.8 \text{ V}$

NOTES: C. The input pulse is supplied by a generator having the following characteristics: $\text{PRR} \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_O = 50 \Omega$.
D. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

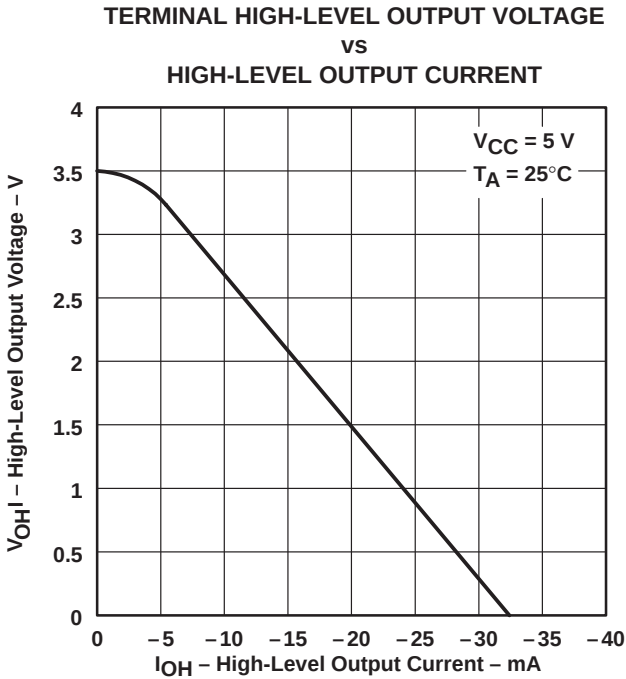


Figure 6

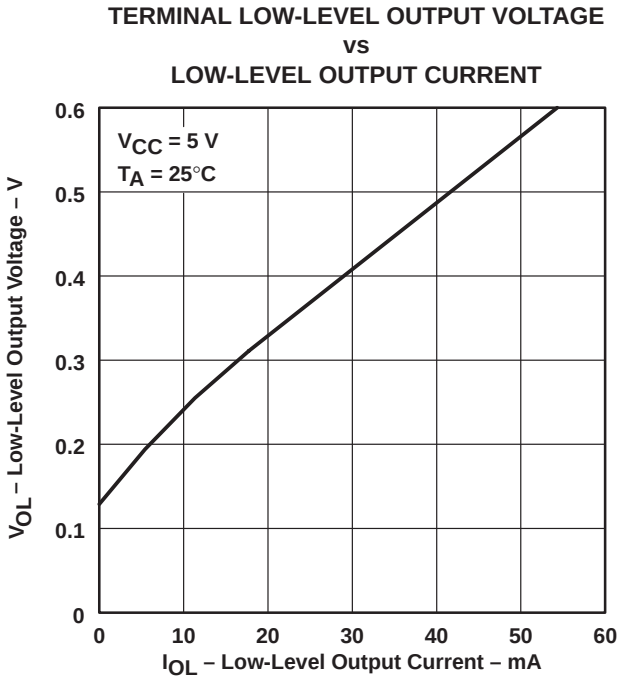


Figure 7

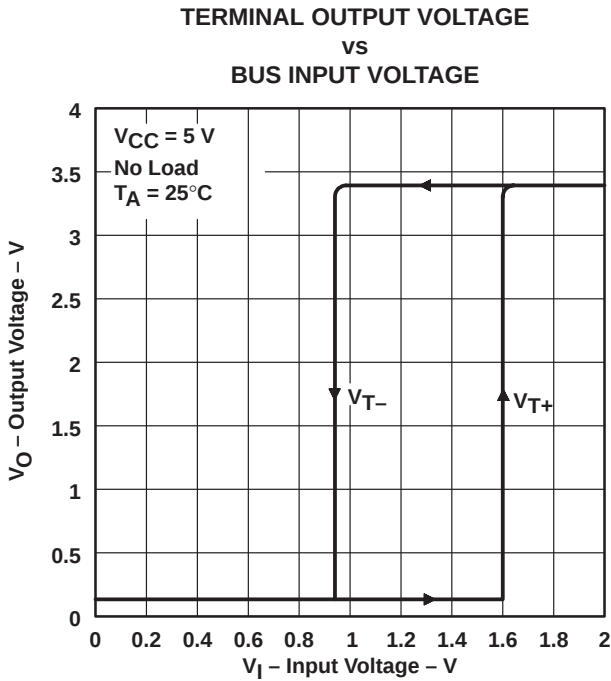


Figure 8

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TYPICAL CHARACTERISTICS

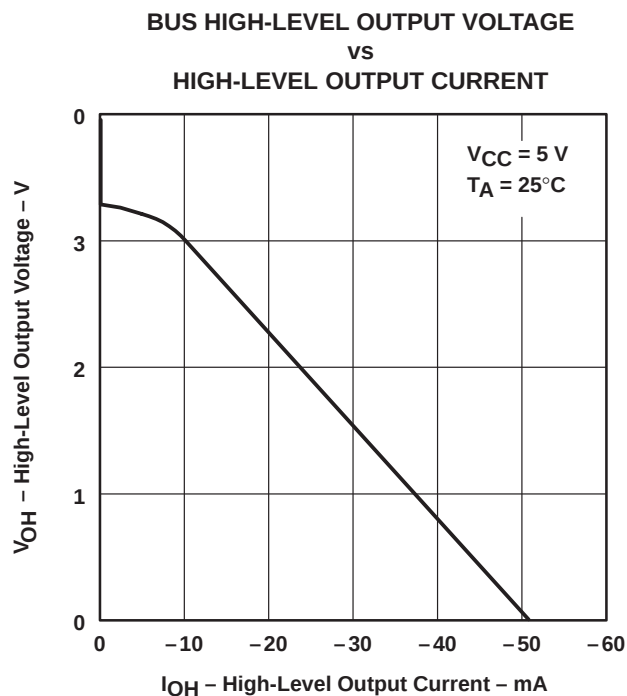


Figure 9

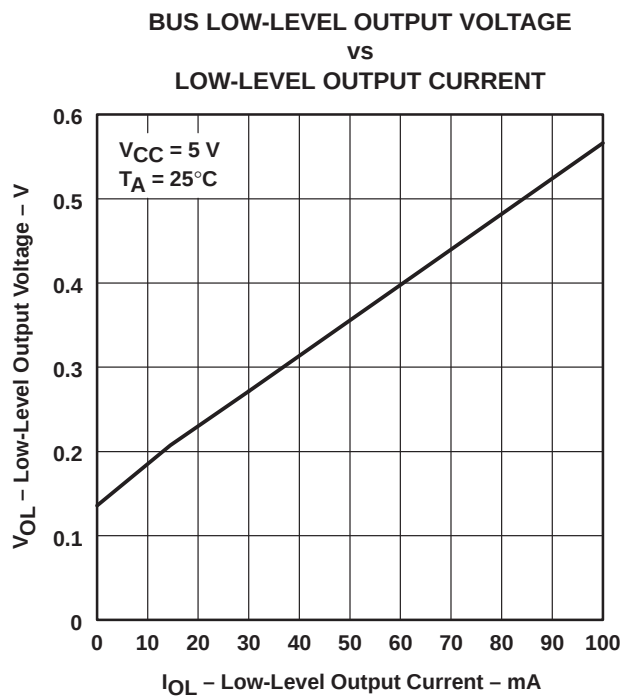


Figure 10

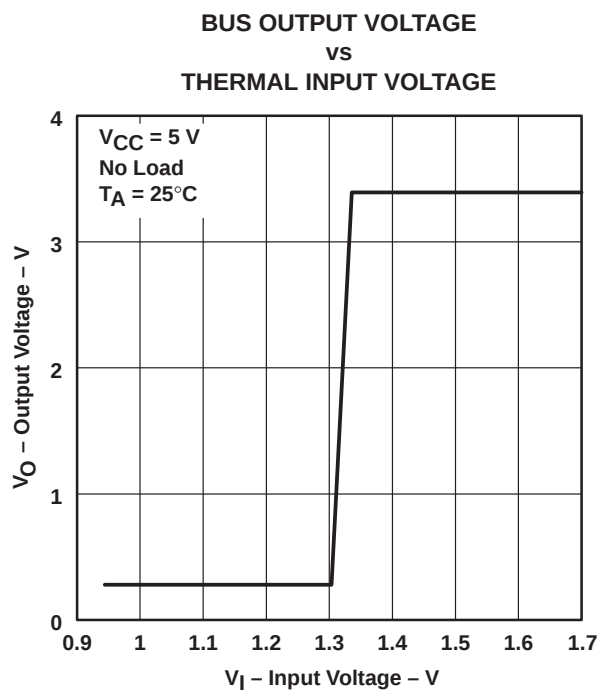


Figure 11

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