- **Supports Provisions of IEEE 1394-1995 Standard for High Performance Serial Bus†**
- **Fully Interoperable with FireWire™ Implementation of IEEE 1394-1995**
- **Provides Three Fully Compliant Cable Ports at 100/200 Megabits per Second (Mbits/s)**
- **Cable Ports Monitor Line Conditions for Active Connection to Remote Node**
- **Device Power-Down Feature to Conserve Energy in Battery-Powered Applications**
- **Inactive Ports Disabled to Save Power**
- **Logic Performs System Initialization and Arbitration Functions**
- **Encode and Decode Functions Included for Data-Strobe Bit-Level Encoding**
- **Incoming Data Resynchronized to Local Clock**
- **Single 3.3-V Supply Operation**
- **Interface to Link-Layer Controller Supports Optional Annex J Electrical Isolation and TI™ Bus-Holder Isolation**
- **Data Interface to Link-Layer Controller Provided Through 2/4 Parallel Lines at 50 Mbits/s**
- **25-MHz Crystal Oscillator and PLL Provide Transmit/Receive Data at 100/200 Mbits/s, and Link-Layer Controller Clock at 50 MHz**
- **Interoperable with 1394 Link-Layer Controllers Using 5-V Supplies**
- **Interoperable Across 1394 Cable with 1394 Physical Layers (Phy) Using 5-V Supplies**
- **Node Power-Class Information Signaling for System Power Management**
- **Cable Power Presence Monitoring**
- **Separate Cable Bias and Driver Termination Voltage Supply for Each Port**
- **Multiple Separate Package Terminals Provided for Analog and Digital Supplies and Grounds**
- **High Performance 64-Pin TQFP (PM) Package**

description

The TSB21LV03 provides the analog physical layer functions needed to implement a three-port node in a cable-based IEEE 1394-1995 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The TSB21LV03 is designed to interface with a link-layer controller (LLC), such as the TSB12LV21, TSB12LV31, or TSB12C01A.

The TSB21LV03 requires either an external 24.576-MHz crystal or crystal oscillator. The internal oscillator drives an internal phase-locked loop (PLL), which generates the required 196.608-MHz reference signal. The 196.608-MHz reference signal is internally divided to provide the 49.152/98.304-MHz clock signals that control transmission of the outbound encoded strobe and data information. The 49.152-MHz clock signal is also supplied to the associated LLC for synchronization of the two chips and is used for resynchronization of the received data. The power-down function, when enabled by taking the PD terminal high, stops operation of the PLL and disables all circuitry except the cable-not-active signal circuitry.

The TSB21LV03 supports an optional isolation barrier between itself and its LLC. When $\overline{\text{ISO}}$ is tied high, the link interface outputs behave normally. When $\overline{\text{ISO}}$ is tied low, internal differentiating logic is enabled, and the outputs become short pulses, which can be coupled through a capacitor or transformer as described in the IEEE 1394-1995 Annex J.

† This serial bus implements technology covered by one or more patents of Apple Computer, Incorporated and INMOS, Limited.

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description (continued)

Data bits to be transmitted through the cable ports are received from the LLC on two or four data lines (D0 – D3), and are latched internally in the TSB21LV03 in synchronization with the 49.152-MHz system clock. These bits are combined serially, encoded, and transmitted at 98.304 or 196.608 Mbits/s as the outbound data-strobe information stream. During transmission, the encoded data information is transmitted differentially on the TPB cable pair(s), and the encoded strobe information is transmitted differentially on the TPA cable pair(s).

During packet reception the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded Strobe information is received on the TPB cable pair. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are split into two or four parallel streams, resynchronized to the local system clock, and sent to the associated LLC. The received data is also transmitted (repeated) out of the other active (connected) cable ports.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common mode voltage is used during arbitration to set the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage for the presence of the remotely supplied twisted-pair bias voltage. The presence or absence of this common-mode voltage is used as an indication of cable connection status. The cable connection status signal is internally debounced in the TSB21LV03 on a cable disconnect-to-connect. The debounced cable connection status signal initiates a bus reset. On a cable disconnect-to-connect a debounce delay is incorporated. There is no delay on a cable disconnect.

The TSB21LV03 provides a 1.86 V nominal bias voltage for driver load termination. This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. The value of this bias voltage has been chosen to allow interoperability between transceiver chips operating from either 5-V or 3-V nominal supplies. This bias voltage source should be stabilized by using an external filter capacitor of approximately 1.0 μF.

The transmitter circuitry is disabled under the following conditions: power down, cable not active, reset, or transmitter disable. The receiver circuitry is disabled under the following conditions: power down, cable not active, or receiver disable. The twisted-pair bias voltage circuitry is disabled under the following conditions: power down or reset. The power-down condition occurs when the PD input is high. The cable-not-active (CNA) condition occurs when the cable connection status indicates that no cable is connected. The reset condition occurs when the $\overline{\text{RESET}}$ input terminal is low. The transmitter disable and receiver disable conditions are determined from the internal logic.

The line drivers in the TSB21LV03 operate in a high-impedance current mode and are designed to work with external 112-Ω line-termination resistor networks. One network is provided at each end of each twisted-pair cable. Each network is composed of a pair of series-connected 56-Ω resistors. The midpoint of the pair of resistors that is directly connected to the twisted-pair A (TPA) package terminals is connected to the TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the twisted-pair B (TPB) package terminals is coupled to ground through a parallel RC network with recommended resistor and capacitor values of 5 KΩ and 250 pF respectively. The values of the external resistors are designed to meet the draft standard specifications when connected in parallel with the internal receiver circuits and are shown in Figure 3.

The driver output current, along with other internal operating currents, is set by an external resistor. This resistor is connected between the R0 and R1 terminals and has a value of 6.3 kΩ, ±0.5%.

description (continued)

Four package terminals are used as inputs to set four configuration status bits in the self-identification (Self-ID) packet. These terminals are hardwired high or low as a function of the equipment design. PC0 – PC2 are the three terminals that indicate either the need for power from the cable or the ability to supply power to the cable. The fourth terminal, C/LKON, indicates whether a node is a contender for bus manager. When the C/LKON terminal is asserted, it means the node can be a contender for bus manager. When the terminal is not asserted, it means that the node is not a contender. The C bit corresponds to bit 20 in the Self-ID packet, PC0 corresponds to bit 21, PC1 corresponds to bit 22, and PC2 corresponds to bit 23 (see Table 4–29 of the IEEE 1394–1995 standard for additional details).

A power-down terminal, PD, is provided to allow a power-down mode where most of the TSB21LV03 circuits are powered down to conserve energy in battery-powered applications. A cable status terminal, CNA, provides a high output when all twisted-pair cable ports are disconnected. This output is not debounced. The CNA output can be used to determine when to power the TSB21LV03 down or up. In the power-down mode all circuitry is disabled except the CNA circuitry. It should be noted that when the device is powered-down it does not act in a repeater mode.

When the power supply of the TSB21LV03 is removed while the twisted-pair cables are connected, the TSB21LV03 transmitter and receiver circuitry has been designed to present a high impedance to the cable in order to not load the TPBias terminal voltage on the other end of the cable.

If the TSB21LV03 is being used with one or more of the ports not being brought out to a connector, the TSB terminals must be terminated for reliable operation. For each unused port, the TPB+ and TPB– terminals must be tied together and connected to GND. This is done in the normal termination network. When a port does not have a cable connected, the normal termination network pulls TPB+ and TPB– to ground through a 5-kΩ resistor, thus disabling the port.

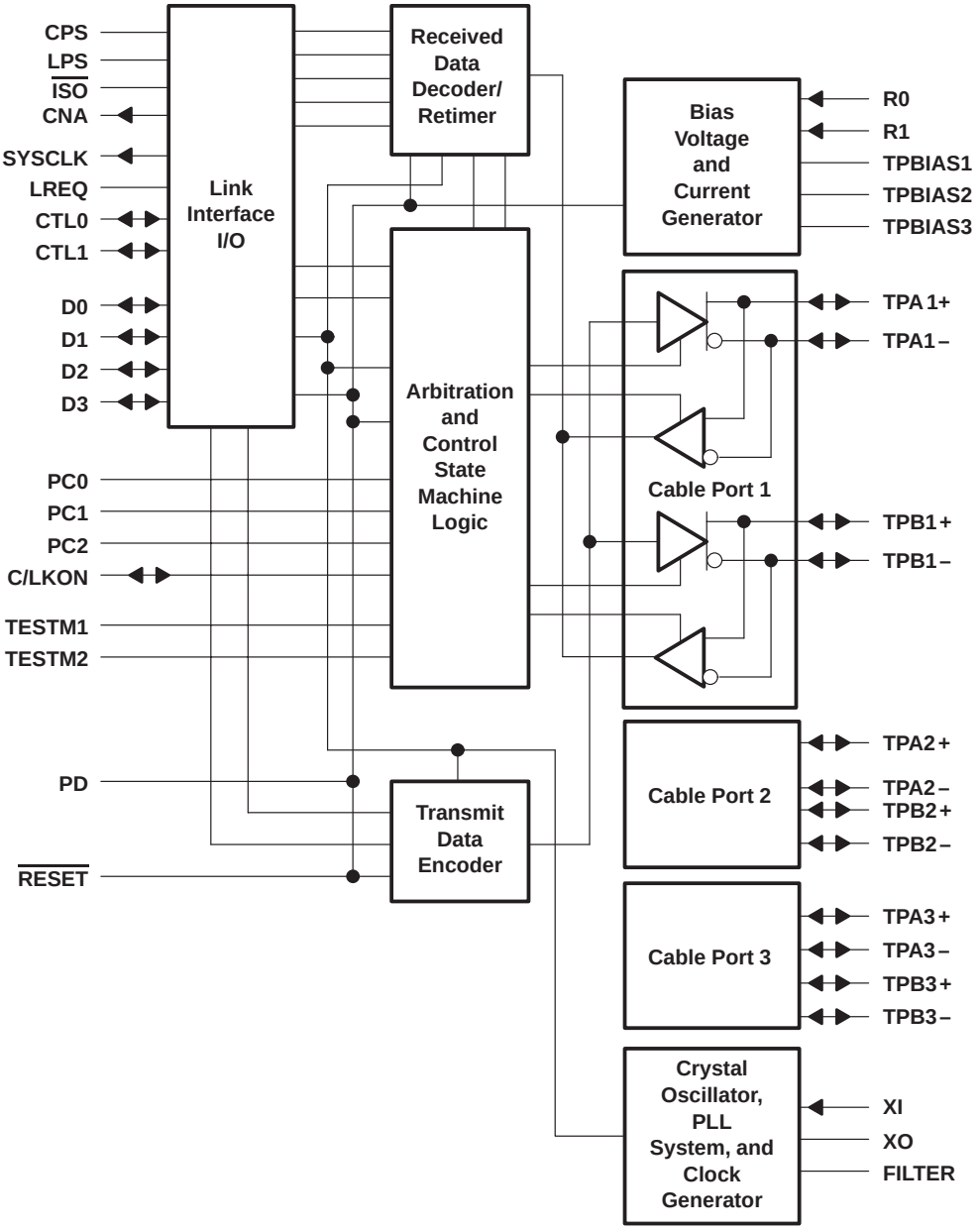
NOTE:

All gap counts on all nodes of a 1394 bus must be identical. This may only be accomplished by using phy configuration packets (see section 4.3.4.3 of IEEE 1394-1995 Standard) or by using two bus resets, which resets the gap counts to the maximum level (3Fh).

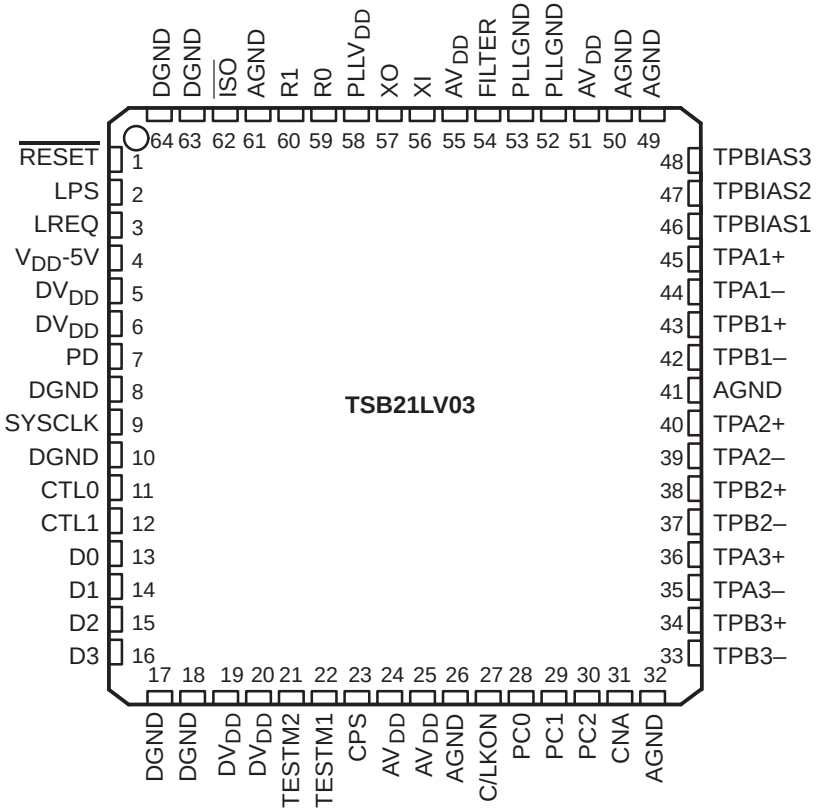
The link power status (LPS) terminal works with the C/LKON terminal to manage the LLC power usage of the node. The LPS terminal indicates that the LLC of the node is powered down and powers down the phy-LLC interface to save power. If the phy then receives a link-on packet, the C/LKON terminal is activated to output a 6.114 MHz signal, which can be used by the LLC to power itself up. Once the LLC is powered up, the LPS signal communicates this to the TSB21LV03 and the C/LKON signal is turned off and the phy-link interface is enabled.

Two of the package terminals are used to set up various test conditions used in manufacturing. These terminals, TESTM1 and TESTM2, should be connected to V_{DD} for normal operation.

functional block diagram



package outline



Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE	I/O	DESCRIPTION
AGND	26, 32, 41, 49, 50, 61	Supply	—	Analog circuit ground. All AGND terminals should be tied together to the low-impedance circuit-board ground plane.
AV_{DD}	24, 25, 51, 55	Supply	—	Analog circuit power. A combination of high frequency decoupling capacitors near each AV_{DD} terminal is suggested, such as 0.1-μF and 0.001-μF capacitors. Lower frequency 10-μF filtering capacitors are also recommended. AV_{DD} terminals are separated from DV_{DD} terminals internally from the other supply terminals to provide noise isolation. They should be tied together at a low-impedance point on the circuit board. Each supply source should be individually filtered.
C/LKON	27	CMOS	I/O	Bus manager capable (input). When set as an input, C/LKON specifies in the Self-ID packet that the node is bus manager capable.
				Link-on (output). When set as an output, C/LKON indicates the reception of a link-on message by asserting a 6.114-MHz signal. The bit value programming is done by tying the terminal through a 10-kΩ resistor to V_{DD} (high, bus manager capable) or to GND (low, not bus manager capable). Using either the pullup or pulldown resistor allows the C/LKON output to override the input value when necessary.
CNA	31	CMOS	O	Cable-not-active output. CNA is asserted high when none of the TSB21LV03 ports are connected to another active port. This circuit remains active during the power-down mode.
CPS	23	CMOS	I	Cable power status. CPS is normally connected to the cable power through a 400-kΩ resistor. This circuit drives an internal comparator that detects the presence of cable power. This information is maintained in two internal registers and is available to the LLC by way of a register read (see the Phy-Link Interface Annex in the IEEE 1394-1995 standard).
CTL0 CTL1	11 12	CMOS	I/O	Control I/O. The CTLn terminals are bidirectional communications control signals between the TSB21LV03 and the LLC. These signals control the passage of information between the two devices. Control I/O terminals are 5-V tolerant.
D0 – D3	13, 14, 15, 16	CMOS	I/O	Data I/O. The D terminals are bidirectional and pass data between the TSB21LV03 and the LLC. Data I/O terminals are 5-V tolerant.
DGND	8, 10, 17, 18, 63, 64	Supply	—	Digital circuit ground. The DGND terminals should be tied to the low-impedance circuit-board ground plane.
DV_{DD}	5, 6, 19, 20	Supply	—	Digital circuit power. DV_{DD} supplies power to the digital portion of the device. It is recommended that a combination of high-frequency decoupling capacitors be connected to DV_{DD} (i.e., paralleled 0.1 μF and 0.001 μF). Lower frequency 10-μF filtering capacitors can also be used. These supply terminals are separated from AV_{DD} internally in the device to provide noise isolation. These terminals should also be tied at a low-impedance point on the circuit board. Individual filtering networks for each is desired.
FILTER	54	CMOS	I/O	PLL filter. FILTER is connected to a 0.1-μF capacitor and then to PLLGND to complete the internal lag-lead filter. This filter is required for stable operation of the frequency multiplier PLL running off of the crystal oscillator.
$\overline{ISO}$	62	CMOS	I	Link interface isolation disable input. $\overline{ISO}$ controls the operation of an internal pulse differentiating function used on the phy-LLC interface terminals, CTLn and Dn, when they operate as outputs. When $\overline{ISO}$ is asserted low, the optional isolation barrier is implemented between TSB21LV03 and its LLC (as described in Annex J of IEEE 1394-1995). $\overline{ISO}$ is normally tied high to disable isolation differentiation.
LPS	2	CMOS	I	Link power status. LPS is connected to either the V_{DD} supplying the LLC or to a pulsed output that is active when the LLC is powered for the purpose of monitoring the LLC power status. The pulsed signal must be between 220 kHz and 5.5 MHz to be sensed as active. If LPS is inactive, the phy-LLC interface is disabled, and the TSB21LV03 performs only the basic repeater functions required for network initialization and operation. LPS is 5-V tolerant.
LREQ	3	CMOS	I	Link request. LREQ is an input from the LLC that requests the TSB21LV03 to perform some service. LREQ is 5-V tolerant.
PC0 – PC2	28, 29, 30	CMOS	I	Power class indicators. The PC signals set the bit values of the three power-class bits in the Self-ID packet (bits 21, 22, and 23). These bits can be programmed by tying the terminals to V_{DD} (high) or to GND (low).
PD	7	CMOS	I	Power down. When asserted high, PD turns off all internal circuitry except the CNA monitor circuits that drive the CNA terminal. PD is 5-V tolerant.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	TYPE	I/O	DESCRIPTION
PLLGND	52, 53	Supply	—	PLL circuit ground. The PLLGND terminals should be tied to the low-impedance circuit-board ground plane.
$PLLV_{DD}$	58	Supply	—	PLL circuit power. $PLLV_{DD}$ supplies power to the PLL portion of the device. It is recommended that a combination of high-frequency decoupling capacitors be connected to $PLLV_{DD}$ (i.e., paralleled 0.1 μF and 0.001 μF). Lower frequency 10-μF filtering capacitors can also be used. These supply terminals are separated from AV_{DD} and DV_{DD} internally in the device to provide noise isolation. These terminals should also be tied at a low-impedance point on the circuit board. Individual filtering networks for each is desired.
R0 R1	59 60	—	—	Current setting resistor. An internal reference voltage is applied to a resistor connected between R0 and R1 to set the operating current and the cable driver output current. A low temperature-coefficient resistor (TCR) 6.3 kΩ ±5% resistor should be used to meet the IEEE 1394-1995 standard requirements for output voltage limits.
$\overline{\text{RESET}}$	1	CMOS	I	Reset. When $\overline{\text{RESET}}$ is asserted low (active), a bus reset condition is set on the active cable ports and the the internal logic is reset to the reset start state. An internal pullup resistor, which is connected to V_{DD}, is provided so only an external delay capacitor is required. This input is a standard logic buffer and can also be driven by an open-drain logic output buffer. The minimum hold time for RESET is listed in the recommended operating characteristics table.
SYSCLK	9	CMOS	O	System clock. SYSCLK provides a 49.152-MHz clock signal, which is synchronized with the data transfers to the LLC.
TESTM1 TESTM2	22 21	CMOS	I	Test mode control. TESTM1 and TESTM2 are used during the manufacturing test and should be tied to V_{DD}.
TPA1+ TPA2+ TPA3+	45 40 36	Cable	O	Portn, port cable pair A. TPAn is the port A connection to the twisted-pair cable. Board traces from these terminals should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPA1– TPA2– TPA3–	44 39 35			
TPB1+ TPB2+ TPB3+	43 38 34	Cable	O	Portn, port cable pair B. TPBn is the port B connection to the twisted-pair cable. Board traces from these terminals should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPB1– TPB2– TPB3–	42 37 33			
TPBIAS1 TPBIAS2 TPBIAS3	46 47 48	Cable	O	Portn, twisted-pair bias. TPBIASn provides the 1.86-V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers and for sending a valid cable connection signal to the remote nodes.
V_{DD}–5V	4	Supply	—	5-V V_{DD} supply. V_{DD}–5V should be connected to the LLC V_{DD} supply when a 5-V LLC is connected to the phy, and it should be connected to the phy DV_{DD} when a 3-V LLC is used.
XI XO	56 57	—	—	Crystal oscillator. XO and XI connect to a 24.576-MHz parallel resonant fundamental mode crystal. Although, when a 24.576-MHz crystal oscillator is used, it can be connected to XI with XO left unconnected. The optimum values for the external shunt capacitors are dependent on the specifications of the crystal used. The suggested values of 12 pF are appropriate for a crystal with 15-pF specified loads.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} . . . . . –0.3 V to 4 V
Input voltage range, V_I . . . . . –0.5 V to V_{DD}+0.5 V
Output voltage range at any output, V_O . . . . . –0.5 V to V_{DD}+0.5V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
PM	1350 mW	10.8 mW/°C	865 mW

‡ This is the inverse of the traditional junction-to-case thermal resistance ($R_{\theta JA}$) and uses a board-mounted 92.5°C/W.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	Source power node	3.0	3.3	3.6	V
	Nonsource power node§	2.7	3	3.6	
High-level input voltage, V_{IH}	CMOS inputs	0.7V_{DD}			V
Low-level input voltage, V_{IL}	CMOS inputs			0.2V_{DD}	V
Differential input voltage, V_{ID}	Cable inputs, 100-Mbit operation	142		260	mV
	Cable inputs, 200-Mbit operation	132		260	
	Cable inputs, during arbitration	171		262	
Common-mode input voltage, V_{IC}	TPB cable inputs, 100-Mbit or speed signaling off, Source power node	1.165		2.515	V
	TPB cable inputs, 100-Mbit or speed signaling off, Nonsource power node§	1.165		2.015	
	TPB cable inputs, 200-Mbit speed signaling, Source power node	0.935		2.515	
	TPB cable inputs, 200-Mbit speed signaling, Nonsource power node§	0.935		2.015	
Receive input jitter	TPA, TPB cable inputs, 100-Mbit operation			±1.08	ns
	TPA, TPB cable inputs, 200-Mbit operation			±0.5	
Receive input slew	Between TPA and TPB cable inputs, 100-Mbit operation			±0.8	ns
	Between TPA and TPB cable inputs, 200-Mbit operation			±0.55	
Output current, I_{OL}/I_{OH}	SYSCLK	–16		16	mA
	Control, Data, CNA and C/LKON outputs	–12		12	
Output current, I_O	TPBIAS outputs	–3		1.3	mA
Hold time, power-up reset ($\overline{RESET}$)		2			ms

§ For a node that does not source power (see Section 4.2.2.2 in IEEE 1394–1995 Standard).

electrical characteristics over recommended operating conditions (unless otherwise noted)

driver

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{OD}	Differential output voltage	56-Ω load	172		265	mV
$V_{(OFF)}$	Off-state common-mode output voltage	Drivers disabled			20	mV
$I_{O(diff)}$	Differential current (TPA+, TPA–, TPB+, TPB–)	Driver enabled, Speed signaling off	–1.05†		1.05†	mA
$I_{(SP)}$	Common-mode speed signaling current (TPB+, TPB–)	200-Mbit speed signaling enabled	–2.53‡		–4.84‡	mA

† Limits are defined as the algebraic sum of TPA+ and TPA– driver currents. Limits also apply to TPB+ and TPB– as the algebraic sum of driver currents.
‡ Limits are defined as the absolute limit of each of TPB+ and TPB– driver currents.

receiver

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IT}	Input threshold voltage		–30		30	mV
V_{IT}	Cable bias-detect input threshold voltage, TPBn cable inputs	Driver disabled	0.6		1.0	V
I_{IC}	Common-mode input current	Driver disabled	–20		20	μA
Z_{ID}	Differential input impedance	Driver disabled	15		6	kΩ pF
Z_{IC}	Common-mode impedance	Driver disabled	20		24	kΩ pF

device

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
I_{DD}	Supply current	V_{DD} = 3.3 V	Node transmitting or repeating		114		mA
			Node receiving		140		mA
		V_{DD} = 3.6 V				175	mA
		V_{DD} = 3.6 V,	Power-down mode		10		
V_{IT}	Power status input threshold voltage (CPS)	R_L = 400 kΩ		4.7		7.5	V
V_{OH}	High-level output voltage	V_{DD} = min,	I_{OH} max	V_{DD}–0.55			V
V_{OL}	Low-level output voltage	V_{DD} = max,	I_{OL} min			0.5	V
I_I	Input current (LREQ, LPS, PD, TESTM1, TESTM2, PC0, PC1, PC2)	V_I = V_{DD} or 0				±1	µA
I_{off}	Off-state output current (CTL0, CTL1, D0, D1, D2, D3, C/LKON)	V_O = V_{DD} or 0				±5	µA
	Pullup current (RESET)	V_I = 1.5 V		–20	–40	–80	µA
		V_I = 0		–22	–45	–90	
	Power-up reset time ($\overline{\text{RESET}}$)			2			ms
V_{TH+}	Positive arbitration comparator-input threshold voltage			89		168	mV
$V_{TH–}$	Negative arbitration comparator-input threshold voltage			–168		–89	mV
V_{IT}	Speed-signal input threshold voltage			49		131	mV
V_{IT+}	Positive input threshold voltage (LREQ, CTLn, Dn)			V_{DD}/2+0.12		V_{DD}/2+0.66	V
$V_{IT–}$	Negative input threshold voltage (LREQ, CTLn, Dn)			V_{DD}/2–0.66		V_{DD}/2–0.12	V
V_O	Output voltage (TPBIAS1, TPBIAS2, TPBIAS3 termianls)			1.665		2.015	V
	Bus holding current (LREQ, CTLn, Dn termianls)	V_I = 1/2 (V_{DD})			250		µA

thermal characteristics

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board mounted, No air flow		92.5		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			10.4		°C/W

switching characteristics

PARAMETER		MEASURED	TEST CONDITION	MIN	TYP	MAX	UNIT
	Jitter, transmit	TPA, TPB				±0.25	ns
	Skew rate, transmit	Between TPA and TPB				±0.15	ns
t_r	Rise time, transmit	10% to 90%	R_L=56Ω, C_L=10 pF			2.2	ns
t_f	Fall time, transmit	90% to 10%	R_L=56Ω, C_L=10 pF			2.2	ns
t_{su}	Setup time, Dn, CTLn, LREQ↑↓ to SYSCLK↑	50% to 50%	See Figure 1	5			ns
t_h	Hold time, Dn, CTLn, LREQ↑↓ before SYSCLK↑	50% to 50%	See Figure 1	2			ns
t_d	Delay time, SYSCLK↑ to Dn, CTLn↑↓	50% to 50%	See Figure 2	2		11	ns

PARAMETER MEASUREMENT INFORMATION

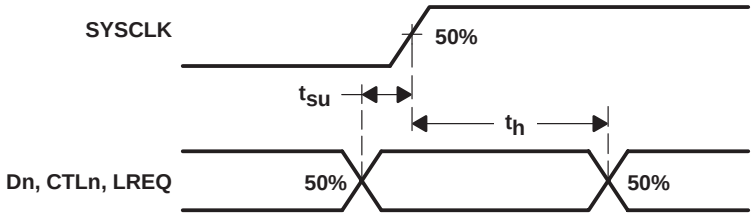


Figure 1. Dn, CTLn, LREQ Input Setup and Hold Timing Waveforms

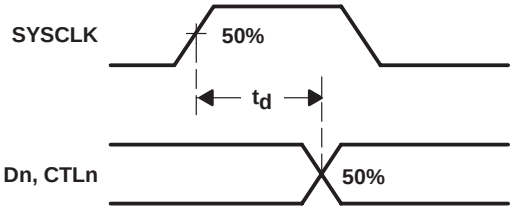


Figure 2. Dn and CTLn Output-Delay Timing Waveforms

APPLICATION INFORMATION

internal register configuration

The accessible internal registers of this device are listed in Table 1.

Table 1. Internal Register Configuration

Address	0	1	2	3	4	5	6	7
0000	Physical ID						R	CPS
0001	RHB	IBR	GC					
0010	SPD		Rev		NP			
0011	AStat1		BStat1		Ch1	Con1	Reserved	
0100	AStat2		BStat2		Ch2	Con2	Reserved	
0101	AStat3		BStat3		Ch3	Con3	Reserved	
0110	LoopInt	CPSInt	CPS	IR	Reserved			C
0111	Reserved							
1000	Reserved							

Table 2. Internal Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
AStat(n)	2	Read only	AStat contains the line state of TPAn. The status is indicated by the following: 11 = high-impedance state 01 = 1 10 = 0 00 = Invalid data state. Power-up reset initializes to this line state. This line state is also output during transmit and receive operations. The line state outputs are generally valid during arbitration and idle conditions on the bus.
BStat(n)	2	Read only	BStat contains the line state of TPBn. The status is indicated by the following: 11 = high-impedance state 01 = 1 10 = 0 00 = Invalid data state. Power-up reset initializes to this line state. This line state is also output during transmit and receive operations. The line state outputs are generally valid during arbitration and idle conditions on the bus.
C	1	R	Bus manager capable. C indicates the state of the Bus Manager Capable input. When set, this bit is used by the TSB21LV03 to specify in the Self-ID packet that the node is Bus Manager Capable.
Ch(n)	1	Read only	When Ch = 1, the port is a child, otherwise it is a parent. This bit is invalid after a hardware reset or a bus reset until tree-ID processing is completed.
Con(n)	1	Read only	Con indicates the connection status of the port. When Con = 1, the port is connected, otherwise it is disconnected. This bit is set to 1 by a hardware reset and is updated to reflect the actual cable connection status of the port during bus reset. The TSB21LV03 contains connection debounce circuitry that prevents a new cable connection on a port from initiating a bus reset until the connection status has been stable for at least 335 ms. A cable disconnect initiates a bus reset immediately. After a hardware reset, the TSB21LV03 sets the connection status of all ports to 0. The TSB21LV03 proceeds with the bus reset, tree-ID, and Self-ID, but with all ports considered to be disconnected child ports. The TSB21LV03 can not transmit any signals on the serial bus ports during this time. The TSB21LV03 does report itself as root with a physical address of 00h at the completion of Self-ID. If any port is actually connected, after the debounce delay, the TSB21LV03 initiates another bus reset, which proceeds normally with interaction between the TSB21LV03 and its peer nodes.

APPLICATION INFORMATION

Table 2. Internal Register Field Descriptions (continued)

FIELD	SIZE	TYPE	DESCRIPTION
CPS	1	Read only	Cable power status (CPS) contains the status of the CPS input terminal. When cable power voltage has dropped too low for reliable operation, CPS is reset (0). CPS is included twice in the internal registers to expedite handling of the CPSInt.
CPSInt	1	Read/ Write	CPSint indicates that a cable power status interrupt has occurred. This interrupt occurs whenever the CPS input goes low. The interrupt indicates that the cable power voltage has dropped too low to ensure reliable operation. This bit is cleared (0) by a hardware reset or by writing a 0 to this register. However, if the CPS input is still low, another cable-power status interrupt immediately occurs.
GC	6	Read/ Write	The gap count (GC) register sets the fair and arb-reset gap times. The gap count may be set to a particular value to optimize bus performance. Typically, the gap count should be set to 2 times the maximum number of hops on the bus and should be set to the same value for all nodes on the bus. The gap count can be set by either a write to this register or by reception or transmission of a PHY_CONFIG packet. The gap count is reset to 3Fh after a hardware reset or after two consecutive bus resets without an intervening write to the gap count register (either a write to the gap count register by the LLC or a PHY_CONFIG packet).
IBR	1	Read/ Write	When set, initiate bus reset (IBR) causes the current node to immediately initiate a bus reset. IBR is cleared (0) after a hardware reset or a bus reset.
IR	1	Read/ Write	IR indicates that the last bus reset was initiated in this TSB21LV03 phy. This bit is also included in the Self-ID packet.
LoopInt	1	Read/ Write	LoopInt indicates that a configuration loop timeout has occurred. This interrupt occurs when the arbitration controller waits for too long a period of time during tree-ID. This interrupt can indicate that the bus is configured in a loop. This bit is cleared (0) by a hardware reset or by writing a 0 to this register bit.
NP	4	Read only	NP contains the number of ports implemented in the core logic (not the number of ports actually on the device). For the TSB21LV03, NP is set to 0011b.
Physical ID	6	Read only	Physical ID contains the physical address of the local node. The physical ID defaults to 09h after a hardware reset or a bus reset until the Self-ID process has been completed. A complete Self-ID is indicated by an unsolicited status transfer of the register 0 contents to the LLC.
R	1	Read only	R indicates whether the current node is the root node or not. This bit is cleared (0) on a hardware reset or a bus reset. This bit is set during tree-ID when the current node is root.
Rev	2	Read only	The revision (Rev) bits indicate the design revision of the core logic. For the TSB21LV03, Rev is set to 00.
RHB	1	Read/ Write	When set, the root hold-off bit (RHB) instructs the local node to try to become the root node during the next bus reset. RHB is reset (0) during a hardware reset and is not affected by a bus reset.
SPD	2	Read only	The speed (SPD) bits indicates the top signaling speed of the local port and for the TSB21LV03 is set to 01b.

APPLICATION INFORMATION

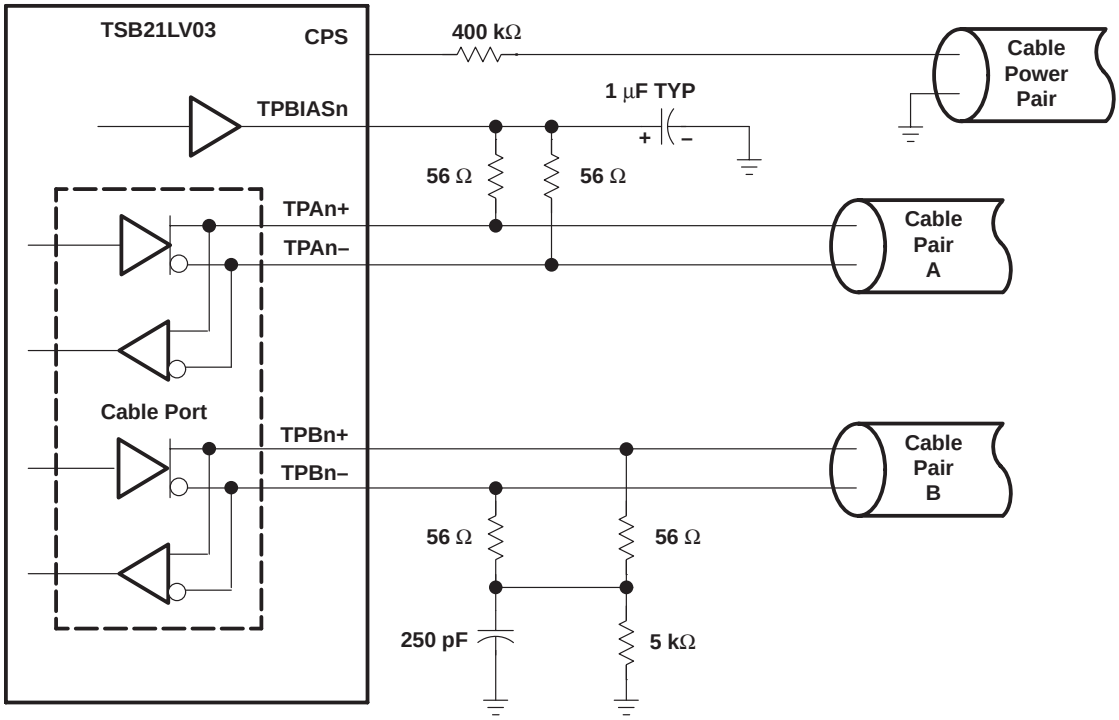


Figure 3. Twisted-Pair Cable Interface Connections

APPLICATION INFORMATION

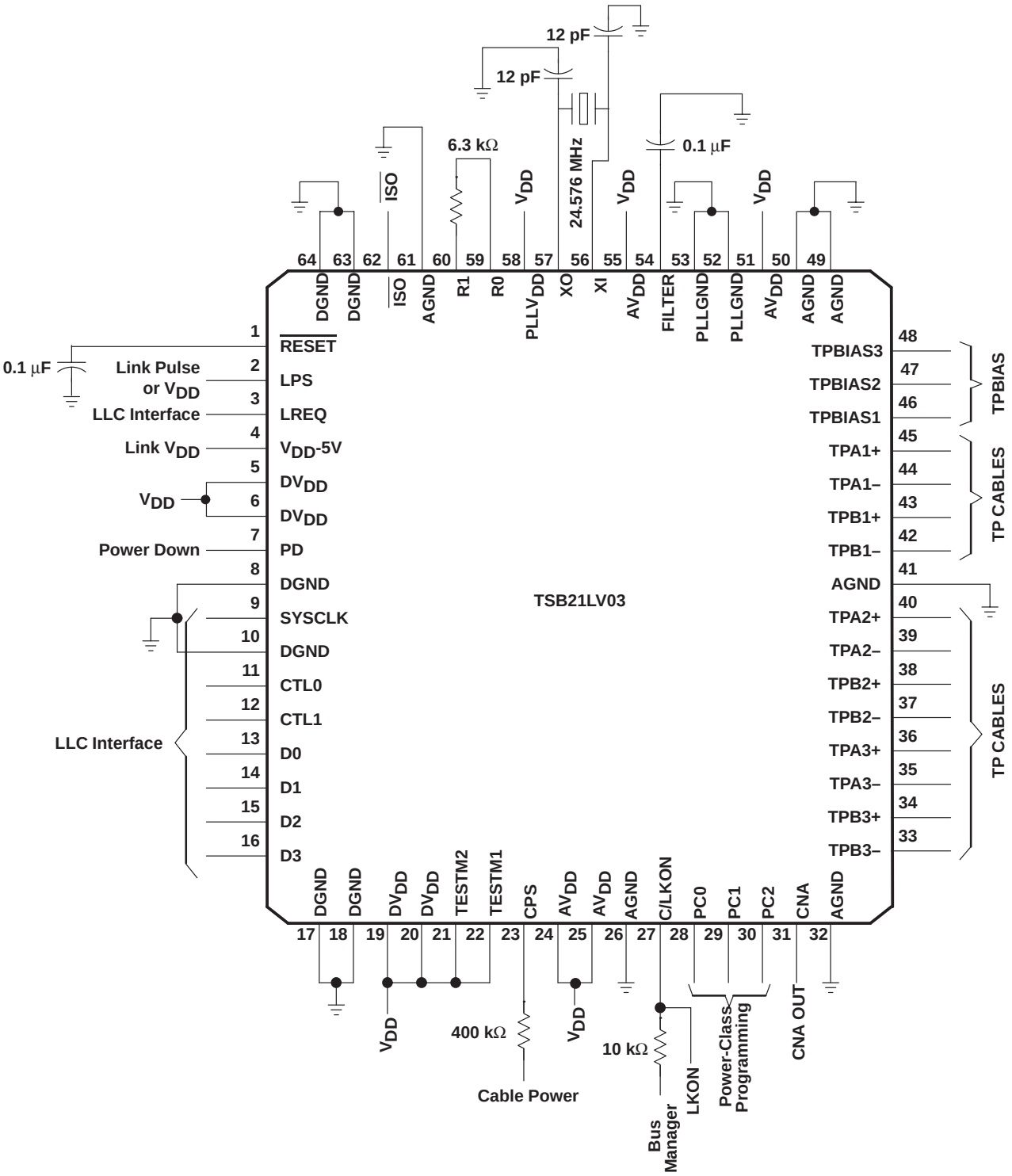


Figure 4. External Component Connections

APPLICATION INFORMATION

galvanic isolation

The IEEE 1394-1995 cable is designed to transmit and receive data at various data rates and also to source and/or sink power to/from remote nodes. This allows remote nodes that either do not have their own source of power or have their power turned off to continue to function in the IEEE 1394-1995 network. Since multiple nodes are allowed to source power connected together,simultaneously, this can cause grounding problems in the system if galvanic isolation between nodes is not handled properly. This section describes the three requirements set forth in IEEE 1394-1995 for isolation:

- Shield termination
- Cable power isolation
- Signal isolation

The majority of this section is dedicated to Texas Instruments patent-pending signal isolation method.

the need for isolation

Due to the distances allowed between nodes in an IEEE 1394-1995 network, different nodes on the network could be plugged into ac outlets that are in different ground domains, commonly referred to as green-wire grounds. The potential difference between these grounds can be dc, ac at 60 Hz along with its harmonics, and various noise components. If these grounds are connected together by the 1394 cable logic ground or shielding, a ground loop exists and current flows into the cable. These ground-loop currents can have several negative effects on the 1394 network, which includes degradation of data signals on the cable, excessive EMI from the cable, ground currents high enough to damage components in the system, and if the potential difference is large enough, a personal shock hazard. Figure 5 illustrates how the different ground domains might be connected together in two nodes of an IEEE 1394 network.

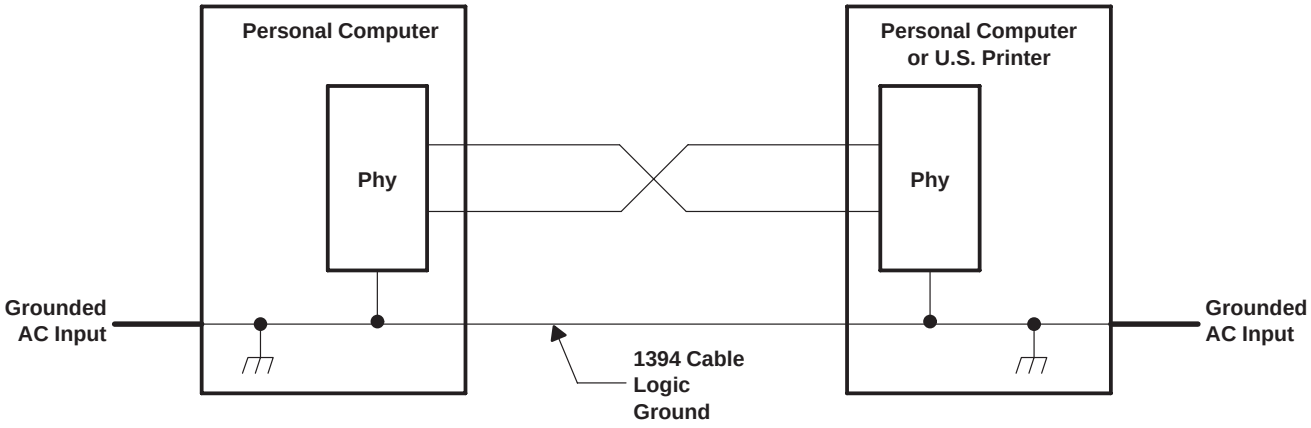


Figure 5. No Galvanic Isolation

To avoid this problem there are three electrical isolation requirements described in Annex A.4 of the IEEE 1394-1995 standard that should be followed for proper operation and safety of the serial bus. They deal with isolation of cable shielding, signal line isolation, and power line isolation.

Some systems may not have either a signal-line or power-line isolation problem. Consumer equipment typically uses a two-prong plug and a transformer in the power supply. For this type of system, isolation is inherent in the isolated power supply and no further isolation is required (see Figure 6). Since the IEEE 1394-1995 network is not connected to a green-wire ground, different ground domains do not pose a problem.

APPLICATION INFORMATION

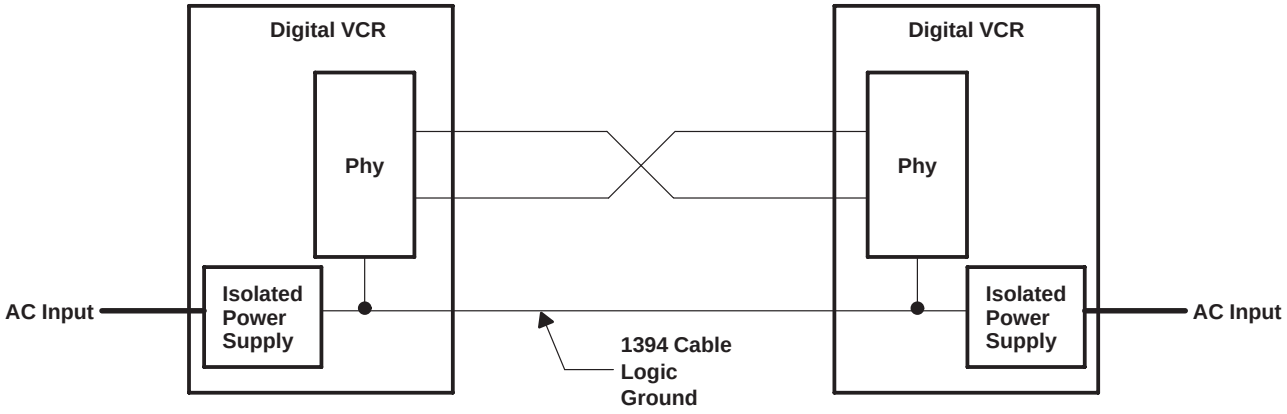


Figure 6. Isolation By Way of Isolated Power Supplies

When a camera is powered only from the IEEE 1394-1995 cable, it would not normally be connected to a green-wire ground and probably would not require isolation to be incorporated in this particular node configuration (see Figure 7).

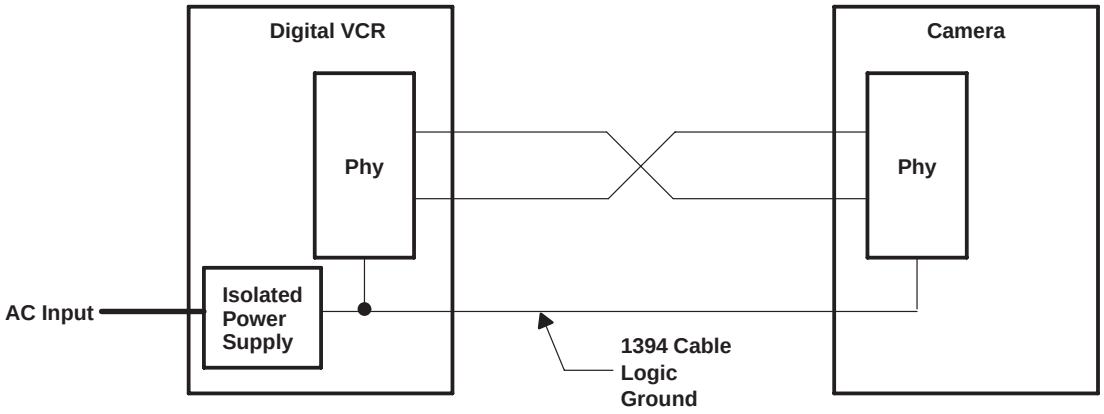


Figure 7. Leaf Node Not Requiring Isolation

In the case of a peripheral that is battery powered and using the 4-signal wire audio/video cable where there is no cable-power logic ground or cable-power wire in the 1394 cable, it probably would not be connected to a green-wire ground. However, there is still the potential that a battery- or cable-powered leaf node may be grounded through some accessory device. Figure 8 shows an example where the shield isolation is not implemented correctly.

APPLICATION INFORMATION

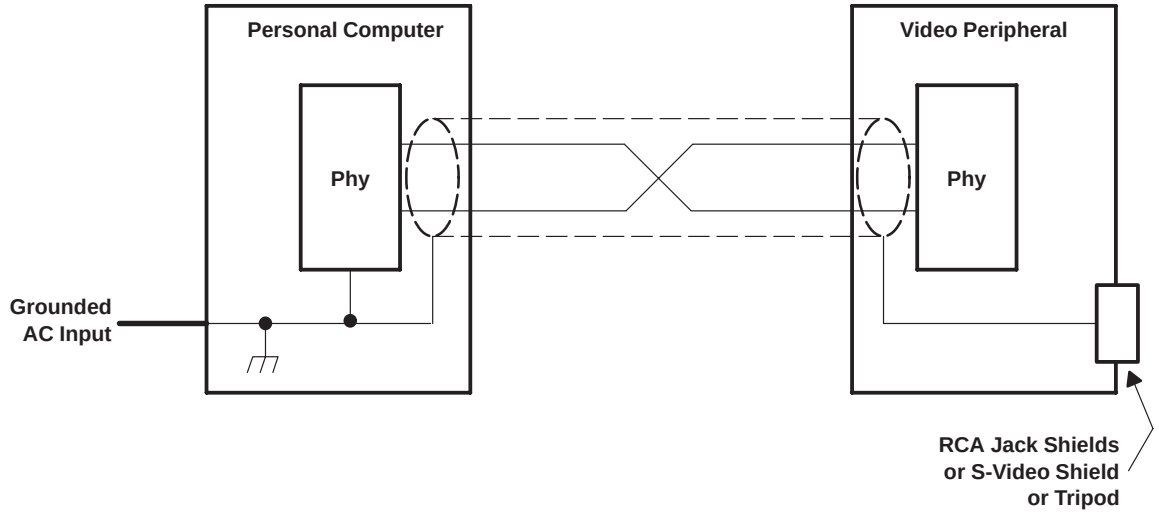


Figure 8. Potential Problem Due To Incorrect Shield Termination

Each node implementing IEEE 1394-1995 must be looked at independently to determine if isolation is required for that particular application. When it is required the following section should help in determining the best method of achieving the required isolation. There are three electrical isolation requirements described in Annex A.4 of the IEEE 1394-1995 standard that should be followed for proper operation and safety of the serial bus. They deal with isolation of cable shielding, cable-power isolation, and signal-line isolation. The cable shield isolation is specified in paragraph 4.2.1.4.8 of IEEE 1394-1995 and an example is shown in Figure 3–30 of the standard. It nominally consists of connecting the outer cable shield to chassis ground through a parallel combination of a 1-MΩ resistor and a 0.1-μF capacitor to provide a relatively high-impedance coupling at low frequencies and a relatively low-impedance coupling at high frequencies. Cable power is described in section A.4 of IEEE 1394-1995 with explanation and examples. Basically, when a node is going to source cable power, it must use an isolating supply to provide that power. This supply can be dedicated to supplying cable power (see Figure 9) or it can be the isolated supply of the entire node (see Figure A–2 of IEEE 1394 draft revision 8.0v2). The remainder of this document addresses signal-line isolation.

IEEE 1394-1995 phy-LLC interface isolation

Annex A in the IEEE 1394-1995 standard discusses the various places that galvanic isolation can be implemented when necessary to achieve galvanic isolation of the node. One of the most cost effective places to isolate a node is at the phy-LLC interface due to the relatively small number of signals that need to be isolated. Annex J of the IEEE 1394-1995 standard illustrates two techniques to achieve phy-LLC galvanic isolation. One method uses capacitive-isolation circuitry and the other uses a transformer-isolation circuit on each phy-LLC signal. The capacitive isolation-circuit is able to galvanically isolate up to the working voltage of the capacitors used in the circuit. The transformer circuit would typically be able to galvanically isolate to higher voltage levels due to its generally higher voltage capability between primary and secondary windings.

The phy-LLC interface consists of the following signal lines: LLC request (LREQ), system clock (SYSCLK), two interface control lines (CTL0 and CTL1), and up to 8 data lines (D0 – D7) plus several additional signals that may or may not require galvanic isolation depending upon the design of the system. These additional signal lines that may require isolation on Texas Instruments phys are the reset input ($\overline{\text{RESET}}$), LLC power status (LPS), power down (PD), configuration manager contender input with link-on output (C/LKON), and cable not active (CNA).

APPLICATION INFORMATION

Figure 9 shows a capacitively coupled phy and LLC that uses the capacitive-isolation circuit described in Annex J of the standard. Each bidirectional signal requires the network shown in Figure 9. A typical application for this type of design would be a host computer with an IEEE 1394-1995 port that is connected to a green-wire ground through a nonisolated power supply and a three-wire ac plug. Note that since the machine power supply is not isolated, an isolating dc/dc converter is required to isolate the host power domain from the cable power domain powering the phy. In these examples it is assumed that the dc/dc converter is internally protected from sinking any current supplied from the cable power domain. The terminal numbers shown on the 1394 connector are according to Table 4–3 of IEEE 1394 revision 8.0v2. The cable shield terminations labeled 7 and 8 are actually the connector tabs connected to the metal shell of the printed-wire board (PWB) 1394 connector.

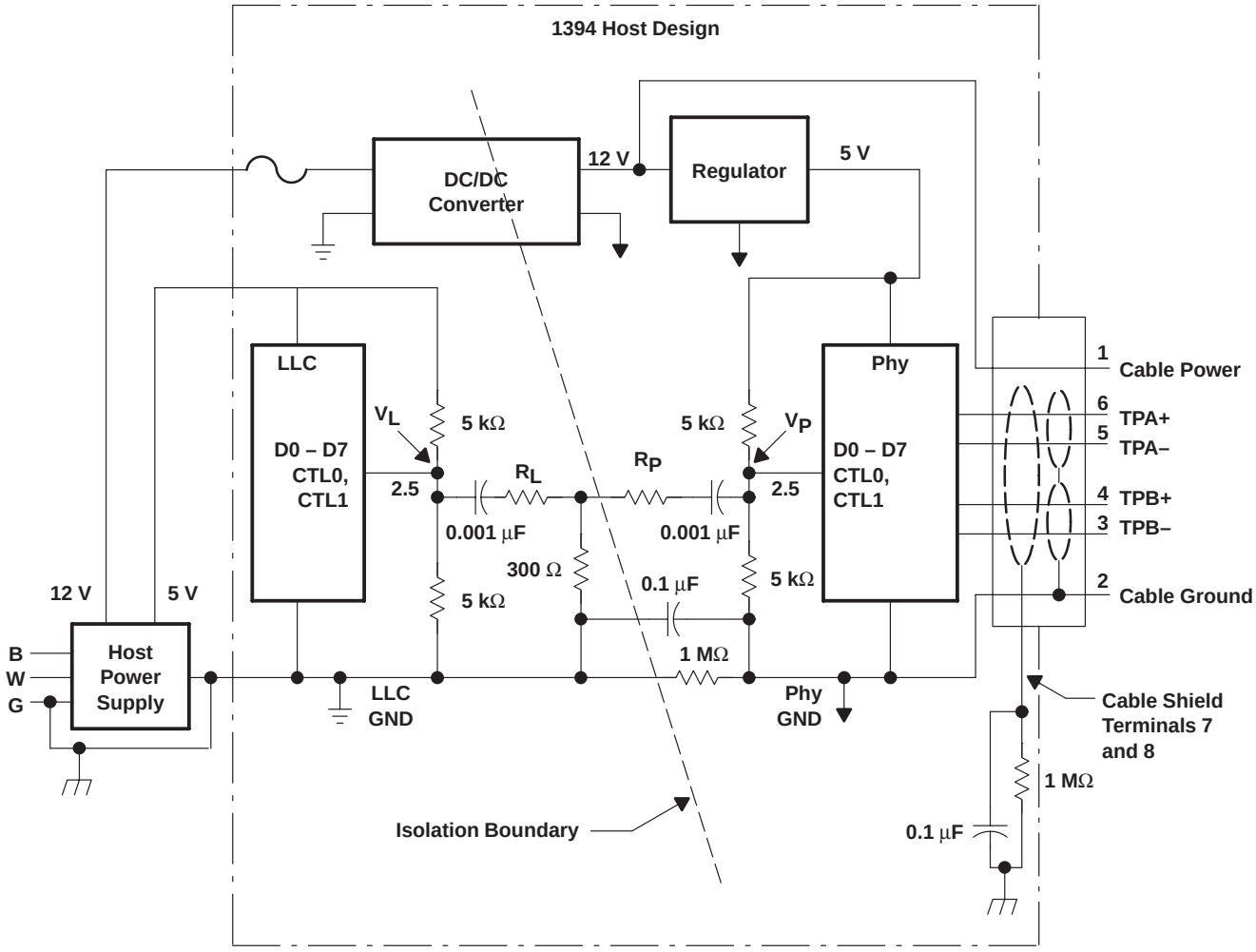


Figure 9. IEEE 1394-1995 Annex J Capacitive Isolation

APPLICATION INFORMATION

The capacitive-isolation circuit and the transformer-isolation circuit operate basically the same. In order for signals to cross the isolation boundary, the driving side output must first be differentiated. Whenever the line state changes, the phy-LLC interface signal is driven to the new state. When the line state remains constant for more than one clock period, the signal is sent into a high-impedance state. When the output signal is at the high-impedance state, the input signals quickly return to $V_{DD}/2$. The differentiation is handled internally in the phy and LLC integrated circuits. Figure 10 shows the logical line state at the output buffer, V_L, when the LLC is driving, and V_P when the phy is driving.

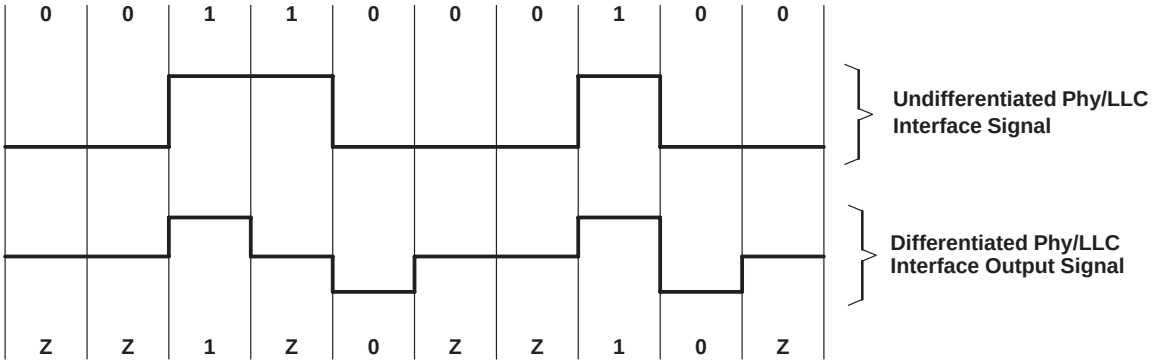


Figure 10. Differentiation of Interface Signal ($\overline{ISO}$ Terminal low)

The signal at the input buffer is shown in the Figure 11. This waveform is for a 5-V device. A 3-V device would have the signals ratioed down accordingly.

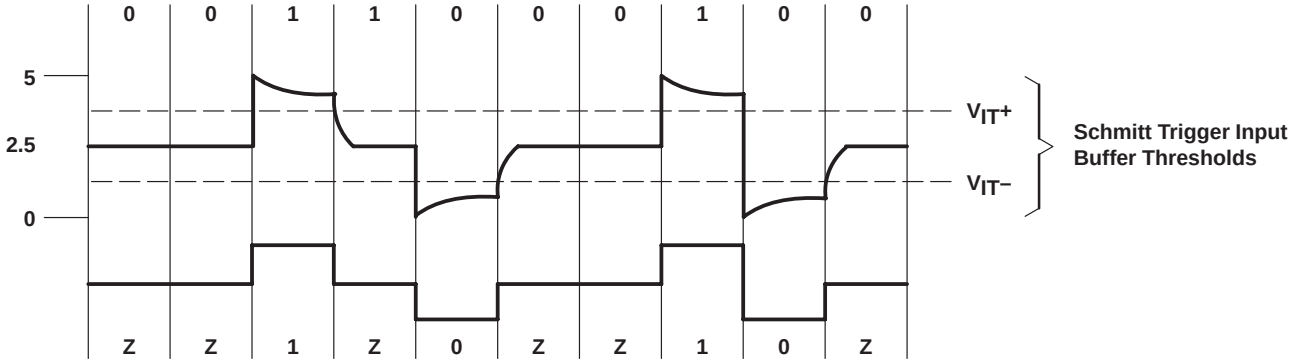


Figure 11. Line Levels of Differentiated Interface Signals

The input buffer output remains in its previous state until a hysteresis threshold is crossed, thus recreating the original undifferentiated signal. To turn the $\overline{ISO}$ terminal on for Texas Instruments devices, it must be held to a low logic level.

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There are several design challenges with transformer-isolation circuit of galvanic isolation barrier. They are:

- The input thresholds must be maintained accurately at $V_{DD}/2$.
- The input hysteresis must be fairly wide and it too must be maintained accurately.
- Two capacitors and seven resistors are required for each bidirectional line to be isolated. This adds to component costs and board space.
- Differentiation circuitry is required in each output buffer, and circuitry to decode the differentiated signal must be added to each input buffer.
- Supply current in the input buffer can be quite high because the input is normally sitting at midsupply. When using CMOS-type input buffers, as much as a mA of supply current can be wasted in each input.
- Supply current is wasted in the external bias resistors that are connected between the supply rail and ground.
- The propagation delay through this isolation circuit can typically be 2 ns to 3 ns. This delay reduces the setup and hold time windows allowed for each input.
- Noise margins on the input buffer are very low. The noise margin is the difference between the maximum threshold level and the minimum hysteresis level on the high side and the difference between the minimum threshold level and the maximum hysteresis level on the low side.
- During power up of either the phy, the LLC, or both, care must be taken to ensure that the output state and the input state are synchronized; in other words, ensure that the voltage levels on each side of the isolation capacitor represent the same logic state. Input power-up glitches can cause output and input states to be out of synchronization causing communication errors between the phy and the LLC. As data is passed through the isolation barrier, the output and input eventually synchronize, but there is the possibility of locking up the system before synchronization occurs.

Texas Instruments bus holder galvanic isolation barrier

Texas Instruments patent-pending bus-holder galvanic isolation technique simplifies most of the previously mentioned design challenges. Bus-holder circuits are required on the input side (both sides when bidirectional) of the single capacitor that forms the galvanic isolation barrier. The bus-hold function consists of a CMOS-buffer stage with a high-resistance feedback path between its output and its input. This prevents bus lines from floating without using pullup or pulldown resistors. The high-impedance inputs of these internal CMOS buffers are connected to the input terminals of the device. The feedback path on the internal buffer stage keeps a bus line tied to the bus holder at the last valid logic state generated by an active driver. Active bus-hold circuitry typically holds unused or floating-data inputs at valid logic levels and eliminates the need for pullup or pulldown resistors. These bus holders can be integrated into the phy and LLC devices at extremely low cost. If either the phy, the LLC, or both does not have the bus holders integrated, external bus holders can be implemented. Bus holder ICs or ICs with bus-holder inputs are available commercially that are capable of performing this function. TI plans to integrate bus holders internally on future revisions of its phys and LLCs. Figure 12 shows a typical implementation using phy and LLC devices with internal bus holders.

APPLICATION INFORMATION

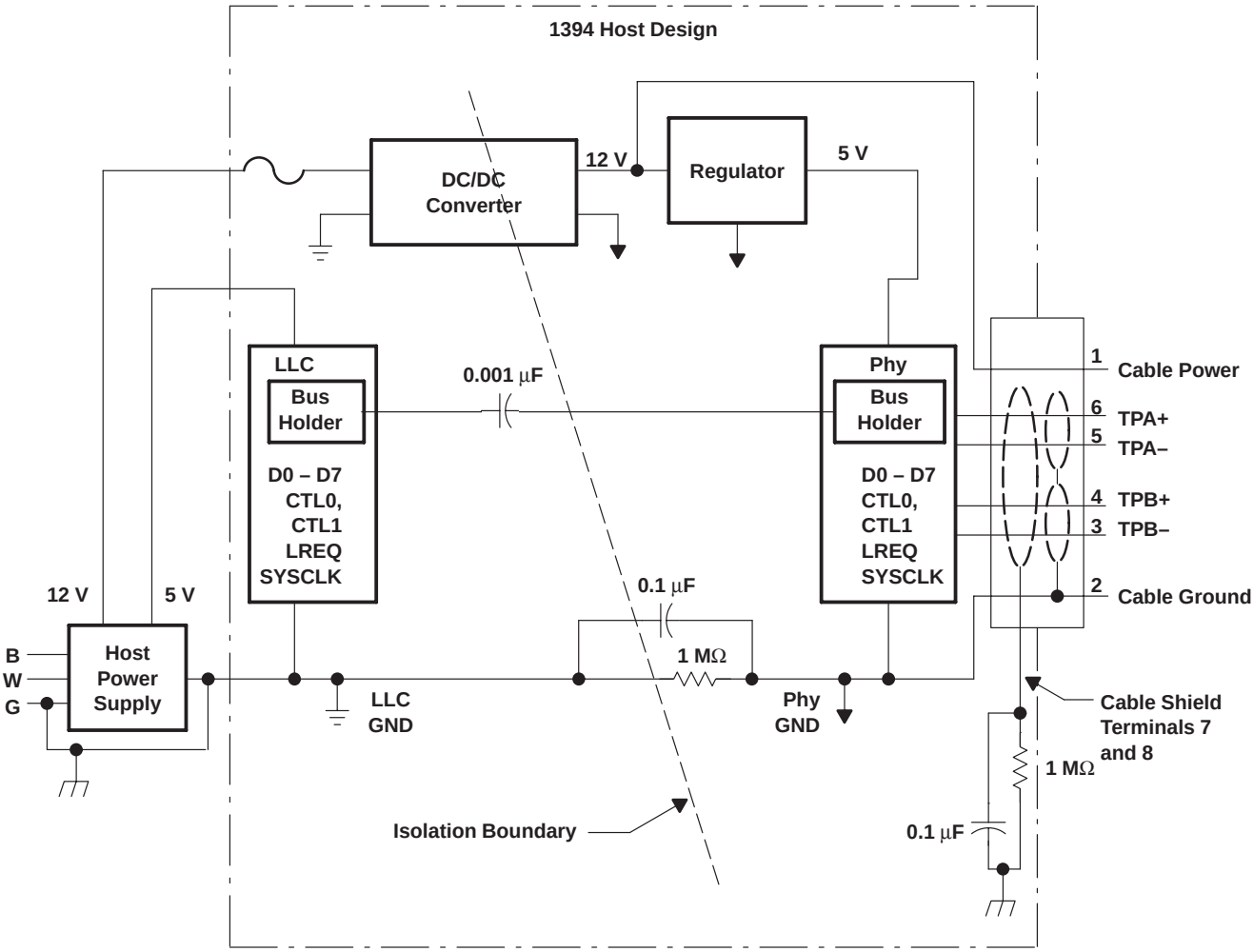

Figure 12. Internal Bus-Holder Isolation

The bus-holder isolation technique is cost effective and eliminates most of the components required for the implementation of galvanic isolation described in the IEEE 1394-1995 High Performance Serial Bus Standard in Appendix J.6. Only one 0.001-µF capacitor per signal line is required. The principal of operation is straight forward. When the output node switches states, the charge on the capacitor is maintained, and voltage on the input node is pulled in the same direction as the output node. The bus holder then maintains the input state until the output makes another transition. This allows normal input buffers to be used that do not require critical threshold values. Critical hysteresis levels also are not required. Board area and external component cost is reduced. Differentiation circuitry in the output buffers is not needed. High supply currents in the input buffers are eliminated. Supply current wasted in the external bias resistors is eliminated. The propagation delay through the single isolation capacitor is extremely small. And finally, noise margins on the input buffer is essentially the same as for the nonisolated CMOS signal levels. Note that since no differentiation is needed the $\overline{\text{ISO}}$ terminal on TI devices needs to be held in a high logic state (differentiation is turned off) to correctly function with bus-holder isolation.

When higher voltage isolation is required than can be provided by the working voltage of a single capacitor, then multiple capacitors can be implemented in series. The working voltages then increase, but the capacitance values of each individual capacitor must be increased to maintain the same voltage for the series combination.

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As with the isolation method described in the IEEE 1394-1995 standard, care must be taken to ensure that the input and output are synchronized during power up of either the phy, LLC, or both. This can be accomplished internally in some cases with the LREQ terminal. During power up reset the LREQ input of the phy can be pulled low, which should also be the driving state of the LREQ output of the LLC device during power up. The LREQ terminal has the potential of hanging the phy-LLC interface if the phy senses a high input while the LLC continues driving low after a power up of either or both devices.

Another phy-LLC signal with the potential to cause problems when the states across the phy-LLC interface do not match is the LPS signal. For instance, when attempting to pass the LPS signal in as a dc signal across a bus-holder and capacitor-type isolation, there are challenges to be met. If the LLC powers up first, while the phy was still powered down, the isolation capacitor could have a charge induced on it. In a 3-V system the LLC side of the capacitor would be charged to 3 V while the phy side remained at ground potential. When the phy was then powered up, the capacitor and the bus holder could keep the LPS input signal at the low level and the states would not be synchronized. This would then cause the phy to disable all phy-LLC output terminals, and the node could lock up. By transitioning the state the logic levels on each side of the capacitor, the states can be synchronized. In the LPS example, a case has been hypothesized where the LLC side of the isolation capacitor is logic high while the phy side is low. If the LLC then drives a low level, the phy side of the capacitor also tries to swing the same voltage down . However since the phy side of the isolation capacitor is already in the low state, the voltage goes negative until the clamping diode is turned on. This diode to ground clamps the voltage and dissipates the charge on the capacitor bringing the state on each side of the isolating capacitor into synchronization. For the dc-type signals, these transitions do not cause a loss of information. However for the ac signals (i.e., LREQ) the first bit of the transmission is lost, making this method of achieving synchronization only useful if a dummy transition of the signal can be generated and tolerated. A much better approach for the LPS signal would be to use an ac signal across the bus holder and capacitor isolation. The TI physical-layer device LPS terminal recognizes a square wave of between 220-kHz and 5.5-MHz as the signal that the LLC is on. The generation of this square-wave signal would need to be designed such that whenever the LLC is powered up, the signal is on. On the TSB12C01A and TSB12LV31 LLC devices, this signal is supplied as the power on terminal (see Figure 13).

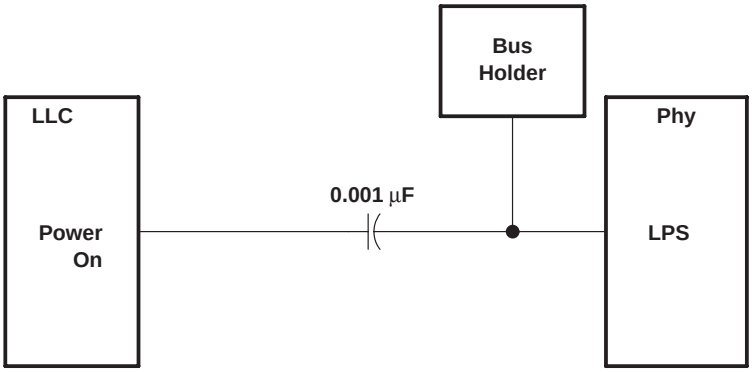


Figure 13. External Bus-Holder Implementation for AC LPS Line

Since the TSB12LV21 does not supply a square-wave signal, the system designer needs to provide either an ac or dc signal to the phy if this feature is desired. A TIL191A optoisolator can provide a square-wave signal in a dc form for slightly more than $0.30 a line (see Figure 14).

APPLICATION INFORMATION

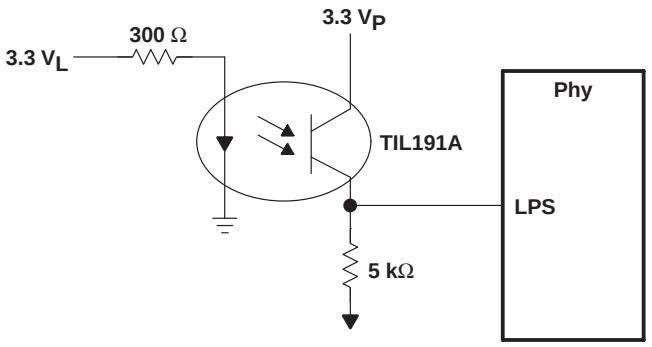


Figure 14. Implementation of Isolation for DC LPS Signal Using TIL191A Optoisolator

A note on optoisolators, it is recommended that optoisolators only be used on slow signals (times in ms) like $\overline{\text{RESET}}$ or PD that are essentially dc signals. There currently are no known optoisolators that have a large enough bandwidth and low enough latency to meet the requirements of the data and control lines of the phy-LLC interface. Since each system is different and requires different sequences associated with startup and power down, it falls back to the system designer to be responsible to check all possible conditions that can occur on the phy-LLC interface to ensure that this type of a nonsynchronized state either does not occur or is resolved correctly.

Table 3. Phy-LLC Interface Initial Signal States

SIGNALS	PHY DEVICES†			LLC DEVICES†		
	TSB21LV03	TSB11LV01	TSB11C01	TSB12C01A	TSB12LV21	TSB12LV31
Phy-LLC Data	L	L	L	I	I	I
Phy-LLC CTL	L	L	L	I	I	I
SCLK	49.152 MHz	49.152 MHz	49.152 MHz	I	I	I
LREQ	I	I	I	L	L	L
LPS	L	I	I	N/A	N/A	N/A
Power-On	N/A	N/A	N/A	BCLK/32	N/A	BCLK/32
$\overline{\text{RESET}}$	I	I	I	I	I	I
PD	I	I	N/A	N/A	N/A	N/A
CMC	I	I	I	N/A	N/A	I
Link-On	Z	Z	Z	N/A	N/A	N/A
CNA	Port State	Port State	N/A	N/A	N/A	N/A
GPIO	N/A	N/A	N/A	N/A	Z	N/A

† H – driven high, I – Input, L – driven low, N/A – not applicable, Z – high-impedance state

When the phy and/or the LLC device is not designed with internal bus holders, this bus-holder isolation scheme can still be implemented with external bus holders. Figure 15 illustrates a circuit implementation where neither the phy or the LLC have internal bus holders. External bus holders are provided on each side of the isolation barrier by SN74ACT1071 10-bit bus termination array with bus-holding function ICs. One SN74ACT1071 on each side of the isolation barrier would provide up to ten signals with bus holding functions.

APPLICATION INFORMATION

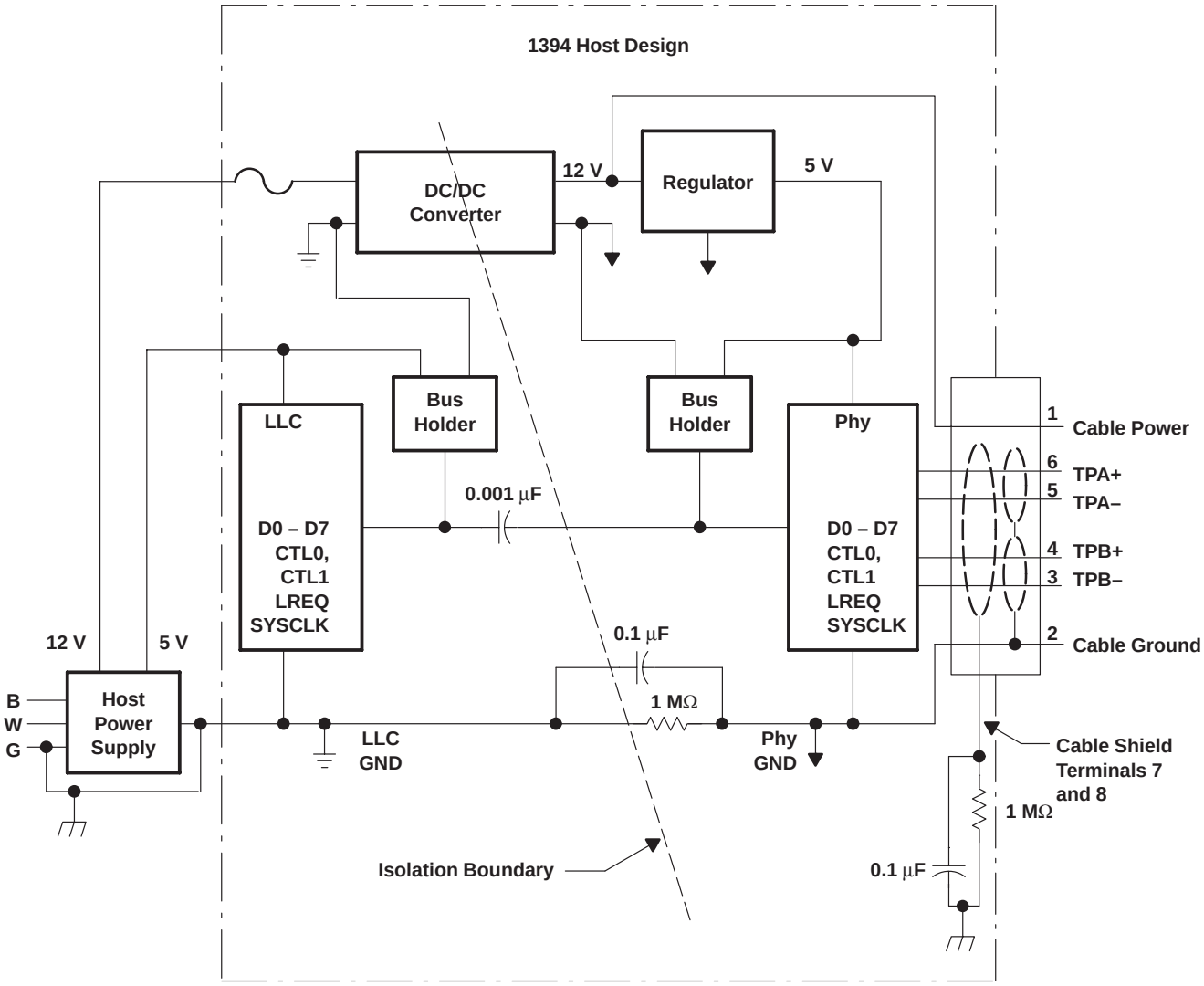


Figure 15. External Implementation of Bus-Holder Isolation

When either the phy or the LLC had internal bus holders present, then the device without bus holders would require an external bus holder to be implemented on its side of the isolation barrier. There are several choices for external bus holders. Depending on the application, the least expensive approach can be to use the inputs to buffer circuits that have bus holders built into their inputs. Several alternative devices that have bus holder circuits on the inputs are available. For 3.3-V applications, the SN74LVCH244, SN74LVCH245, and SN74LVCH16244 are available. For 5-V applications, the SN74ABTH245, SN74ACT1071, or SN74ACT1073 are available. Figure 16 and Figure 17 show the implementation of the bus-holder isolation for a monodirectional signal.

NOTE:

A bus holder is only required on the receiving side of the isolation capacitor, regardless of whether that side is in the LLC power domain or the phy power domain.

APPLICATION INFORMATION

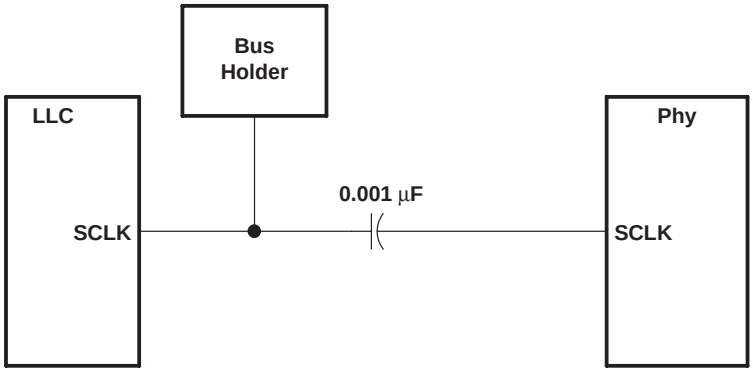


Figure 16. External Implementation of Bus-Holder Isolation for SCLK Line

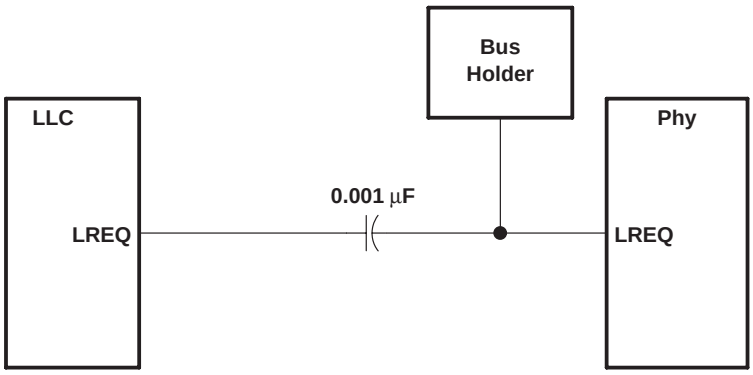


Figure 17. External Implementation of Bus-Holder Isolation for LREQ Line

The bus-holder isolation works well on the other ac signals that may be used in the phy-LLC interface. As noted above the LPS signal can be a square wave of between 220 kHz and 5.5 MHz. The LPS signal easily passes through the bus-holder isolation network from the LLC to the phy. The same can be said of the link-on signal, with a frequency of 6.114 MHz it also can use the bus-holder isolation to pass from the phy to whatever digital circuitry is implemented to use this signal to turn on the LLC.

Several other useful dc signals or functions can be implemented across an isolation barrier when required. The CNA signal is a dc signal and while it can be transmitted directly across the isolation barrier using bus holders or optoisolators, the same information is available in the phy register space as the connected bit in the individual port status registers. This information can be transferred across the isolation barrier on the data lines using a phy register read request, unless the CNA signal is being used in the LLC power domain to turn on and off the phy using the power-down line. When this is the case, the CNA electrical signal must be brought across the isolation barrier.

All of Texas Instruments low-voltage phys have a power-down signal (PD) to enable a power-saving mode for battery operation. This mode generates a dc signal since battery-powered devices are usually leaf nodes not typically connected to two different power domains. The PD signal can be transmitted across the isolation interface using either bus-holder isolation or optoisolators (see Figure 18).

APPLICATION INFORMATION

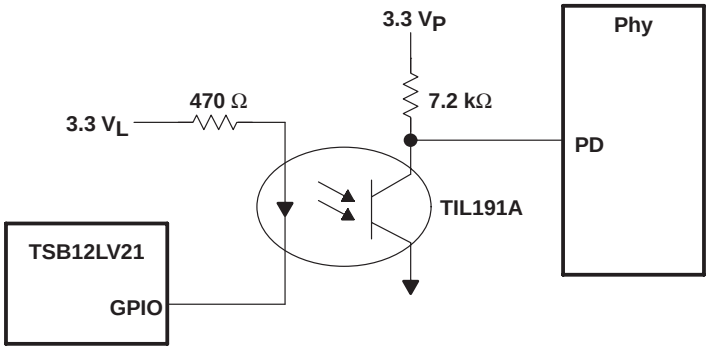


Figure 18. Isolation of PD Signal Using An Optoisolator

The power-up reset of TI phy devices is designed to be used with a 0.1-μF capacitor hooked to the reset terminal. This provides the necessary delay (2 ms minimum) to allow the analog circuitry to reach a quiescent state before suppling power to the rest of the device. Since no connection to the LLC is required, no isolation is required. While the $\overline{\text{RESET}}$ signal may be transmitted across the isolation interface using bus-holder isolation or optoisolation, it typically would not need to be. When it is required to have control over the phy device reset from the LLC power domain, an example implementation is shown in Figure 19. The $\overline{\text{RESET}}$ line needs to be held low for a minimum of 2 ms and the LLC driver needs to be able to sink 11 mA.

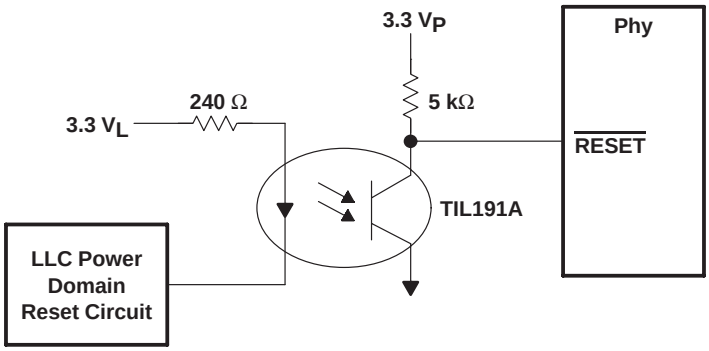


Figure 19. Optoisolator Isolation for Phy Reset Terminal

The current implementation of the configuration-manager contender (CMC) bit is as a terminal tied high or low on the phy. Since this can be set on the phy without need for a connection to the LLC, no isolation is required. However when control of the status of the configuration-manager contender bit state is desired from the LLC power domain, isolation may be accomplished by using a combination of bus-holder isolation and an optoisolator as shown in Figure 20. This signal isolation is complicated by the fact that it shares a terminal with the ac signal LKON. The top path is for the link-on signal from the phy to the LLC through an isolating capacitor with a bus holder on the receiving (LLC) side of the capacitor. The bottom path is to pass a dc signal to program the state of the CMC bit. This dc signal is isolated using an optoisolator. The output path of the optoisolator on the phy side contains an in-line resistor to dissipate the energy produced by the LKON signal without damaging the optoisolator. A pullup resistor is provided on the LLC side of the optoisolator to ensure that the power-on state of the configuration-management contender bit is low. The LVCH244 is needed in this configuration to source and sink the current required for the chosen optoisolator. It is assumed that a spare buffer is available if external bus holders are used and the inputs to LVCH244 are used to provide them.

APPLICATION INFORMATION

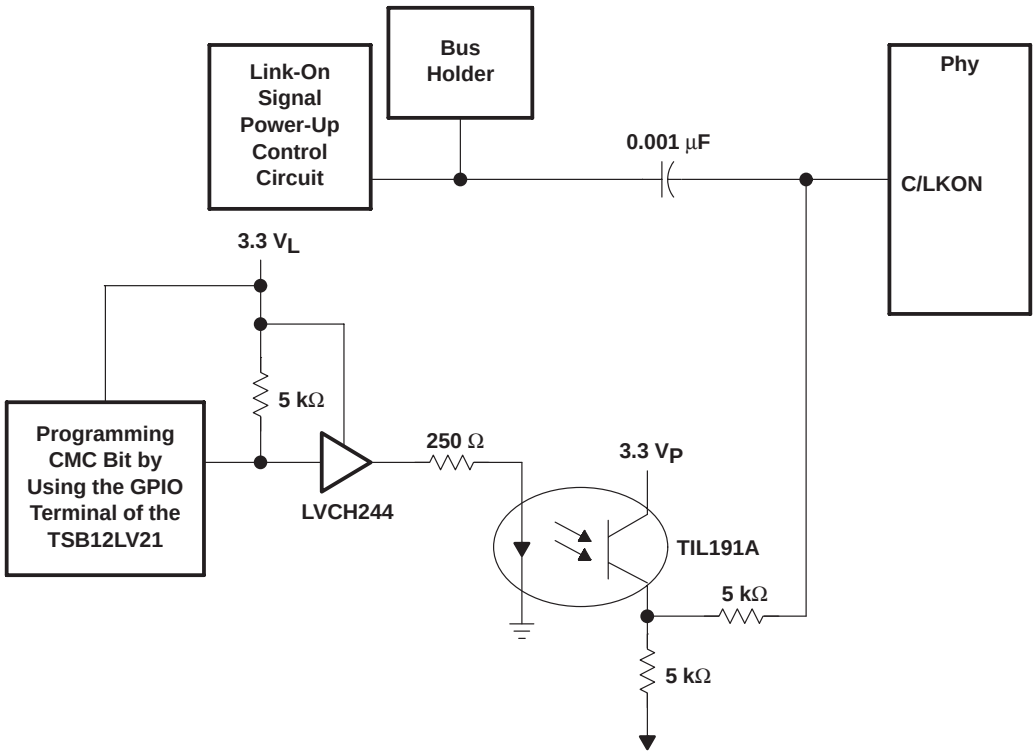


Figure 20. External Implementation of Bus-Holder Isolation for Phy Link-On Signal and Circuit for Setting CMC Bit (C/LKON)

APPLICATION INFORMATION

Table 4. Terminals That Need Isolation

TERMINAL	COMMENT
D0 – D7	Isolation circuitry required on data lines used (D0, D1 for S100; D0 – D3 for S200; D0 – D7 for S400)
CTL0, CTL1	Isolation circuitry required
LREQ	Isolation circuitry required
SCLK	Isolation circuitry required
LPS	Isolation circuitry required if implementing link-on packets. When not implementing link-on packets LPS can be tied high in the phy power domain to always have the phy-LLC interface enabled, but it puts incorrect LLC power status into Self-ID packet if LLC is powered down.
$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ only requires isolation circuitry if software control over hardware reset is required. Normally $\overline{\text{RESET}}$ is connected to a 0.1-μF capacitor in the phy power domain and resets itself upon power up, thus requiring no isolation circuit. Other means of resetting the phy include: ● Initiating a bus reset results in an almost complete phy layer reset ● The power down terminal on TI low-voltage parts powers down the entire chip except for the CNA circuit ● The LLC power status terminal, when pulled low, powers down the phy-LLC interface
PD	PD only requires isolation circuitry if software control over the power-down mode is required. When control is not required PD is normally pulled low in the phy power domain.
CNA	CNA only requires isolation circuitry when cable not active is used in the LLC power domain, for example, to determine what state to drive the PD terminal. CNA still operates when the phy is in power-down mode and gives LLC power domain circuitry an indication when a cable has been plugged into the phy and to power up or power down the phy. Otherwise CNA is not connected and the connected status of a phy port is determined by reading the phy registers
C/LKON	Isolation circuitry is required if implementing link-on packets. Otherwise C/LKON is not connected to LLC power domain.
CMC	CMC only requires isolation circuitry if software control over the state of the configuration-manager contender bit is required. When software control is not required it may be pulled high to be a CMC or low to not be a CMC in the phy power domain

The bus-holder isolation, as described previously, can be used with mixed voltage systems with modification. When the driving side is at a low-power-level device then the bus holders on the high-power-level receiving side pull a high logic level to the higher supply voltage rail. When the transition to the low side takes place, the 3.3-V swing may not be enough to pass the thresholds if 5-V bus holders are used on the receiving side. To compensate for this, a 3.3-V bus holder can be used on the inputs to the 5-V device (this requires the 5-V device to have TTL input thresholds). A diode chain can lower the voltage of the power supplied to the bus holder as shown in Figure 21. The low-voltage bus holder limits the voltage swing and the thresholds to be compatible with the swing induced by the low-voltage driver on the other side of the isolation capacitor. When the 5-V device (an LLC in Figure 21) has TTL inputs, the ≈3.2-V powered bus holder meets those thresholds.

APPLICATION INFORMATION

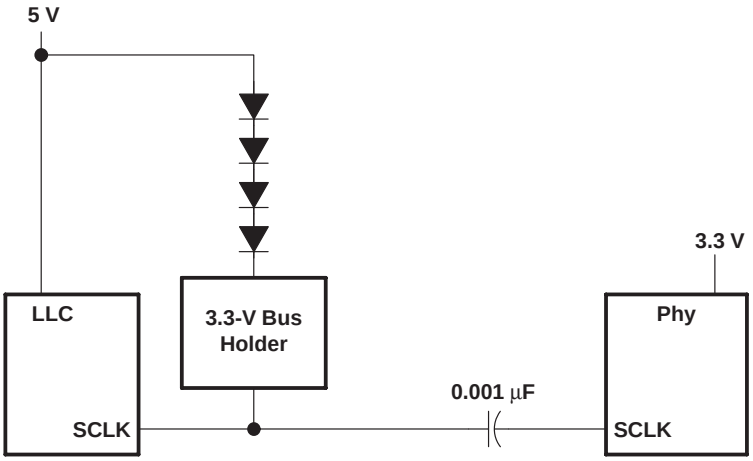


Figure 21. Isolated Mixed-Voltage System

Determination of whether a node requires galvanic isolation of IEEE 1394-1995 nodes is a node-by-node requirement of the system designer. Isolation of 1394 nodes requires three parts: cable shielding, cable-power isolation, and signal-line isolation. Cable shielding requires the correct termination of the cable outer shield with a parallel combination of a 1-MΩ resistor and a 0.1-μF capacitor. Cable power isolation requires isolation of the cable power supply when providing power, or keeping cable power physically separate when not providing cable power, or keeping cable power physically separate when not using cable power exclusively for the entire node (with no other outside connections). Texas Instruments recommends its bus-holder isolation technique for signal-line isolation. It is superior in cost and performance to the method described in Annex J of the IEEE 1394-1995 standard. Table 5 compares the aspects of the capacitive isolation shown in the informative Annex J of IEEE1394-1995 with the TI bus-holder isolation.

Table 5. Implementation Comparison

EXAMPLE COMPARISON FOR 200-Mbits/s NODE (DATA, CTL, LREQ, SYSCLK)			
PARAMETERS	**ANNEX J METHOD**	**TI METHOD**	**TI BUS-HOLDER BENEFITS**
External capacitors	14	8	Reduced PWB area Reduced complexity Reduced cost
External resistors	48	0	Reduced PWB area Reduced power Reduced complexity Reduced cost
Voltage swing	$V_{DD}/2$	Rail to rail	Better noise margin
Digital differentiaters on outputs	Required	None	Reduced complexity Reduced cost
Special threshold requirements	Required	None	Reduced complexity Reduced cost
Isolation network power drain	Holds input cells at $V_{DD}/2$	Method causes no impact	Minimal quiescent power drain No special input cell requirement Reduced cost
Hysteresis on inputs	Requires Schmitt triggers on inputs	None	Reduced complexity Reduced cost
Delay through network	Introduces 2-ns to 3-ns delay	Introduces near-zero delay	Fewer timing issues

PRINCIPLES OF OPERATION

The TSB21LV03 is designed to operate with a LLC such as the TI TSB12LV21, TSB12LV31, and TSB12C01A. These devices use an interface as described in Annex J of the IEEE 1394-1995 standard. Details of how the TSB12LV21, TSB12LV31, and TSB12C01A LLC devices operate are described in the LLC data sheets (i.e.,TSB12LV21, TSB12LV31, and TSB12C01A). The following paragraphs describe the operation of the phy-LLC interface.

The TSB21LV03 supports 100-/200-Mbit/s data transfer and has four bidirectional data lines, D0 – D3, crossing the interface. In 100-Mbit/s operation only D0 and D1 terminals are used. In 200 Mbit/s operation, all Dn terminals are used for data transfer. The unused Dn terminals are driven low. In addition, there are two bidirectional control lines CTL0 and CTL1, the 50-MHz SYSCLK line from the phy to the LLC, and the LLC request terminal LREQ from the LLC to the phy. The TSB21LV03 has control of all bidirectional terminals. The LLC is allowed to drive these terminals only after it has been given permission by the phy. The dedicated LREQ request terminal is used by the LLC for any activity that it wishes to initiate.

There are four operations that may occur in the phy-LLC interface: request, status, transmit, and receive. With the exception of the request operation, all actions are initiated by the phy.

When the phy has control of the bus the CTL0 and CTL1 lines are encoded as shown in Table 6.

Table 6. CTLn Status When Phy Has Control of the Bus

CTL0	CTL1	STATUS NAME	DESCRIPTION
0	0	Idle	No activity is occurring (this is the default mode).
0	1	Status	Status information is being sent from the phy to the LLC.
1	0	Receive	An incoming packet is being sent from the phy to the LLC.
1	1	Transmit	The LLC has been given control of the bus to send an outgoing packet.

When the LLC has control of the bus (phy permission) the CTL0 and CTL1 terminals are encoded as shown in Table 7.

Table 7. CTLn Status When LLC Has Control of the Bus

CTL0	CTL1	STATUS NAME	DESCRIPTION
0	0	Idle	The LLC releases the bus (transmission has been completed).
0	1	Hold	The LLC is holding the bus while data is being prepared for transmission or is sending another packet without arbitrating.
1	0	Transmit	An outgoing packet is being sent from the LLC to the phy.
1	1	Reserved	None

Request

When the LLC requests the bus or accesses a register that is located in the TSB21LV03, a serial stream of information is sent across the LREQ line. The length of the stream varies depending on whether the transfer is a bus request, a read command, or a write command. Regardless of the type of transfer, a start bit of 1 is required at the beginning of the stream, and a stop bit of 0 is required at the end of the stream. Bit 0 is the most significant bit, and is transmitted first. The LREQ terminal is required to idle low (logic level 0).

Table 8. LLC Bus-Request or Register-Access-Request Bit Length

REQUEST TYPE	NUMBER OF BITS
Bus request	7
Read register request	9
Write register request	17

PRINCIPLES OF OPERATION

For a Bus Request the length of the LREQ data stream is 7 bits as shown in Table 9.

Table 9. LLC Bus Request

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Indicates the beginning of the transfer (always 1).
1–3	Request Type	Indicates the type of bus request (see Table 12 for the encoding of this field).
4–5	Request Speed	Should be 00 for TSB21LV03 100-Mbit/s speed and 01 for 200-Mbit/s speed.
6	Stop Bit	Indicates the end of the transfer (always 0).

For a Read Register Request the length of the LREQ data stream is 9 bits as shown in Table 10.

Table 10. LLC Read Register Access

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Indicates the beginning of the transfer (always 1).
1–3	Request Type	Always a 100 indicating that this is a read register request.
4–7	Address	Identifies the address of the phy register to be read.
8	Stop Bit	Indicates the end of the transfer (always 0).

For a Write Register Request the Length of the LREQ data stream is 17 bits as shown in Table 11.

Table 11. LLC Write Register Access

BIT(S)	NAME	DESCRIPTION
0	Start Bit	Indicates the beginning of the transfer (always 1).
1–3	Request Type	Always a 101 indicating that this is a write register request.
4–7	Address	Identifies the address of the phy register to be written to.
8–15	Data	Gives the data that is to be written to the specified register address.
16	Stop Bit	Indicates the end of the transfer (always 0).

The 3-bit Request Type field has the values shown in Table 12.

Table 12. LLC Bus Request Type

LREQ1	LREQ2	LREQ3	NAME	DESCRIPTION
0	0	0	ImmReq	Immediate request. Upon detection of an idle, the LLC takes control of the bus immediately (no arbitration).
0	0	1	IsoReq	Isochronous request: the LLC arbitrates for the bus, no gaps.
0	1	0	PriReq	Priority request: the LLC arbitrates after a subaction gap, ignores fair protocol.
0	1	1	FairReq	Fair request: the LLC arbitrates after a subaction gap, follows fair protocol.
1	0	0	RdReg	The LLC returns the specified register contents through a status transfer.
1	0	1	WrReg	The LLC writes to the specified register.
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

PRINCIPLES OF OPERATION

LREQ timing (each cell represents one clock sample time):

NOTE A: Each cell represents one clock sample time.

Figure 22. LREQ Timing

For fair or priority access, the LLC requests control of the bus at least one clock after the phy-LLC interface becomes idle. If the LLC senses that the CTLn terminals are in a receive state (CTL0 = 1, CTL1 = 0), this indicates that its request has been lost. This is true anytime during or after the LLC sends the bus request transfer. Additionally, the phy ignores any fair or priority requests if it asserts the receive state while the LLC is requesting the bus. The LLC then reissues the request one clock after the next interface idle.

The cycle master uses a normal priority request to send a cycle-start message. After receiving a cycle-start message, the LLC can issue an isochronous bus request. When arbitration is won, the LLC proceeds with the isochronous transfer of data. The isochronous request register is cleared in the phy once the LLC sends another type of request or when the isochronous transfer has been completed. The isochronous request must be issued during a packet reception. Generally this request would be during reception of a cycle-start packet.

The ImmReq request is issued when the LLC needs to send an acknowledgment after reception of a packet addressed to it. This request must be issued during packet reception. This is done to minimize the delays that a phy would have to wait between the end of a packet and the transmittal of an acknowledgment. As soon as the packet ends, the phy immediately grants access of the bus to the LLC. The LLC sends an acknowledgment to the sender unless the header CRC of the packet turns out to be bad. In this case, the LLC releases the bus immediately; it is not allowed to send another type of packet on this grant. To guarantee this, the LLC is forced to wait 160 ns after the end of the packet is received. The phy then gains control of the bus and the acknowledgement with the CRC error is sent. Then the bus is released and allowed to proceed with another requests.

Although highly improbable, it is conceivable that two separate nodes can believe that an incoming packet is intended for them. The nodes then issue a ImmReq request before checking the CRC of the packet. Since both phys seize control of the bus at the same time, a temporary, localized collision of the bus occurs somewhere between the competing nodes. This collision would be interpreted by the other nodes on the network as being a high-impedance line state, not a bus reset. As soon as the two nodes check the CRC, the mistaken node drops its request and the false line state is removed. The only side effect would be the loss of the intended acknowledgment packet (this is handled by the higher-layer protocol).

Read/Write Requests

When the LLC requests to read the specified register contents, the phy sends the contents of the register to the LLC through a status transfer. When an incoming packet is received while the phy is transferring status information to the LLC, the phy continues to attempt to transfer the contents of the register until it is successful.

For write requests, the phy loads the data field into the appropriately addressed register as soon as the transfer has been completed. The LLC is allowed to request read or write operations at any time.

PRINCIPLES OF OPERATION

Status

A status transfer is initiated by the phy when it has status information to transfer to the LLC. The phy waits until the interface is idle before starting the transfer. The transfer is initiated by asserting the following on the control terminals: CTL0 – CTL1 = 01 along with the first two bits of status information on the D0 – D3 terminals. The phy maintains CTL0 – CTL1 = 01 for the duration of status transfer. The phy may prematurely end a status transfer by asserting something else other than CTL0 – CTL1 = 01 on the control terminals. This could be caused by an incoming packet from another node. The phy continues to attempt to complete the transfer until the information has been successfully transmitted. There must be at least one idle cycle in between consecutive status transfers.

The phy normally sends just the first 4 bits of status to the LLC. These bits are status flags that are needed by the LLC state machines. The phy sends an entire status packet to the LLC after a request transfer that contains a read request, or when the phy has pertinent information to send to the LLC or transaction layers. The only defined condition where the phy automatically sends a register to the LLC is after Self-ID, when it sends the physical-ID register, which contains the new node address.

The definition of the bits in the status transfer are shown in Table 13 and the timing is shown in Figure 23.

Table 13. 16-Bit Stream Status Request

BIT(S)	NAME	DESCRIPTION
0	Arbitration Reset Gap	Bit 0 indicates that the phy has detected that the bus has been idle for an arbitration reset gap time (this time is defined in the IEEE 1394–1995 standard). Bit 0 is used by the LLC in its busy/retry state machine.
1	Subaction Gap	Bit 1 indicates that the phy has detected that the bus has been idle for a subaction gap time (this time is defined in the IEEE 1394–1995 standard). Bit 1 is used by the LLC to detect the completion of an isochronous cycle.
2	Bus Reset	Bit 2 indicates that the phy has entered the bus reset state.
3	State Timeout or CPS	Bit 3 indicates that the phy stayed in a particular state for too long a period, which is usually the effect of a loop in the cable topology, or that the cable power has dropped below the threshold for reliable operation.
4–7	Address	Bits 4 – 7 hold the address of the phy register whose contents are transferred to the LLC.
8–15	Data	Bits 8 – 15 contain the data that is to be sent to the LLC.

Figure 23. Status Transfer Timing

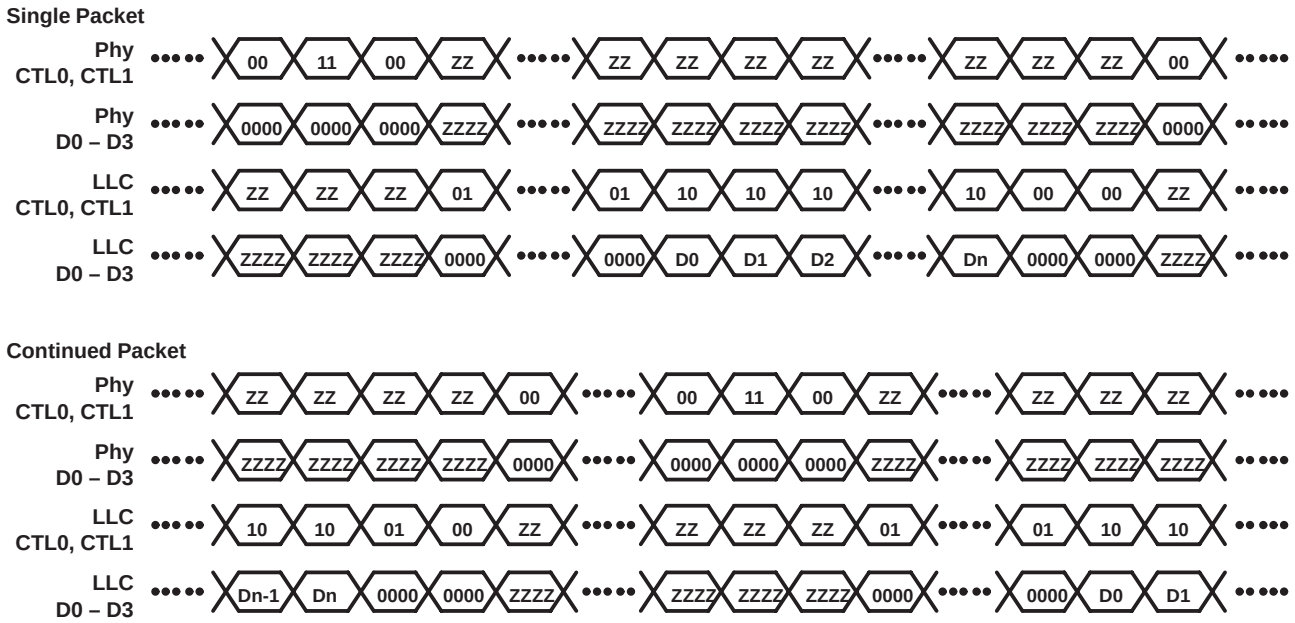
PRINCIPLES OF OPERATION

Transmit

When the LLC wants to transmit information, it first requests access to the bus through the LREQ terminal. Once the phy receives this request, it arbitrates to gain control of the bus. When the phy wins ownership of the serial bus, it grants the bus to the LLC by asserting the transmit state on the CTLn terminals for at least one SYSCLK cycle, followed by idle for one clock cycle. The LLC takes control of the bus by asserting either hold or transmit on the CTLn terminals. Hold is used by the LLC to keep control of the bus when it needs some time to prepare the data for transmission. The phy keeps control of the bus for the LLC by asserting a data-on state on the bus. It is not necessary for the LLC to use hold when it is ready to transmit as soon as bus ownership is granted.

When the LLC is prepared to send data, it asserts the transmit state on the CTLn terminals as well as sending the first bits of the packet on the D0 – D3 lines (assuming 200 Mbits/s). The transmit state is held on the CTLn terminals until the last bits of data have been sent. The LLC then asserts an idle state on the CTLn terminals for one clock cycle after which it releases control of the interface.

However, there are times when the LLC needs to send another packet without releasing the bus. For example, the LLC may want to send consecutive isochronous packets or it may want to attach a response to an acknowledgment. To do this, the LLC asserts a hold state instead of an idle state when the first packet of data has been completely transmitted. In this case, hold informs the phy that the LLC needs to send another packet without releasing control of the bus. The phy then waits a set amount of time before asserting a transmit state. The LLC can then proceed with the transmittal of the second packet. After all data has been transmitted and the LLC has asserted an idle state on the CTLn terminals, the phy asserts its own idle state on the CTLn terminals. When sending multiple packets in this fashion, it is required that all data be transmitted at the same speed. This is required because the transmission speed is set during arbitration and since the arbitration step is skipped, there is no way of informing the network of a change in speed.



NOTE A: ZZ = High-impedance state
D0 => Dn = Packet data

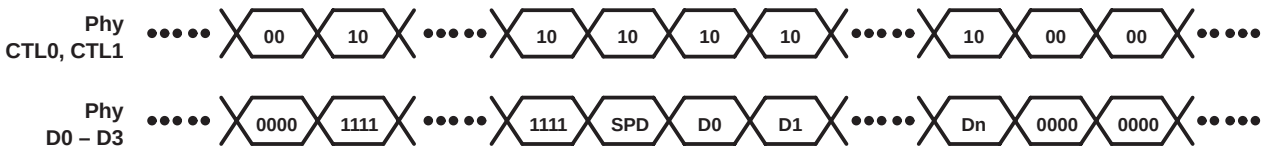
Figure 24. Transmit Timing Waveforms

PRINCIPLES OF OPERATION

Receive

When data is received by the phy from the serial bus, the phy transfers the data to the LLC for further processing. The phy asserts a receive state on the CTLn terminals and asserts a 1 on each Dn terminal. The phy indicates the start of the packet by placing the speed code on the data bus. The phy then proceeds with the transmittal of the packet to the LLC on the Dn terminals while still keeping the receive status on the CTLn terminals. Once the packet has been completely transferred, the phy asserts an idle state on the CTLn terminals, which completes the receive operation.

NOTE:
The speed is a phy-LLC protocol and not included in the CRC.



NOTE A: SPD = Speed Code
D0 => Dn = Packet data

Figure 25. Receive Timing Waveforms

Table 14. Speed Code for the Receiver

D0 – D3	Data Rate
00YY†	100 Mbit/s
0100	200 Mbit/s

† Y = Transmitted as 0, ignored on receive.

Power Class Bits in Self-ID Packet

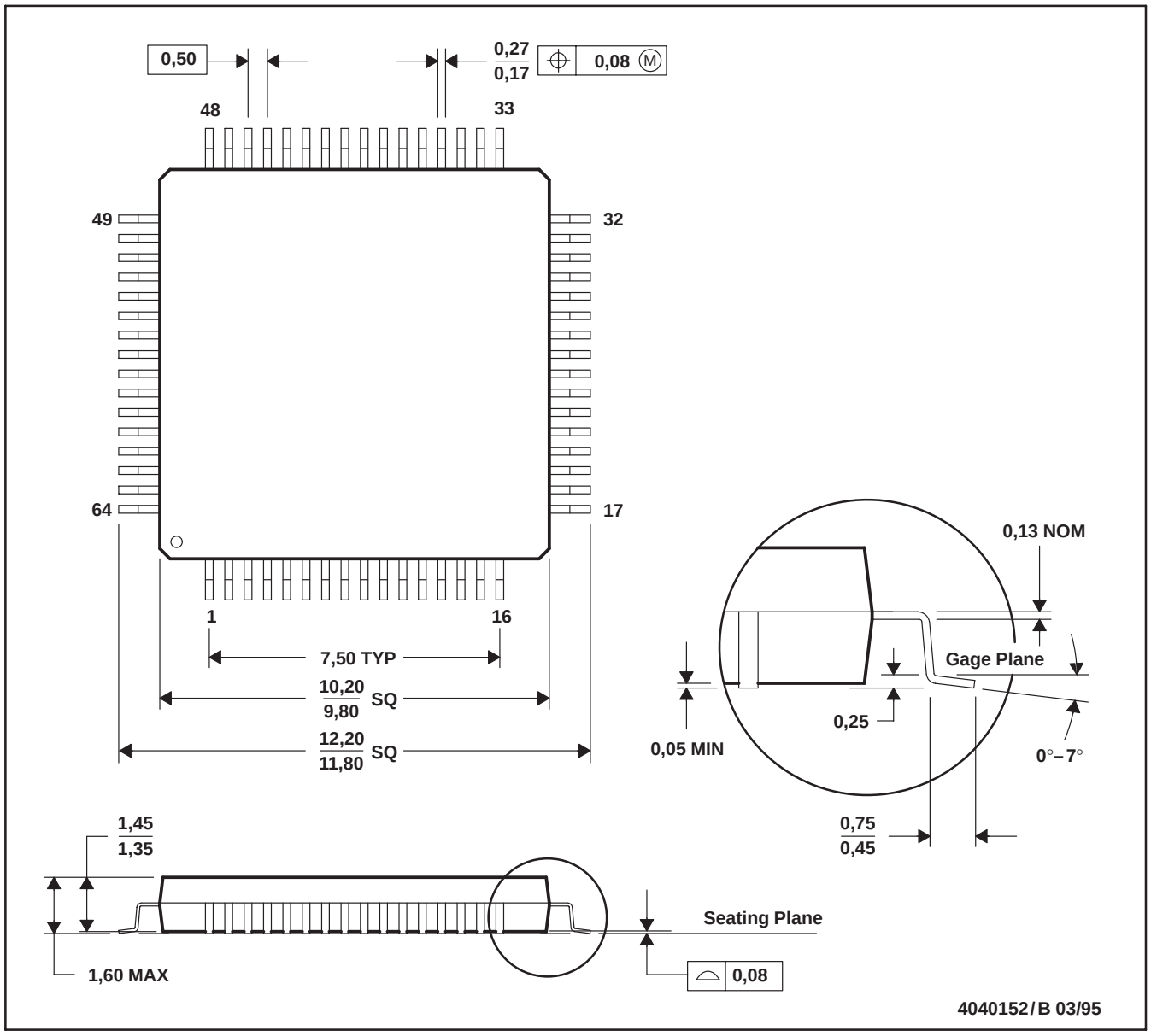
Table 15 describes the meaning of the power-class bits in the pwr field of the Self-ID packet. Bit 21 is transmitted first, followed by bit 22 and then bit 23.

Table 15. Self-ID Packet Pwr-Field Bit Description

PC [21:23]	DESCRIPTION
000	Node does not need power and does not repeat power.
001	Node is self powered, and provides a minimum of 15 W to the bus.
010	Node is self powered, and provides a minimum of 30 W to the bus.
011	Node is self powered, and provides a minimum of 45 W to the bus.
100	Node may be powered from the bus, and is using up to 1 W.
101	Node may be powered from the bus, and is using up to 1 W. An additional 2 W is needed to enable the LLC and higher layers.
110	Node may be powered from the bus, and is using up to 1 W. An additional 5 W is needed to enable the LLC and higher layers.
111	Node may be powered from the bus, and is using up to 1 W. An additional 9 W is needed to enable the LLC and higher layers.

MECHANICAL INFORMATION

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

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