ERRATA
TO THE TSB41LV06 DATA SHEET
(TEXAS INSTRUMENTS LITERATURE NO. SLLS289, DECEMBER 1998)

This document contains corrections and additions to information in the TSB41LV06 data sheet (TI Literature Number SLLS289, December 1998).

a. The TSB41LV06 5-V tolerance terminal does not operate properly. Therefore, the TSB41LV06 should not be directly connected to 5-V devices. The V_{DD}-5V terminal (pin 9) should be connected to the DV_{DD} (3.3 V) supply. TI plans to correct this in a future revision.

b. Bus-reset status contention for a node that is not connected to any other. A rare condition exists where a phy-link contention problem can occur if an unconnected node is transmitting cycle starts or other packets and another node is plugged in. If a bus-reset is initiated (due to a new connection) then TSB41LV06 phy will try to take control of the phy-link interface and send a bus-reset status transfer to the link. If the link is transmitting a packet at the same time, then there may be contention on the phy-link interface since both the phy and link are driving. The result is that the link will not see the bus-reset status transfer and will continue transmitting data.

Workaround:

A node should check its node and root status before transmitting cycle start or other packets. If the physical id is 0, but the node is root, then it is the only node on the bus. In this case, the node should not transmit any packets and the link's cycle master bits should be cleared.

A node can tell if an undetected bus reset has occurred if it receives one or more Self-IDs and/or an unsolicited register 0 status transfer.

c. Bus-reset Status. If the link writes to the Initiate Bus-Reset bit (IBR) while the PHY is already in bus-reset, no additional bus-reset status will be sent to the link. Software must allow for this case. TI plans to correct this in a future revision.

Workaround:

Software should not initiate another bus reset once it has received a bus reset status until the current bus reset is over.

d. IBR and Initiate Short Bus-Reset (ISBR) bits should be ***cleared*** only by bus-reset and ***set*** only by a register write. They should not be cleared by a register write. Currently, IBR and ISBR are allowed to be cleared by a register write, but software should not attempt this or rely on this. TI plans to correct this in a future revision.

e. ACK accelerated arbitration, one of the 1394a arbitration enhancement features, does not work correctly in the following circumstance. If the link transmits an ACK packet and then immediately issues a fair bus request, the arbitration for the fair bus request will not be accelerated as expected. Instead, the PHY will arbitrate for the bus after an arb-reset gap has elapsed. This problem does not occur if the start of the fair bus request is issued four or more SYSCLK cycles after the last data cycle of the transmitted ACK packet (as seen on the PHY-link interface). Also, this problem does not occur when the ACK packet is being received by the PHY (it occurs only when the ACK packet is being transmitted).

f. The Root-holdoff bit (RHB) does not automatically clear upon a bus-reset when the PHY is a not connected to any other nodes (stand alone mode), as required by the 1394a specification. The RHB should therefore be cleared by S/W when a node becomes standalone. If the RHB is left set true in a standalone node, and this node is later connected to a network in which another node has its RHB set, then the bus-initialization process will take longer than otherwise required.

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