Winbond Electronics Corp.

128K × 16 CMOS FLASH MEMORY WITH SYNCHRONOUS BURST READ

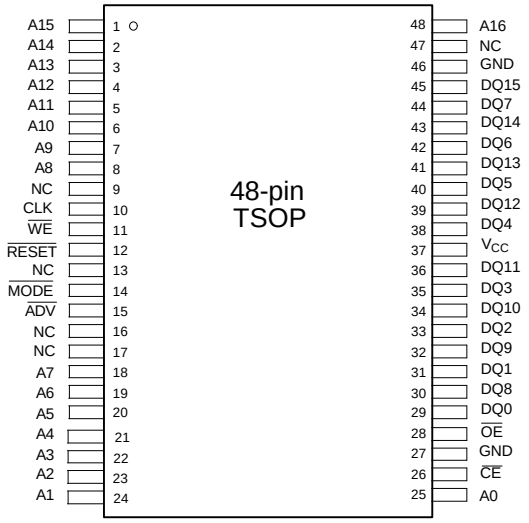
GENERAL DESCRIPTION

The W49S201 is a 2-megabit, 5-volt only CMOS flash memory organized as 128K × 16 bits. The W49S201 supports both asynchronous & high performance synchronous burst read modes. The device can be programmed and erased in-system with a standard 5V power supply. A 12-volt V_{PP} is not required. The unique cell architecture of the W49S201 results in fast program/erase operations with extremely low current consumption (compared to other comparable 5-volt flash memory products). The device can also be programmed and erased using standard EPROM programmers.

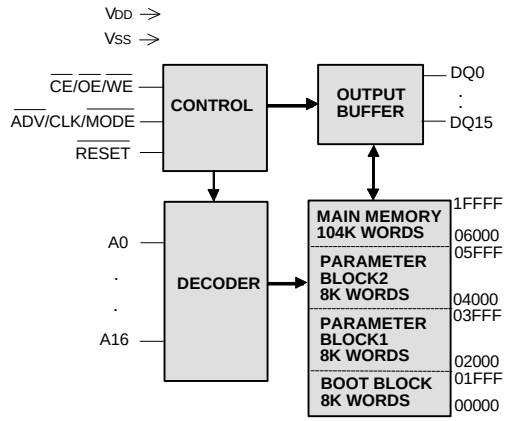
FEATURES

- Single 5-volt operations:
  - 5-volt Read
  - 5-volt Erase
  - 5-volt Program
- Fast Program operation:
  - Word-by-Word programming: 50 µS (max.)
- Fast Erase operation: 100 mS (typ.)
- Fast Synchronous Burst Read access time: 15/17 nS (typ.)
- High performance synchronous burst read mode up to 50 MHz Clock Frequency
- Support Linear Burst Mode Read with Wrap-Around Feature.
- No Burst Length Limitation.
- Fast Asynchronous Random Read access time: 55/70 nS
- Endurance: 10K/100K cycles (Typical.)
- Twenty-year data retention
- Hardware data protection
- Sector configuration
  - One 8K words boot block with lockout protection
  - Two 8K words parameter blocks
  - One 104K words (208K bytes) Main Memory Array Blocks
- Low power consumption
  - Active current: 35 mA (typ.)
  - Standby current: 20 µA (typ.)
- Automatic program and erase timing with internal V_{PP} generation
- End of program or erase detection
  - Toggle bit
  - Data polling
- Latched address and data
- TTL compatible I/O
- JEDEC standard word-wide pinouts
- Packaged in 48-pin TSOP

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
$\overline{RESET}$	Reset
A0–A16	Address Inputs
DQ0–DQ15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{ADV}$	Address Valid
CLK	Clock
$\overline{MODE}$	Synch/Asynch Mode Select
VDD	Power Supply
GND	Ground
NC	No Connection

FUNCTIONAL DESCRIPTION

Synchronous Burst & Asynchronous Read Mode Features

The Winbond's W49S201 Flash device requires 3 additional control pins for synchronous burst read operations: Synchronous/Asynchronous Read Mode Select ($\overline{MODE}$), Address Valid ($\overline{ADV}$), and Clock (CLK). This synchronous read mode feature allows W49S201 to be interfaced easily to a wide range of DSP, microprocessors, micro-controllers for higher performance read operations. All these 3 pins are only activated internally when chip is selected ($\overline{CE}$ = V_{IL}). The $\overline{MODE}$ input pin is used to select either synchronous or asynchronous read mode for the memory read operations. If $\overline{MODE}$ is held low, the synchronous burst read mode is selected for the read operation, and if $\overline{MODE}$ is held high then asynchronous read mode is selected for all read operations (the $\overline{ADV}$ and CLK are ignored by the Flash internally). The $\overline{ADV}$ input pin is used when the chip is selected in the synchronous read mode ($\overline{CE}$ = V_{IL} and $\overline{MODE}$ = V_{IL}) to load the initial random address into the Flash at the rising edge of the clock when $\overline{ADV}$ = V_{IL}, and to increment the internal address counter at the rising edge of the clock when $\overline{ADV}$ = V_{IH}. The CLK input pin can be tied to the system clock to provide the fundamental timing and array synchronous burst read operating frequency. Both $\overline{ADV}$ and CLK inputs are only enabled when chip is selected to operate in the synchronous burst read mode ($\overline{CE}$ = V_{IL} and $\overline{MODE}$ = V_{IL}). The $\overline{MODE}$ input pin is internally pulled high for applications which does not require the synchronous burst read operations, hence allowing these additional 3 pins to be considered as the No Connect (NC) pins. However, Winbond recommends that these 3 pins be driven at known logic level externally if possible. The states of these 3 additional pins are ignored during all write operations.

Asynchronous Random Read Mode

The asynchronous read operation of the W49S201 is controlled by $\overline{CE}$ and $\overline{OE}$, both of which have to be low for the host to obtain data from the outputs. $\overline{CE}$ is used for device selection. When $\overline{CE}$ is high, the chip is de-selected and only standby power will be consumed. $\overline{OE}$ is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. Refer to the timing waveforms for further details.

Synchronous Burst Read Mode

Beside being asynchronously controlled by $\overline{CE}$ and $\overline{OE}$ pins similarly as in the asynchronous read operations, the selected W49S201 Flash device when used in synchronous burst read operation mode ($\overline{MODE}$ = V_{IL}) requires the host to provide the initial random burst address by driving the $\overline{ADV}$ pin low at the rising edge of the clock (CLK) to latch the initial burst random address into the Flash device. Initial output data (at DQ pins) become available 2 clock cycles (or 3 clock cycles depending on starting address, refer to the timing waveforms for further details). By driving the $\overline{ADV}$ pin high at the rising edge of the clock enables the W49S201 device to read data from the next binary incremental address (linear burst mode). Sequential output data becomes available T_{KQV} (15/17) nS of burst access time after the rising edge of the clock (always 2 CLK periods after the address increment started, i.e., $\overline{ADV}$ pin went high). There is no burst length limitation for the W49S201 device architecture, hence allowing the host to sequentially read out the entire memory

data (128K words) with just one burst read operation. The W49S201 also supports full memory array linear wrap-around mode. The W49S201Q-15/17 can be used to operate at a system clock frequency as high as 50/40 MHz with only 3 initial wait-states (3-1-1-1) required for the initial random access depending on the host performance and capability on the starting & ending burst address selection. Refer to the timing waveforms for further details.

Reset Operation

The $\overline{\text{RESET}}$ input pin can be used in some application. When $\overline{\text{RESET}}$ pin is at high state, the device is in normal operation mode. When $\overline{\text{RESET}}$ pin is driven low for at least a period of T_{RP}, it will halts the device and all outputs are at high impedance state. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to assure data integrity. As the high state re-asserted to the $\overline{\text{RESET}}$ pin, the device will return to read or standby mode, it depends on the control signals. The system can read data T_{RH} after the $\overline{\text{RESET}}$ pin returns to V_{IH}. The other function for $\overline{\text{RESET}}$ pin is temporary reset the boot block. By applying the 12V to $\overline{\text{RESET}}$ pin, the boot block can be reprogrammed even though the boot block lockout function is enabled.

Boot Block Operation

There is one 8K-word boot block in this device, which can be used to store boot code. It is located in the first 8K words of the memory with the address range from 0000(hex) to 1FFF(hex).

See Command Codes for Boot Block Lockout Enable for the specific code. Once this feature is set the data for the designated block cannot be erased or programmed (programming lockout); other memory locations can be changed by the regular programming method. Once the boot block programming lockout feature is activated, the chip erase function will be disable.

There is one condition that the lockout feature can be overrides. Just apply 12V to $\overline{\text{RESET}}$ pin, the lockout feature will temporary be inactivated and the block can be erased/programmed. Once the $\overline{\text{RESET}}$ pin returns to TTL level, the lockout feature will be activated again.

In order to detect whether the boot block feature is set on the 8K-words block, users can perform software command sequence: enter the product identification mode (see Command Codes for Identification/Boot Block Lockout Detection for specific code), and then read from address "0002 hex". If the output data in DQ0 is "1", the boot block programming lockout feature is activated; if the output data in DQ0 is "0", the lockout feature is inactivated and the block can be erased or programmed.

To return to normal operation, perform a three-byte command sequence (or an alternate single-word command) to exit the identification mode. For the specific code, see Command Codes for Identification/Boot Block Lockout Detection.

Chip Erase Operation

The chip-erase mode can be initiated by a six-word command sequence. After the command loading cycle, the device enters the internal chip erase mode, which is automatically timed and will be completed in a fast 100 mS (typical). The host system is not required to provide any control or timing during this operation. The entire memory array will be erased to FF(hex) by the chip erase operation if the boot block programming lockout feature is not activated. Once the boot block lockout feature is activated, the chip erase function will only erase the main memory block and the 2 parameter blocks, data in the boot block remains unchanged. The device will automatically return to normal read mode

after the erase operation completed. Data polling and/or Toggle Bits can be used to detect end of erase cycle.

Sector Erase Operation

The three sectors, main memory and two parameters blocks, can be erased individually by initiating a six-word command sequence. Sector address is latched on the falling WE edge of the sixth cycle while the 30(hex) data input command is latched at the rising edge of WE. After the command loading cycle, the device enters the internal sector erase mode, which is automatically timed and will be completed in a fast 100 mS (typical). The host system is not required to provide any control or timing during this operation. The device will automatically return to normal read mode after the erase operation completed. Data polling and/or Toggle Bits can be used to detect end of erase cycle.

When the boot block lockout feature is inactivated, the boot block and the main memory block will be erased together. Once the boot block is locked, only the main memory block will be erased by the execution of sector erase operation.

Program Operation

The W49S201 is programmed on a word-by-word basis. Program operation can only change logical data "1" to logical data "0" The erase operation (changed entire data in main memory and/or boot block from "0" to "1" is needed before programming.

The program operation is initiated by a 4-word command cycle (see Command Codes for Word Programming). The device will internally enter the program operation immediately after the word-program command is entered. The internal program timer will automatically time-out (50 µS max. - T_{BP}) once completed and return to normal read mode. Data polling and/or Toggle Bits can be used to detect end of program cycle.

Hardware Data Protection

The integrity of the data stored in the W49S201 is also hardware protected in the following ways:

(1) Noise/Glitch Protection: A $\overline{WE}$ pulse of less than 15 nS in duration will not initiate a write cycle.

(2) V_{DD} Power Up/Down Detection: The programming operation is inhibited when V_{DD} is less than 2.5V typical.

(3) Write Inhibit Mode: Forcing $\overline{OE}$ low, $\overline{CE}$ high, or $\overline{WE}$ high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.

(4) V_{DD} power-on delay: When V_{DD} has reached its sense level, the device will automatically time-out 5 mS before any write (erase/program) operation.

Data Polling (DQ_7)- Write Status Detection

The W49S201 includes a data polling feature to indicate the end of a program or erase cycle. When the W49S201 is in the internal program or erase cycle, any attempt to read DQ_7 of the last word loaded will receive the complement of the true data. Once the program or erase cycle is completed, DQ_7 will show the true data. Note that DQ_7 will show logical "0" during the erase cycle, and become logical "1" or true data when the erase cycle has been completed. Note that is for asynchronous read mode only ($\overline{MODE}$ = V_{IH}).

Toggle Bit (DQ6)- Write Status Detection

In addition to data polling, the W49S201 provides another method for determining the end of a program cycle. During the internal program or erase cycle, any consecutive attempts to read DQ6 will produce alternating 0's and 1's. When the program or erase cycle is completed, this toggling between 0's and 1's will stop. The device is then ready for the next operation. Note that is for asynchronous read mode only ($\overline{MODE}$ = V_{IH}).

Product Identification

The product ID operation outputs the manufacturer code and device code. Programming equipment automatically matches the device with its proper erase and programming algorithms.

The manufacturer and device codes can be accessed by software or hardware operation. In the software access mode, a six-word (or JEDEC 3-word) command sequence can be used to access the product ID. A read from address 0000H outputs the manufacturer code, 00DA(hex). A read from address 0001(hex) outputs the device code, 0FAE(hex) if $\overline{MODE}$ = V_{IL}, or 00AE(hex) if $\overline{MODE}$ = V_{IH}.

The product ID operation can be terminated by a three-word command sequence or an alternative one-word command sequence (see Command Definition table).

In the hardware access mode, access to the product ID is activated by forcing $\overline{CE}$ and $\overline{OE}$ low, $\overline{WE}$ high, and raising A9 to 12 volts.

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage to V_{SS} Potential	-0.5 to +7.0	V
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +150	°C
D.C. Voltage on Any Pin to Ground Potential except A9	-0.5 to V_{DD} +1.0	V
Transient Voltage (<20 nS) on Any Pin to Ground Potential	-1.0 to V_{DD} +1.0	V
Voltage on A9 Pin to Ground Potential	-0.5 to 12.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device. The above ratings are for maximum stress ratings only, functional operation under these conditions or at any other condition beyond those indicated in the operational sections of this datasheet is not implied.

TABLE OF OPERATING MODES

Operating Mode Selection

(V_{HH} = 12V ± 0.5V)

MODE	PINS								
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	$\overline{MODE}$	$\overline{ADV}$	CLK	ADDRESS	DQ.
Latch Burst Address	V_{IL}	X	V_{IH}	V_{IH}	V_{IL}	V_{IL}	↑	A_{IN}	High Z/D_{OUT}
Burst Address Increment Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	↑	X	D_{OUT}

Operating Mode Selection, continued

MODE	PINS								
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	$\overline{MODE}$	$\overline{ADV}$	CLK	ADDRESS	DQ.
Read (Asynch.)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	A_{IN}	Dout
Erase/Program	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	X	X	A_{IN}	Din
Standby	V_{IH}	X	X	V_{IH}	X	X	X	X	High Z
Erase/Program	X	V_{IL}	X	V_{IH}	X	X	X	X	High Z/D_{OUT}
Inhibit	X	X	V_{IH}	V_{IH}	X	X	X	X	High Z/D_{OUT}
Output Disable	X	V_{IH}	X	V_{IH}	X	X	X	X	High Z
Product ID	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	X	A0 = V_{IL}; A1–A15 = V_{IL}; A9 = V_{HH}	Manufacturer Code 00DA (Hex)
	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	X	A0 = V_{IH}; A1–A15 = V_{IL}; A9 = V_{HH}	Device Code 0FAE (Hex) (Synch. Mode)
	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	A0 = V_{IH}; A1–A15 = V_{IL}; A9 = V_{HH}	Device Code 00AE (Hex) (Asynch. Mode)
Reset	X	X	X	V_{IL}	X	X	X	X	High Z

TABLE OF COMMAND DEFINITION

COMMAND DESCRIPTION	NO. OF Cycles	1ST CYCLE	2ND CYCLE	3RD CYCLE	4TH CYCLE	5TH CYCLE	6TH CYCLE
		Addr. Data	Addr. Data	Addr. Data	Addr. Data	Addr. Data	Addr. Data
Read	1	A_{IN} D_{OUT}					
Chip Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 10
Main Memory Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	SA 30
Word Program	4	5555 AA	2AAA 55	5555 A0	A_{IN} D_{IN}		
Boot Block Lockout	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 40
Product ID Entry	3	5555 AA	2AAA 55	5555 90			
Product ID Exit (1)	3	5555 AA	2AAA 55	5555 F0			
Product ID Exit (1)	1	XXXX F0					

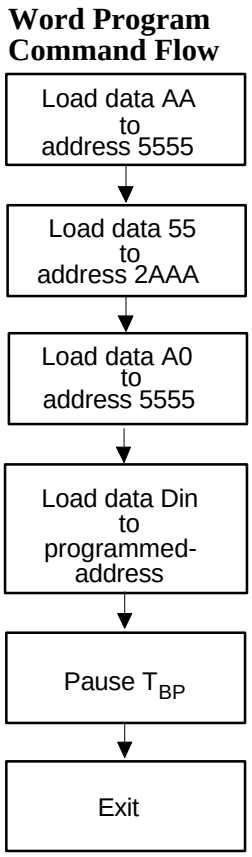
Notes:

1. Address Format: A14–A0 (Hex); Data Format: DQ15–DQ8 (Don't Care); DQ7-DQ0 (Hex)
2. Either one of the two Product ID Exit commands can be used.
3. SA: Sector Address
   SA = 03XXXh for Parameter Block1
   SA = 05XXXh for Parameter Block2
   SA = 1FXXXh
   - for Main Memory Block when Boot Block lockout feature is activated
   - for both Boot Block and Main Memory Block when Boot Block lockout feature is inactivated

Command Codes for Word Program

WORD SEQUENCE	ADDRESS	DATA
0 Write	5555H	AAH
1 Write	2AAAH	55H
2 Write	5555H	A0H
3 Write	Programmed-address	Programmed-data
	Pause T_{BP}	

Word Program Flow Chart

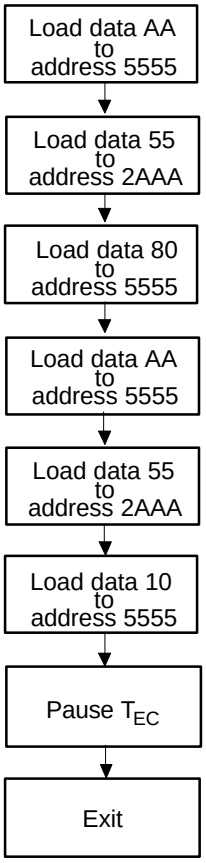


Notes for software program code:
Data Format: DQ15–DQ8: Don't Care; DQ7-DQ0(Hex)
Address Format: A14–A0 (Hex)

Command Codes for Chip Erase

BYTE SEQUENCE	ADDRESS	DATA
1 Write	5555H	AAH
2 Write	2AAAH	55H
3 Write	5555H	80H
4 Write	5555H	AAH
5 Write	2AAAH	55H
6 Write	5555H	10H
	Pause T_{EC}	

Chip Erase Acquisition Flow

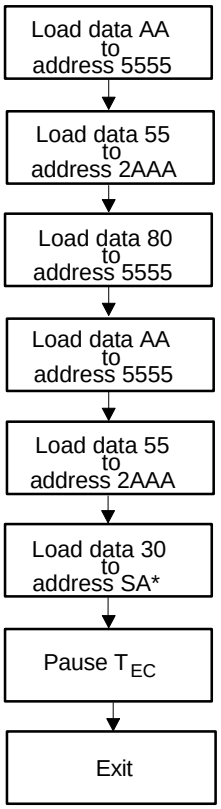


Notes for chip erase:
Data Format: DQ15-DQ8: Don't Care; DQ7–DQ0 (Hex)
Address Format: A14–A0 (Hex)

Command Codes for Sector Erase

BYTE SEQUENCE	ADDRESS	DATA
1 Write	5555H	AAH
2 Write	2AAAH	55H
3 Write	5555H	80H
4 Write	5555H	AAH
5 Write	2AAAH	55H
6 Write	SA*	30H
	Pause T_{EC}	

Sector Erase Acquisition Flow

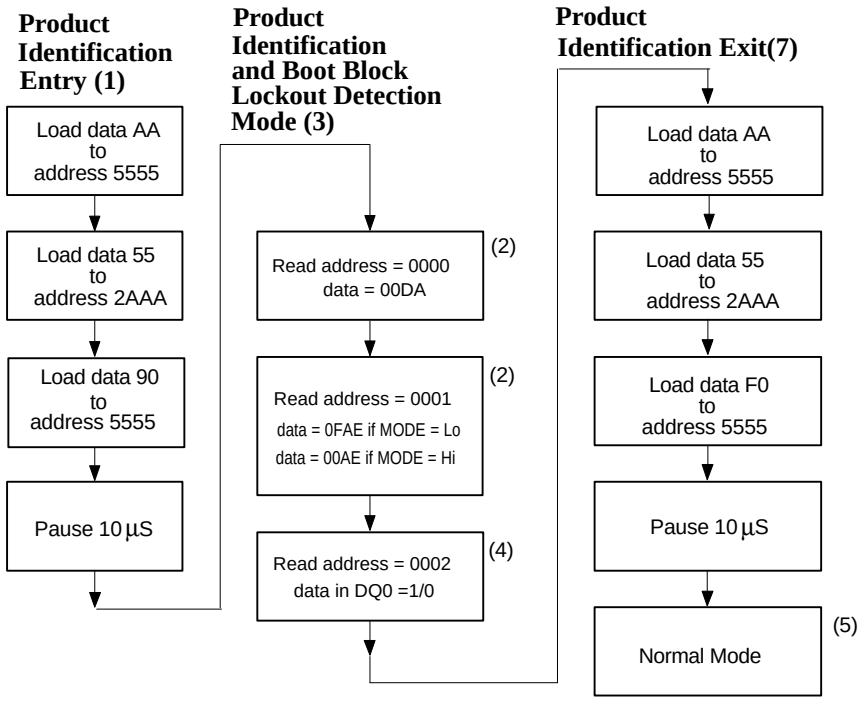


Notes for chip erase:
Data Format: DQ15-DQ8: Don't Care; DQ7–DQ0 (Hex)
Address Format: A14–A0 (Hex)
SA = 03XXX for parameter block1
SA = 05XXX for parameter block2
SA = 1FXXX
- for Main Memory Block when Boot Block lockout feature is activated
- for both Boot Block and Main Memory Block when Boot Block lockout feature is inactivated

Command Codes for Product Identification and Boot Block Lockout Detection

BYTE SEQUENCE	ALTERNATE PRODUCT (6) IDENTIFICATION/BOOT BLOCK LOCKOUT DETECTION ENTRY		SOFTWARE PRODUCT IDENTIFICATION/BOOT BLOCK LOCKOUT DETECTION EXIT (7)	
	ADDRESS	DATA	ADDRESS	DATA
1 Write	5555	AA	5555H	AAH
2 Write	2AAA	55	2AAAH	55H
3 Write	5555	90	5555H	F0H
	Pause 10 µS		Pause 10 µS	

Software Product Identification and Boot Block Lockout Detection Acquisition Flow



Notes for software product identification/boot block lockout detection:

(1) Data Format: DQ15-DQ8 (Don't Care), DQ7–DQ0 (Hex); Address Format: A14–A0 (Hex)

(2) A1–A16 = V_{IL}; manufacture code is read for A0 = V_{IL}; device code is read for A0 = V_{IH}.

(3) The device does not remain in identification and boot block lockout detection mode if power down.

(4) If the output data in DQ0 = 1, the boot block programming lockout feature is activated; if the output data in DQ0 = 0, the lockout feature is inactivated and the block can be programmed.

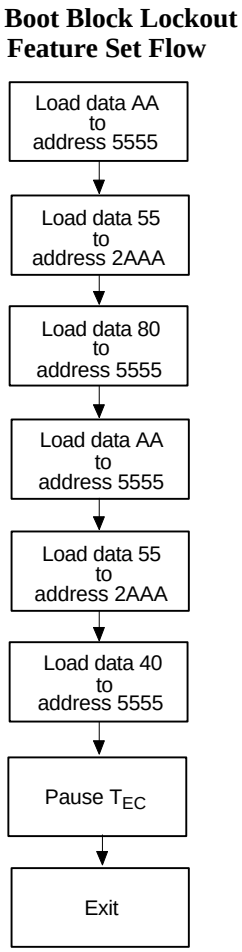
(5) The device returns to standard operation mode.

(6) Optional 1-write cycle (write F0 hex at XXXX address) can be used to exit the product identification/boot block lockout detection.

Command Codes for Boot Block Lockout Enable

BYTE SEQUENCE	BOOT BLOCK LOCKOUT FEATURE SET	
	ADDRESS	DATA
1 Write	5555H	AAH
2 Write	2AAAH	55H
3 Write	5555H	80H
4 Write	5555H	AAH
5 Write	2AAAH	55H
6 Write	5555H	40H
	Pause T_{EC}	

Boot Block Lockout Enable Acquisition Flow



Notes for boot block lockout enable:
Data Format: DQ15-DQ8 Don't Care), DQ7–DQ0 (Hex)
Address Format: A14–A0 (Hex)

DC CHARACTERISTICS

DC Operating Characteristics

(V_{DD} = 5.0V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
V_{DD} Asynch. Read Current	I_{CCR1}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, $\overline{MODE}$ = V_{IH}, all DQs open, CLK & $\overline{ADV}$ = V_{IL}/V_{IH}, Address Inputs = V_{IL}/V_{IH} at f = 5 MHz	-	35	75	mA
V_{DD} Synch Burst Read Current	I_{CCR2}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, $\overline{MODE}$ = V_{IL}, all DQs open, $\overline{ADV}$ = V_{IL}/V_{IH}, Address Inputs = V_{IL}/V_{IH}, CLK at f = F_{CLK} (max.)	-	-	175	mA
V_{DD} Erase or Program Current	I_{CCW}	Erase or Program Operation in Progress, all DQs open.	-	-	50	mA
Standby V_{DD} Current (TTL input)	I_{SB1}	$\overline{CE}$ = V_{IH}, all DQs open Other inputs = V_{IL}/V_{IH}	-	2	3	mA
Standby V_{DD} Current (CMOS input)	I_{SB2}	$\overline{CE}$ = V_{DD} ±0.3V, all DQs open Other Inputs = GND ±0.3V or V_{DD} ±0.3V	-	20	200	µA
Input Leakage Current	I_{LI}	V_{IN} = GND to V_{DD}	-	-	± 10	µA
Output Leakage Current	I_{LO}	V_{OUT} = GND to V_{DD}	-	-	± 10	µA
Input Low Voltage	V_{IL}	-	-0.3	-	0.8	V
Input High Voltage	V_{IH}	-	2.0	-	V_{DD} +0.5	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage	V_{OH}	I_{OH} = -0.4 mA	2.4	-	-	V

Power-up Timing

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	$T_{PU. READ}$	100	µS
Power-up to Write Operation	$T_{PU. WRITE}$	5	mS

CAPACITANCE

(V_{DD} = 5.0V, T_A = 25° C, f = 1 MHz)

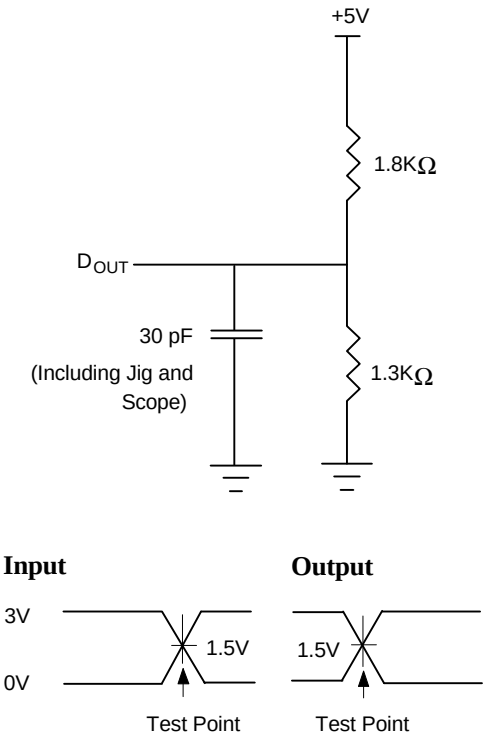
PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
I/O Pin Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	12	pf
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pf

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3.0V
Input Rise/Fall Time	< 5 nS
Input/Output Timing Level	1.5V/1.5V
Output Load	1 TTL Gate and C_L = 30 pF

AC Test Load and Waveform



Asynchronous Read Cycle Timing Parameters

(V_{CC} = 5.0V ±10%, V_{CC} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	W49S201-15		W49S201-17		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	55	-	70	-	nS
Chip Enable Access Time	T_{CE}	-	55	-	70	nS
Address Access Time	T_{AA}	-	55	-	70	nS
Output Enable Access Time	T_{OE}	-	25	-	35	nS
$\overline{CE}$ Low to Active Output	T_{CLZ}	0	-	0	-	nS
$\overline{OE}$ Low to Active Output	T_{OLZ}	0	-	0	-	nS
$\overline{CE}$ High to High-Z Output	T_{CHZ}	-	20	-	25	nS
$\overline{OE}$ High to High-Z Output	T_{OHZ}	-	20	-	25	nS
Output Hold Time	T_{OH}	0	-	0	-	nS

Note: The parameter of T_{CLZ}, T_{OLZ}, T_{CHZ}, T_{OHZ} are characterized only and is not 100% tested.

Synchronous Burst Read Cycle Timing Parameters

(V_{CC} = 5.0V ± 10%, V_{CC} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	W49S201-15		W49S201-17		UNIT
		MIN.	MAX.	MIN.	MAX.	
CLK Frequency	F_{CLK}	-	50	-	40	MHz
CLK Period	T_{CYC}	20	-	25	-	nS
CLK High Time	T_{KH}	7	-	8	-	nS
CLK Low Time	T_{KL}	7	-	8	-	nS
CLK Rise Time	T_{KLH}	-	2	-	3	nS
CLK Fall Time	T_{KHL}	-	2	-	3	nS
$\overline{CE}$ Setup Time to CLK	T_{CES}	15	-	20	-	nS
Address Setup Time to CLK	T_{AKS}	12	-	15	-	nS
Address Hold Time From CLK	T_{AKH}	2	-	2	-	nS
$\overline{ADV}$ Setup Time to CLK	T_{ADVS}	12	-	15	-	nS
$\overline{ADV}$ Hold Time From CLK	T_{ADVH}	2	-	2	-	nS
$\overline{MODE}$ Setup Time to CLK	T_{MODS}	15	-	20	-	nS
$\overline{MODE}$ Hold Time From CLK	T_{MODH}	5	-	5	-	nS
CLK to Valid Output	T_{KQV}	-	15	-	17	nS
Output Hold Time From CLK	T_{KQH}	1	-	1	-	nS

Note: The parameter of T_{KQH} is characterized only and is not 100% tested.

AC Characteristics, continued

Write Cycle Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Setup Time	T_{AS}	0	-	-	nS
Address Hold Time	T_{AH}	50	-	-	nS
$\overline{WE}$ and $\overline{CE}$ Setup Time	T_{CS}	0	-	-	nS
$\overline{WE}$ and $\overline{CE}$ Hold Time	T_{CH}	0	-	-	nS
$\overline{OE}$ High Setup Time	T_{OES}	0	-	-	nS
$\overline{OE}$ High Hold Time	T_{OEH}	0	-	-	nS
$\overline{CE}$ Pulse Width	T_{CP}	70	-	-	nS
$\overline{WE}$ Pulse Width	T_{WP}	70	-	-	nS
$\overline{WE}$ High Width	T_{WPH}	100	-	-	nS
Data Setup Time	T_{DS}	50	-	-	nS
Data Hold Time	T_{DH}	10	-	-	nS
Word programming Time	T_{BP}	-	10	50	µS
Erase Cycle Time	T_{EC}	-	0.1	1	S

Note: All AC timing signals observe the following guidelines for determining setup and hold times:
(a) High level signal's reference level is V_{IH} and (b) low level signal's reference level is V_{IL}.

Data Polling and Toggle Bit Timing Parameters

PARAMETER	SYM.	W49S201-15		W49S201-17		UNIT
		MIN.	MAX.	MIN.	MAX.	
$\overline{OE}$ to Data Polling Output Delay	T_{OEP}	-	25	-	35	nS
$\overline{CE}$ to Data Polling Output Delay	T_{CEP}	-	55	-	70	nS
$\overline{OE}$ to Toggle Bit Output Delay	T_{OET}	-	25	-	35	nS
$\overline{CE}$ to Toggle Bit Output Delay	T_{CET}	-	55	-	70	nS

Hardware Reset Timing Parameters

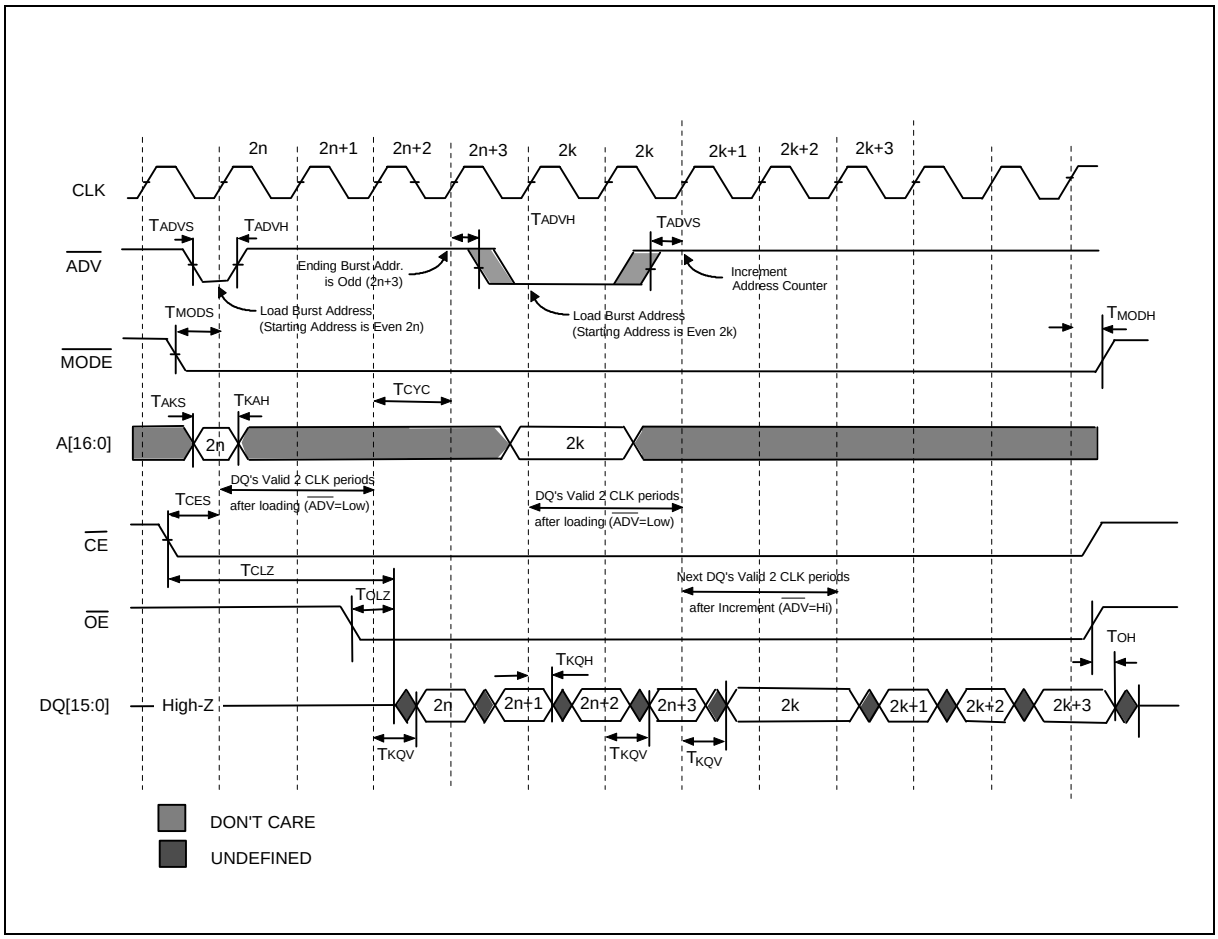
PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{RESET}$ Pin Low to Read or Write	T_{READY}	-	500	nS
$\overline{RESET}$ Pulse Width	T_{RP}	500	-	nS
$\overline{RESET}$ High Time Before Read(1)	T_{RH}	50	-	nS

Note: 1. The parameters are characterized only and is not 100% tested.

TIMING WAVEFORMS

Synchronous Burst Read Cycle Timing 1 (3-1-1-1 linear mode)

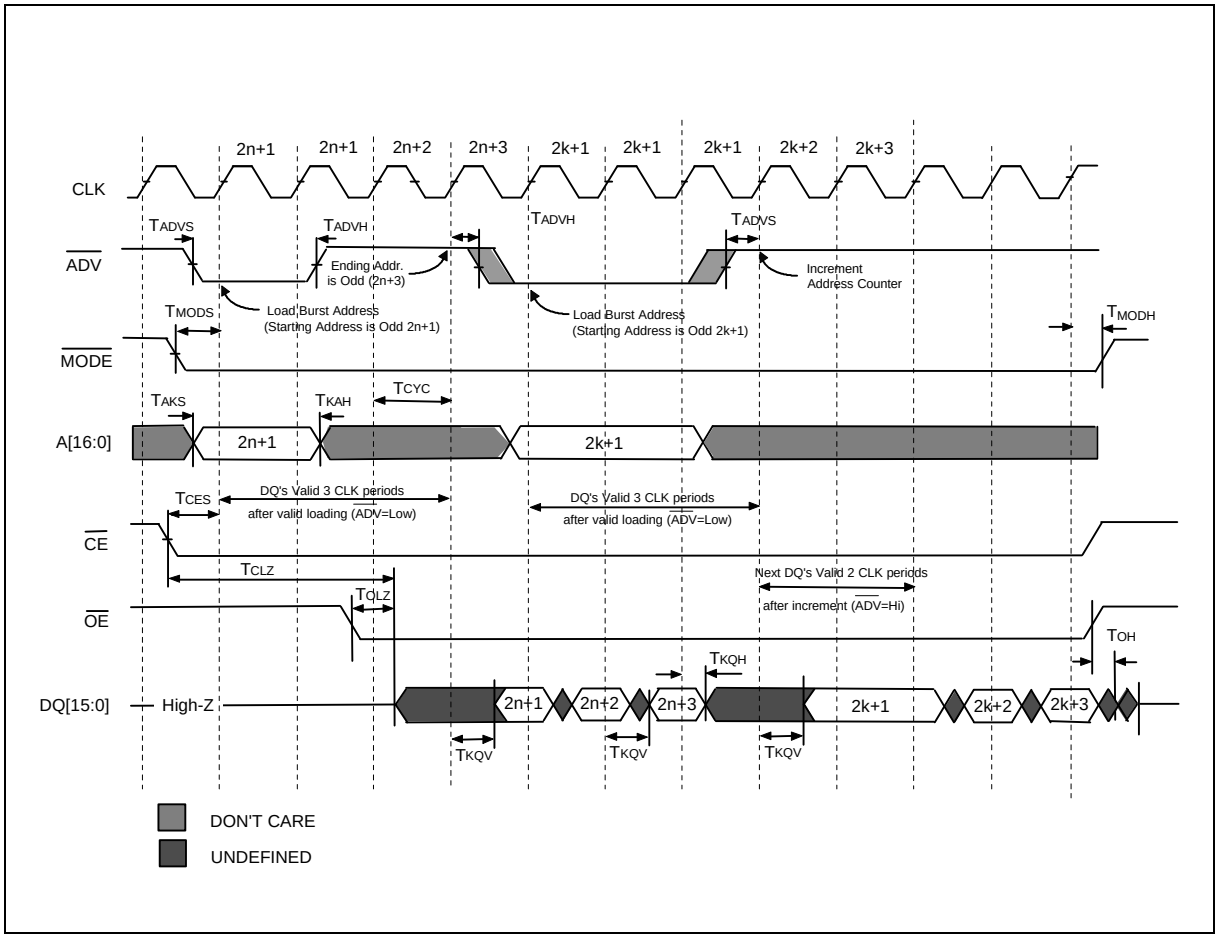
(Starting Address is Even and Ending Address is Odd)



Note: The above waveform is applicable to synchronous read mode with starting random address is always Even and ending address is always Odd address only. The $\overline{ADV}$ can be 1 CLK period pulse minimum, and the total wait states can be 3 CLK periods minimum. Initial output data DQ[15:0] become valid 2 CLK periods after the valid address loading started ($\overline{ADV}$ = Low) & next sequential output data DQ[15:0] become valid 2 CLK periods after address increment started ($\overline{ADV}$ = Hi).

Synchronous Burst Read Cycle Timing 2 (4-1-1-1 linear mode)

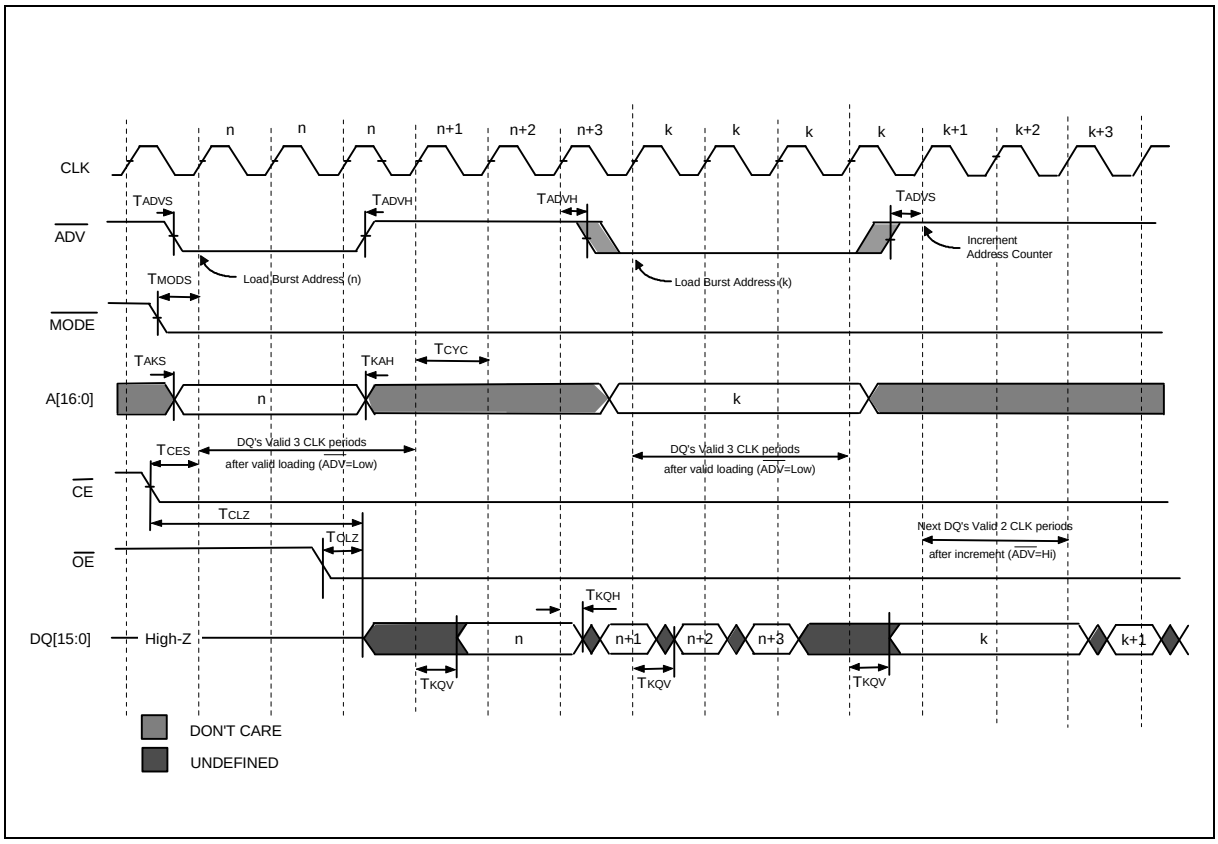
(Starting Address & Ending Address are both either Even or Odd)



Note: The above waveform is applicable to synchronous burst read mode with starting random address and ending burst address are both either Even or Odd only (shown above with Starting & Ending are Odd address). The $\overline{ADV}$ must be minimum 2 CLK period pulse, and the total wait states hence can be 4 CLK periods minimum. Initial output data DQ[15:0] become valid 3 CLK periods after the valid address loading started ($\overline{ADV}$ = Low) & next sequential output data DQ[15:0] become valid 2 CLK periods after address increment started ($\overline{ADV}$ = Hi).

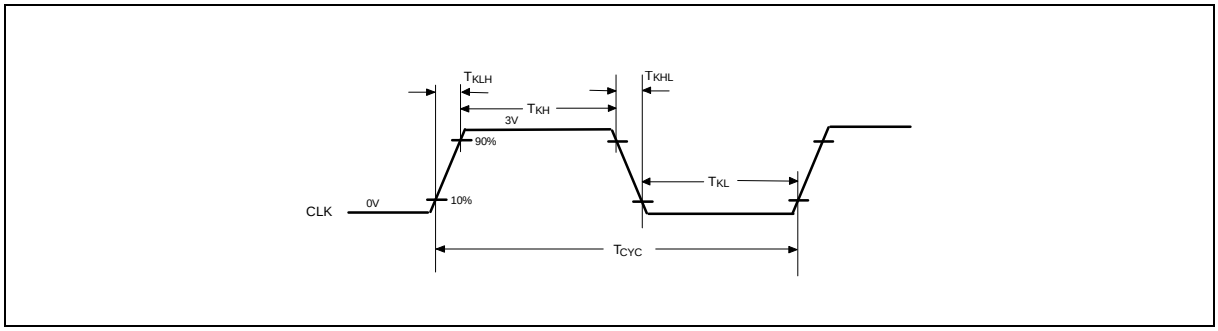
Synchronous Burst Read Cycle Timing 3 (5-1-1-1 linear mode)

(Starting Address & Ending Address can be Any Random Address)

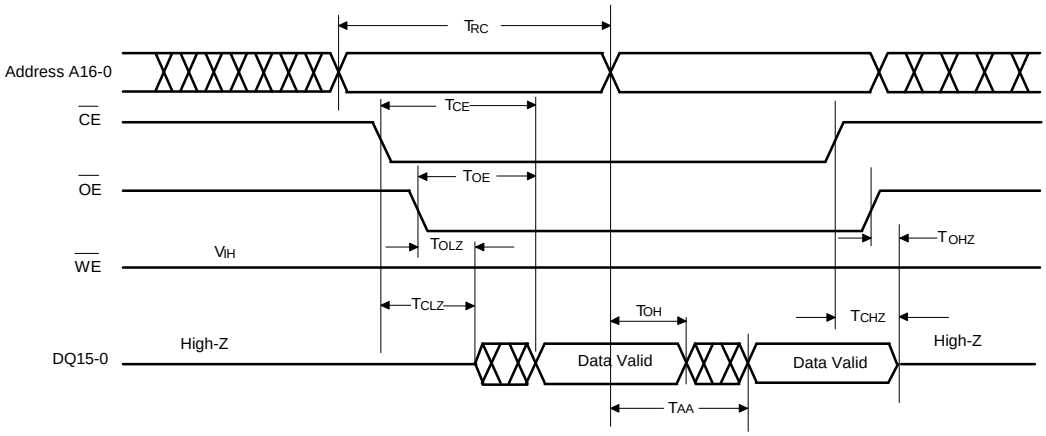


Note: The above waveform is applicable to synchronous burst read mode with any starting random address and any ending burst (can be either even or odd). The $\overline{ADV}$ must be minimum 3 CLK period pulse, and the total wait states hence can be 5 CLK periods minimum. Initial output data DQ[15:0] become valid 3 CLK periods after the valid address loading started ($\overline{ADV}$ = Low) & next sequential output data DQ[15:0] become valid 2 CLK periods after address increment started ($\overline{ADV}$ = Hi).

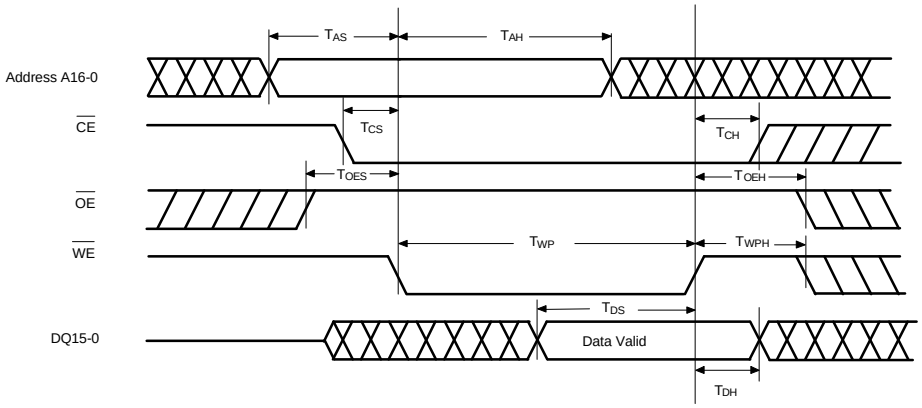
Clock Input Timing Diagram



Asynchronous Read Cycle Timing Diagram

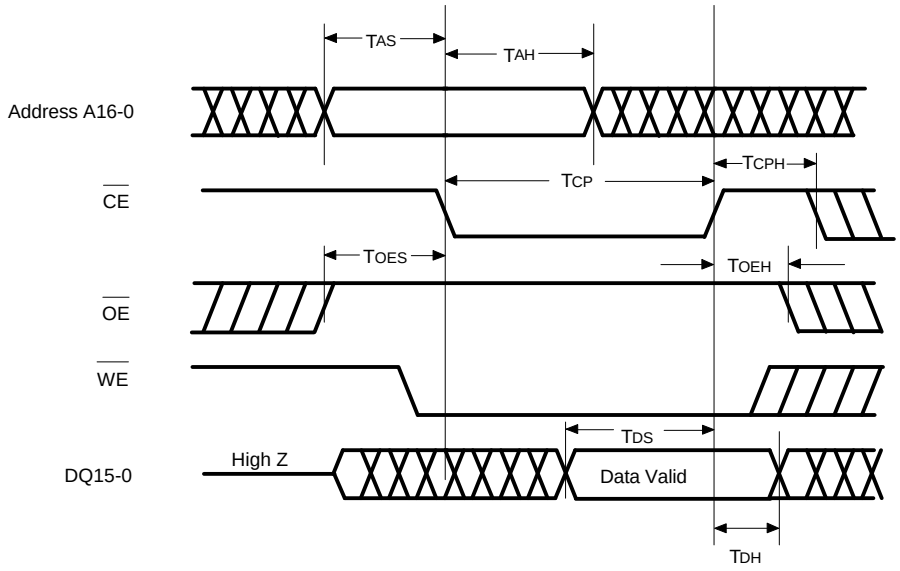


WE Controlled Command Write Cycle Timing Diagram

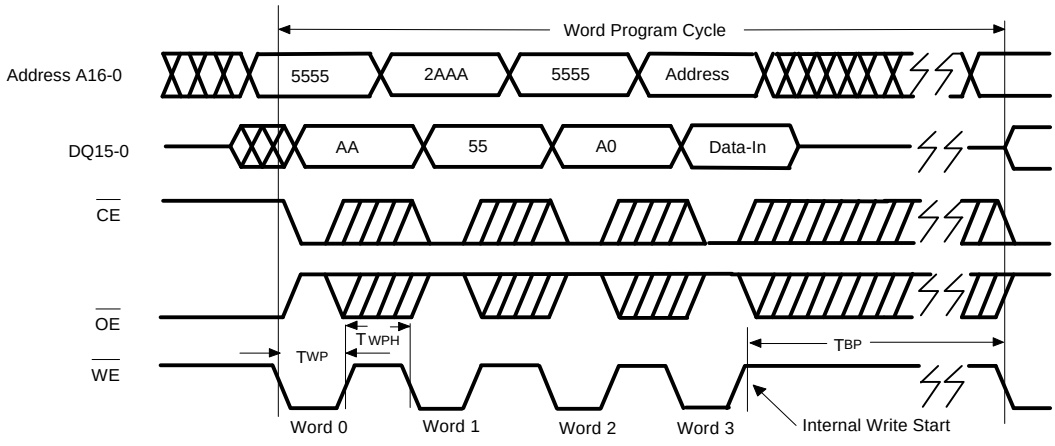


Timing Waveforms, continued

$\overline{CE}$ Controlled Command Write Cycle Timing Diagram

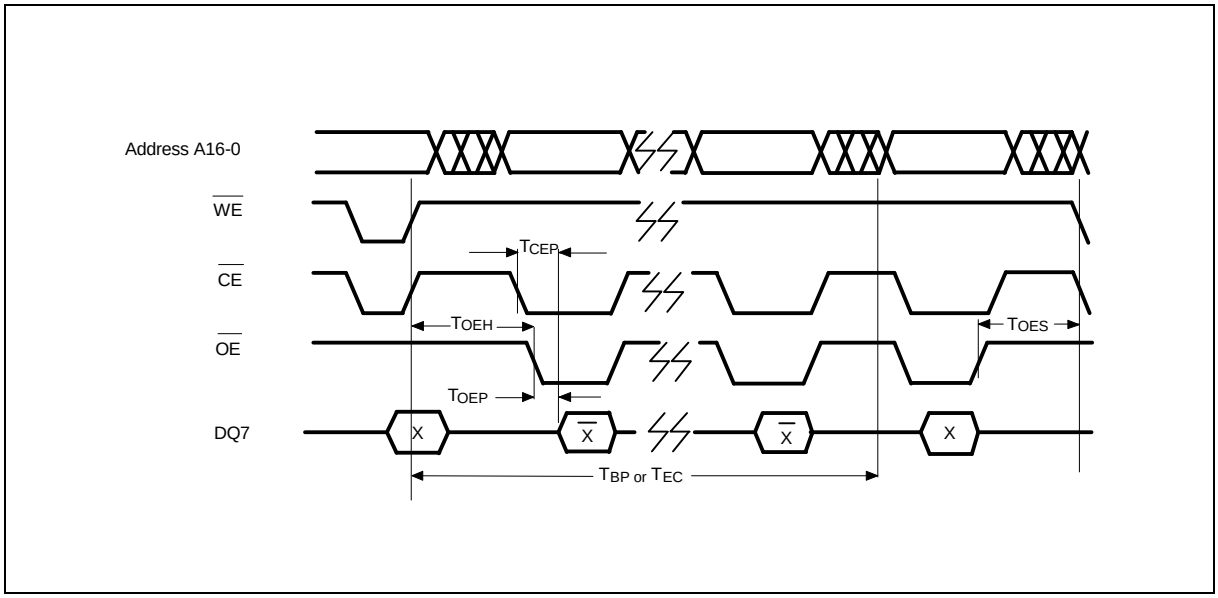


Program Cycle Timing Diagram

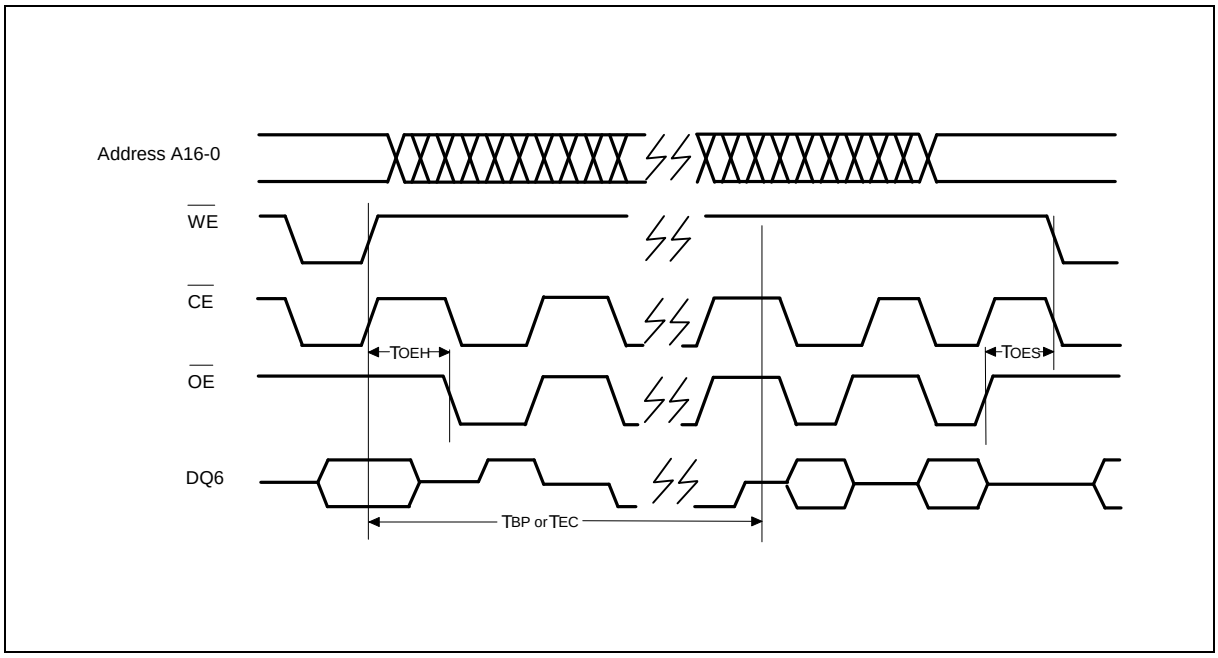


Timing Waveforms, continued

$\overline{\text{DATA}}$ Polling Timing Diagram

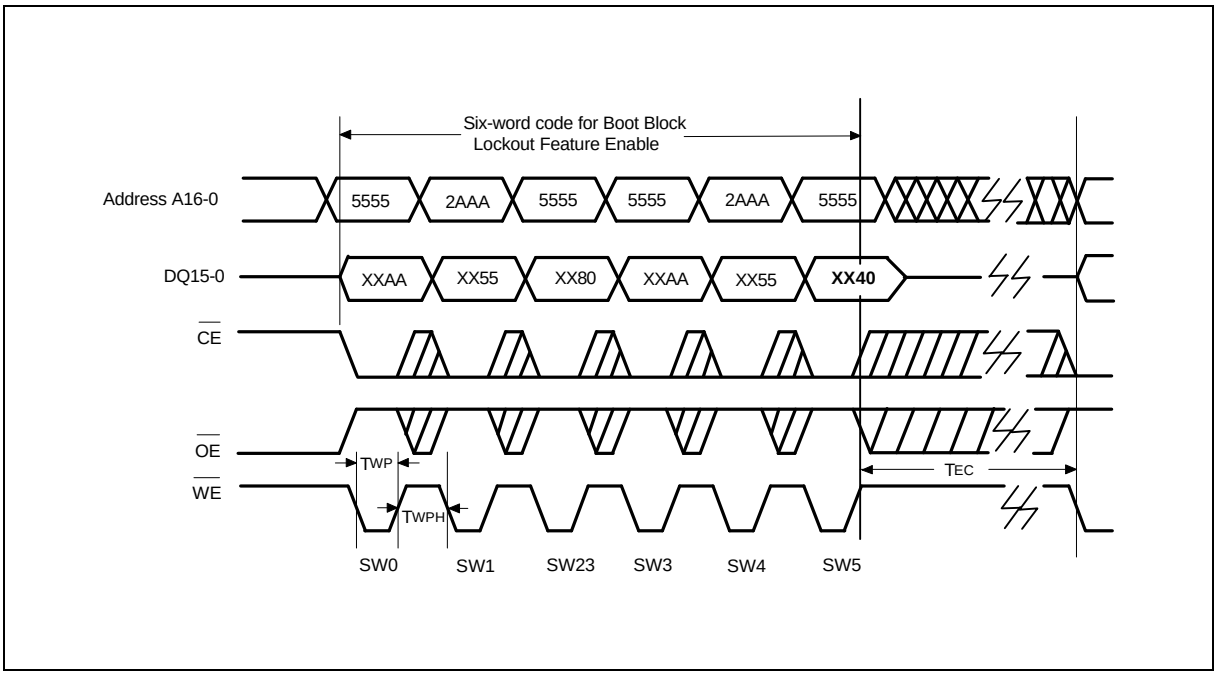


Toggle Bit Timing Diagram

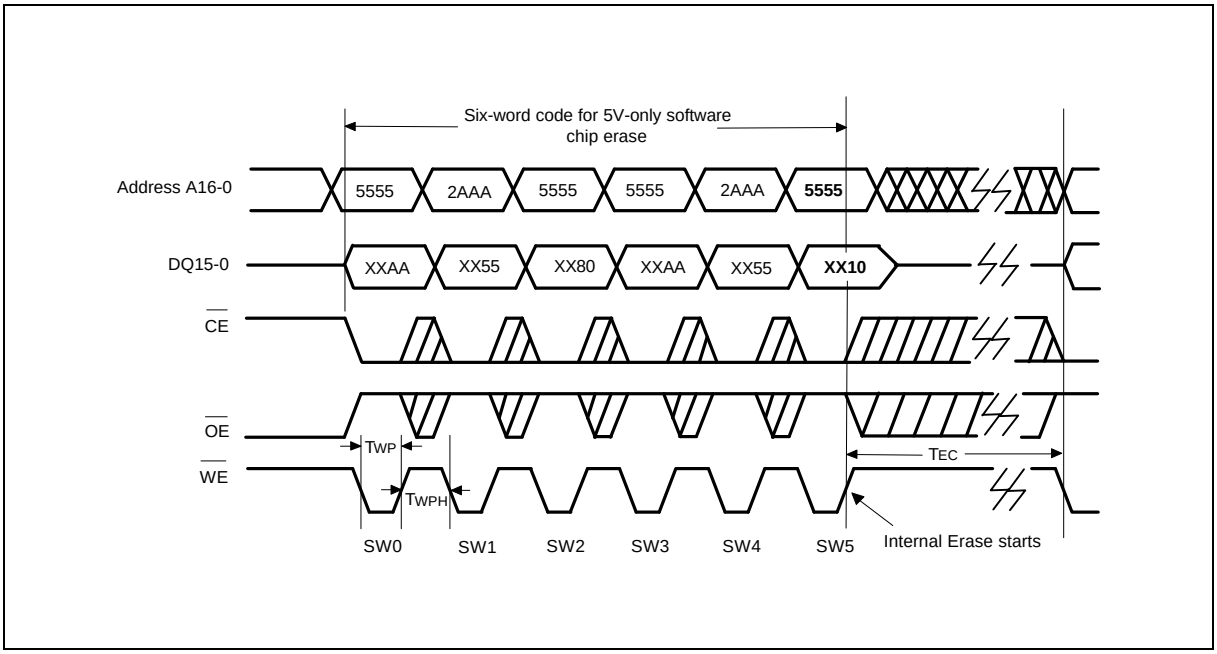


Timing Waveforms, continued

Boot Block Lockout Enable Timing Diagram

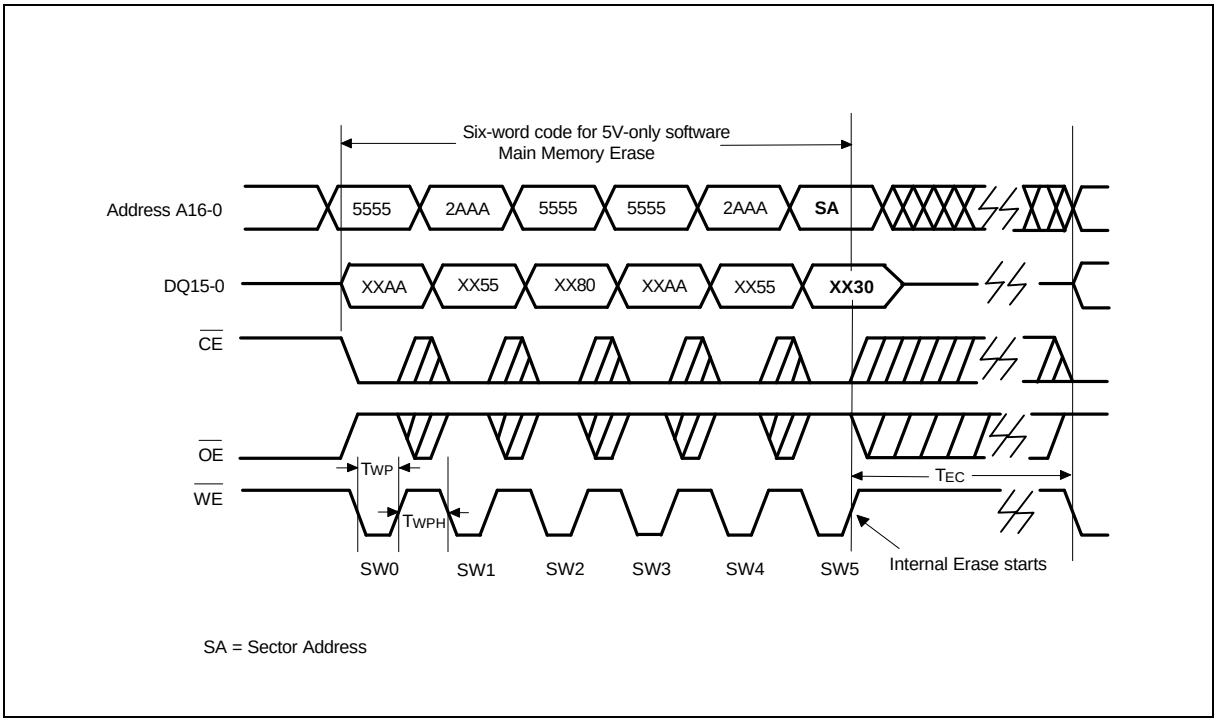


Chip Erase Timing Diagram

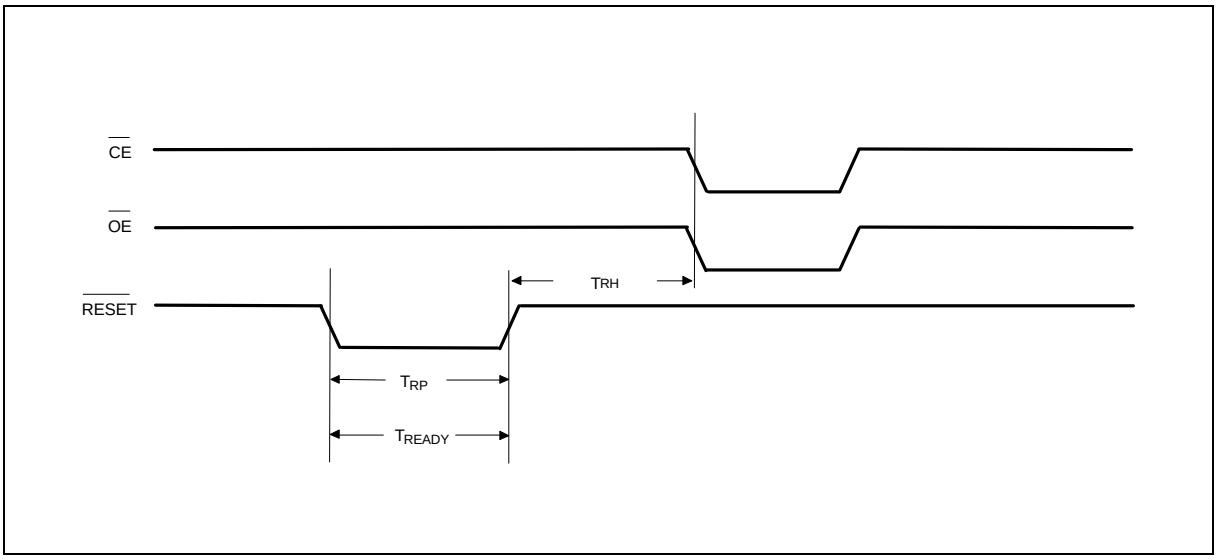


Timing Waveforms, continued

Sector Erase Timing Diagram



Reset Timing Diagram



ORDERING INFORMATION

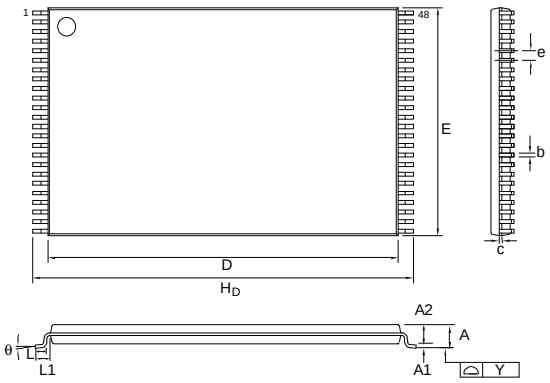
PART NO.	ACCESS TIME T_{KQV} (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY V_{DD} CURRENT MAX. (mA)	PACKAGE	CYCLE
W49S201Q-15B	15	75	200 (CMOS)	48-pin TSOP (12 mm × 20 mm)	10K
W49S201Q-17B	17	75	200 (CMOS)	48-pin TSOP (12 mm × 20 mm)	10K
W49S201Q-15C	15	75	200 (CMOS)	48-pin TSOP (12 mm × 20 mm)	100K
W49S201Q-17C	17	75	200 (CMOS)	48-pin TSOP (12 mm × 20 mm)	100K

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

48-pin TSOP (12 mm · 20 mm)



Symbol	Dimension in mm			Dimension in Inches		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	—	0.002	—	—
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	18.3	18.4	18.5	0.720	0.724	0.728
H_D	19.8	20.0	20.2	0.780	0.787	0.795
E	11.9	12.0	12.1	0.468	0.472	0.476
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.10	—	0.21	0.004	—	0.008
e	—	0.50	—	—	0.020	—
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	—	0.80	—	—	0.031	—
Y	—	—	0.10	—	—	0.004
θ	0	—	5	0	—	5

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A0	Nov. 1998	-	Advance Information only, some parameters & waveforms are to be determined.
A1	Jun. 1999	-	Updated Product Number to W49S201, Device Codes, and some AC parameters.

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